

Wing LDA

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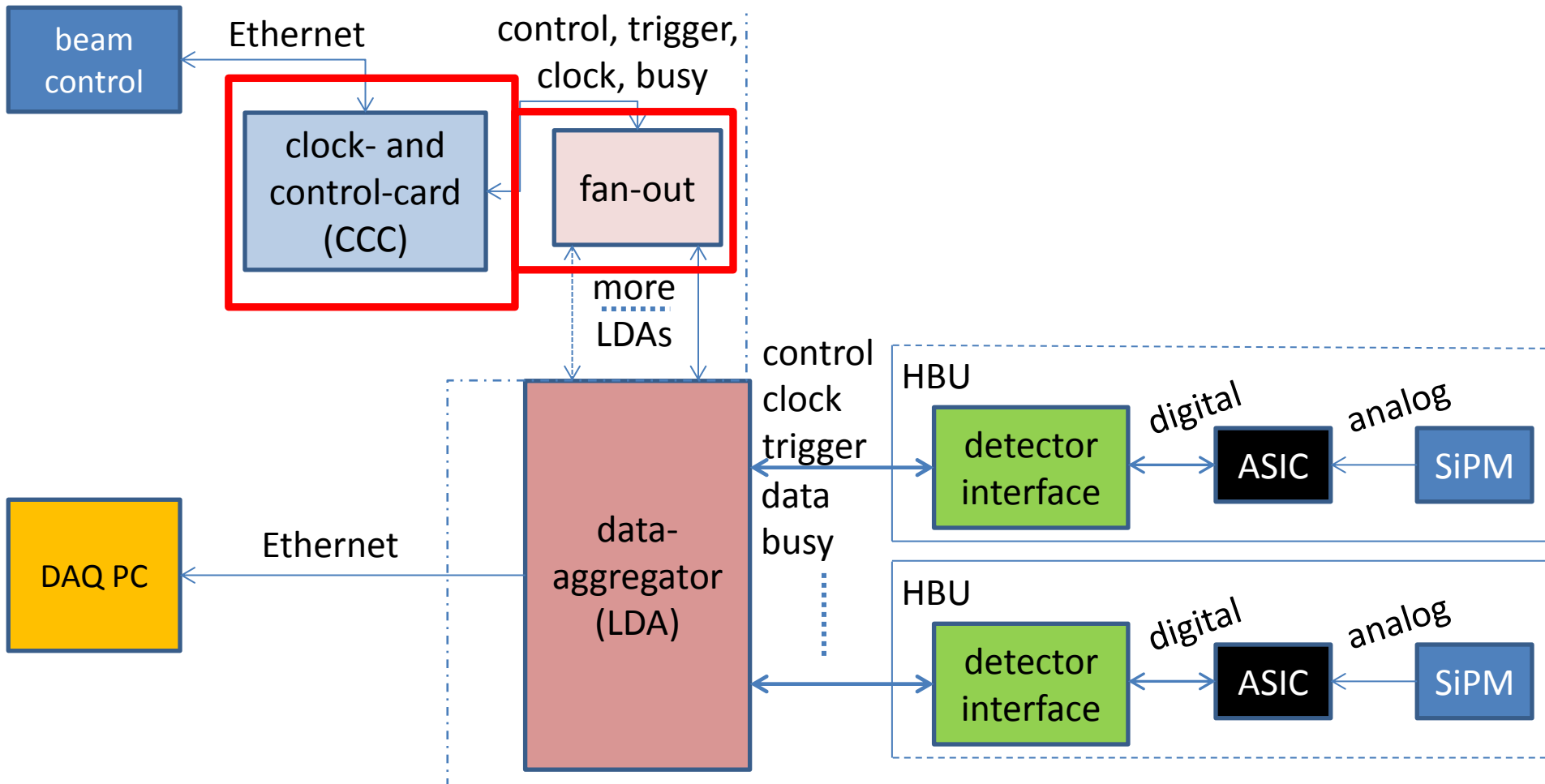
JOHANNES GUTENBERG
UNIVERSITÄT MAINZ



Read-out-chain

off-detector-electronic

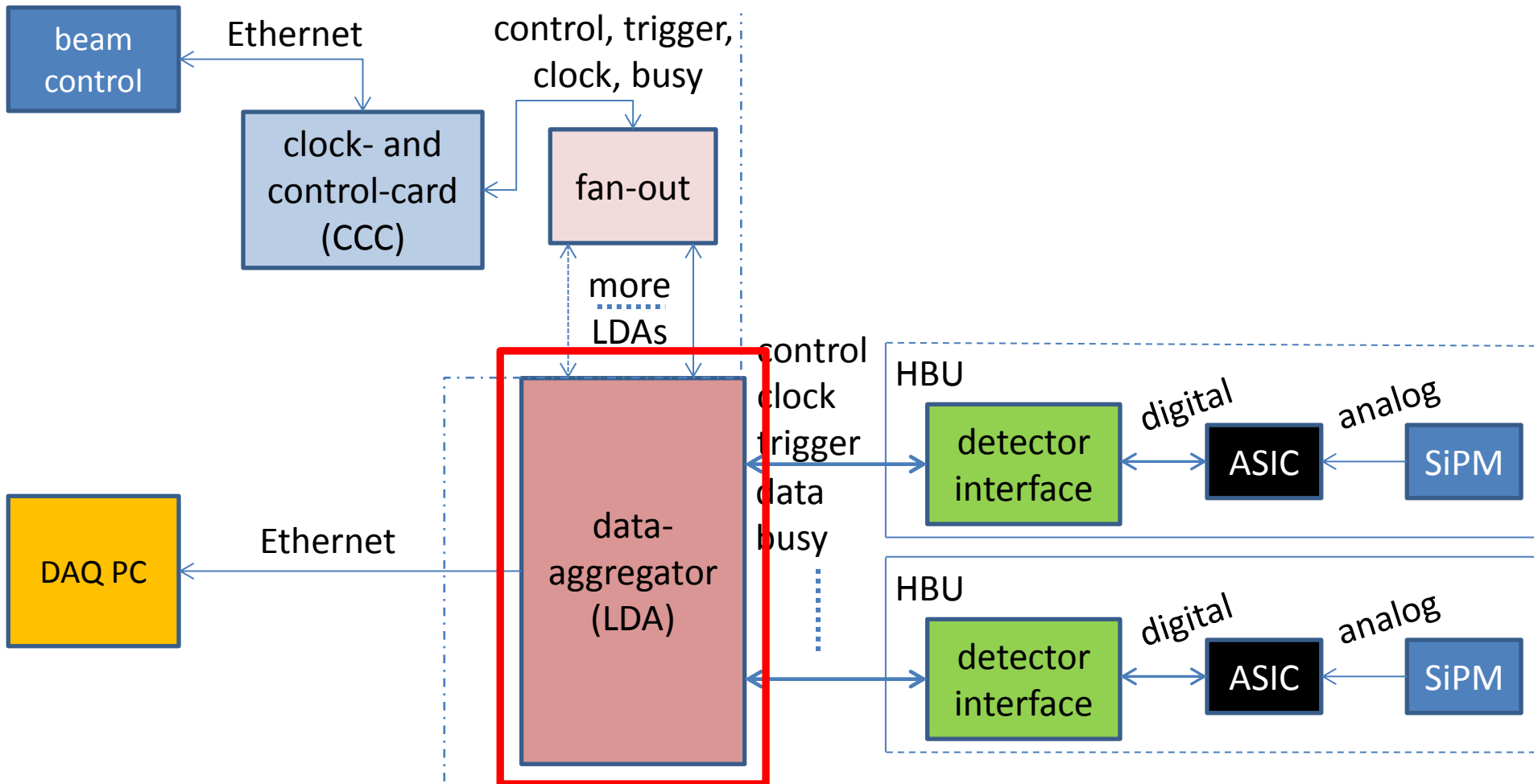
on-detector-electronic



Read-out-chain

off-detector-electronic

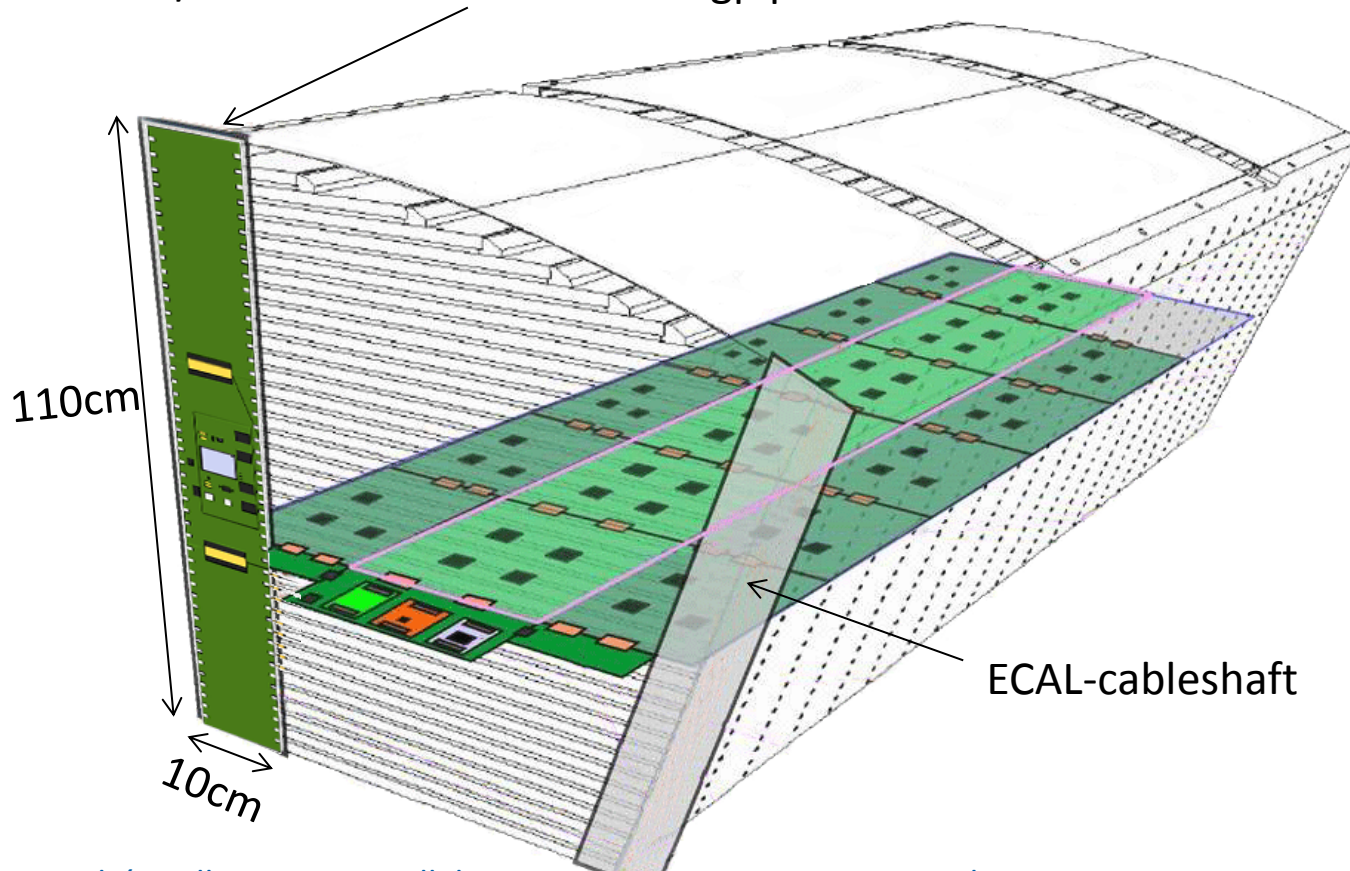
on-detector-electronic



Position of the LDA

LDA integrated in the 10x10cm cables shaft:

HCAL- /TPC-cabelshaft with coolingpipes



challenges:

problems:

- LDA outside of the detector
- 96 cables in the cables shaft

solution/problem:

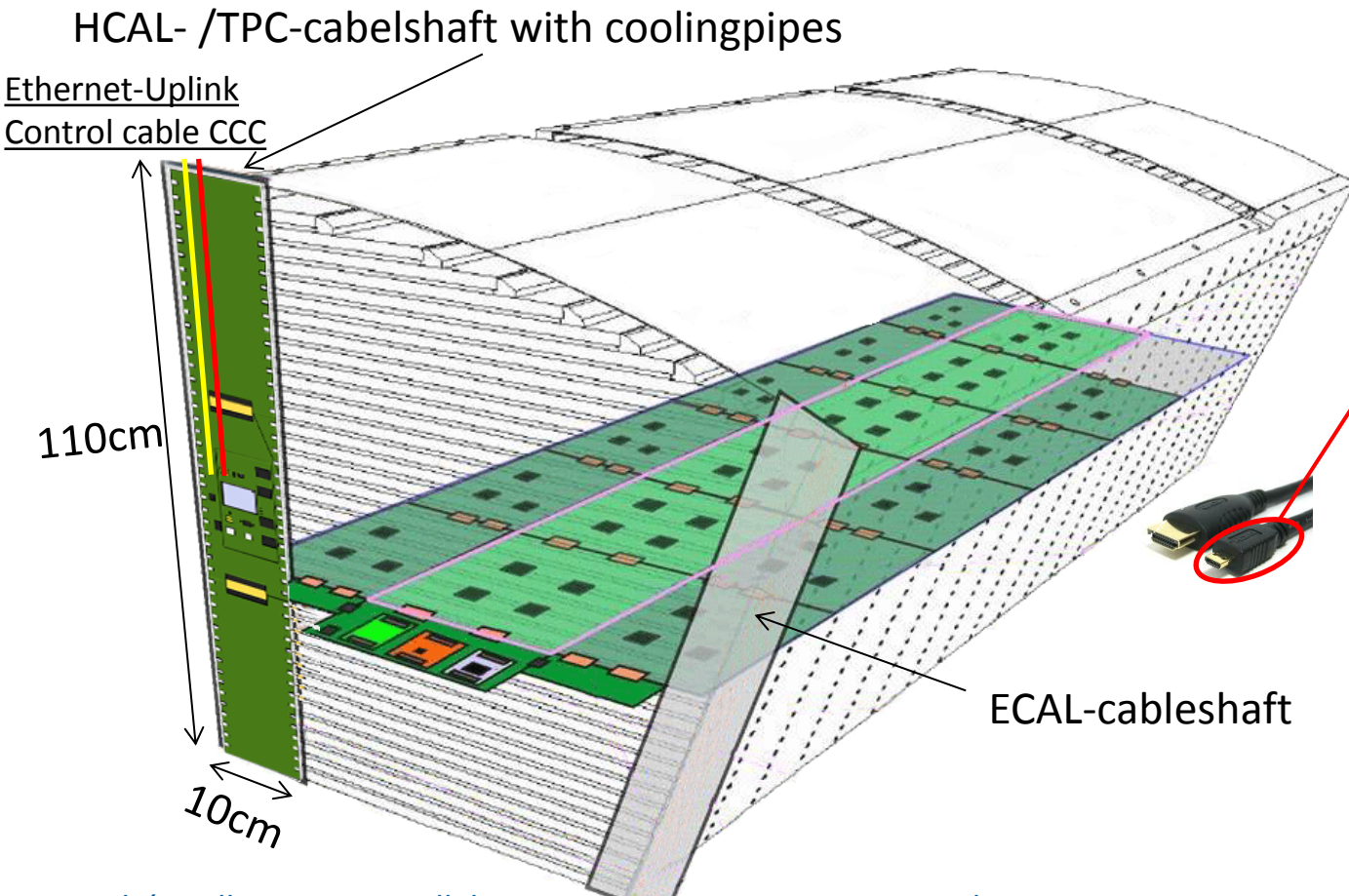
- 110 cm PCB
- timedelay between each layer (up to 5ns)

solution:

- on-board-electronic regulates timing differences

Position of the LDA

LDA integrated in the 10x10cm cables shaft:



challenges:

problems:

- Pitch between the 48 layers depends on (18/23 mm for W/Fe)

solution:

→ Smallest possible HDMI micro connector

- Now only
 - One Ethernet cable
 - One control cable in the detector

Active and Passive

LDA consists of 4 parts:

1. Three passive PCBs:

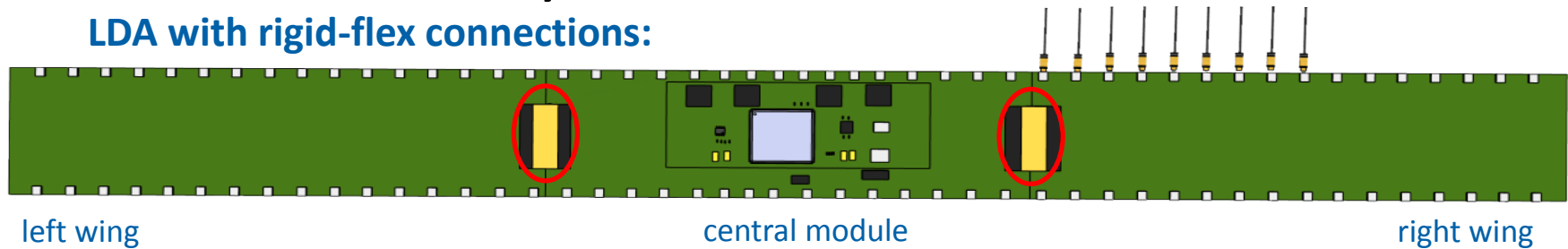
The 96 connectors are on these PCBs.

2. One active PCB:

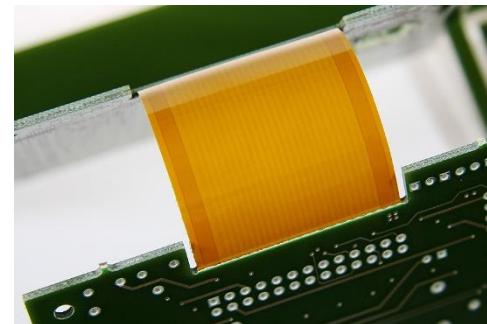
it is a daughter module for tests and fast repairs.

Mechanic and flexibility:

LDA with rigid-flex connections:



rigid-flex connection

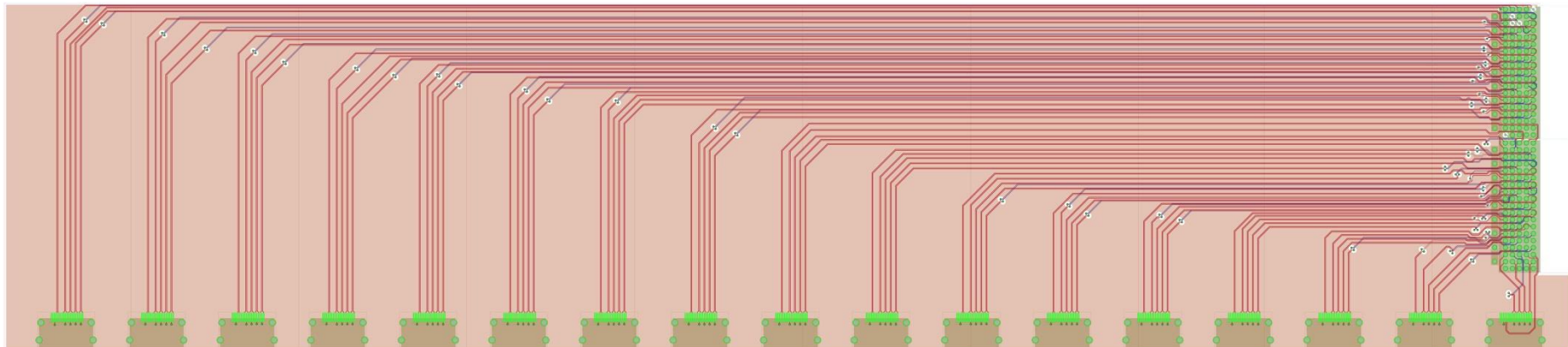


Wing-LDA

old ideas

The first PCB:

1. Wing with 17 HDMI-connectors routed:



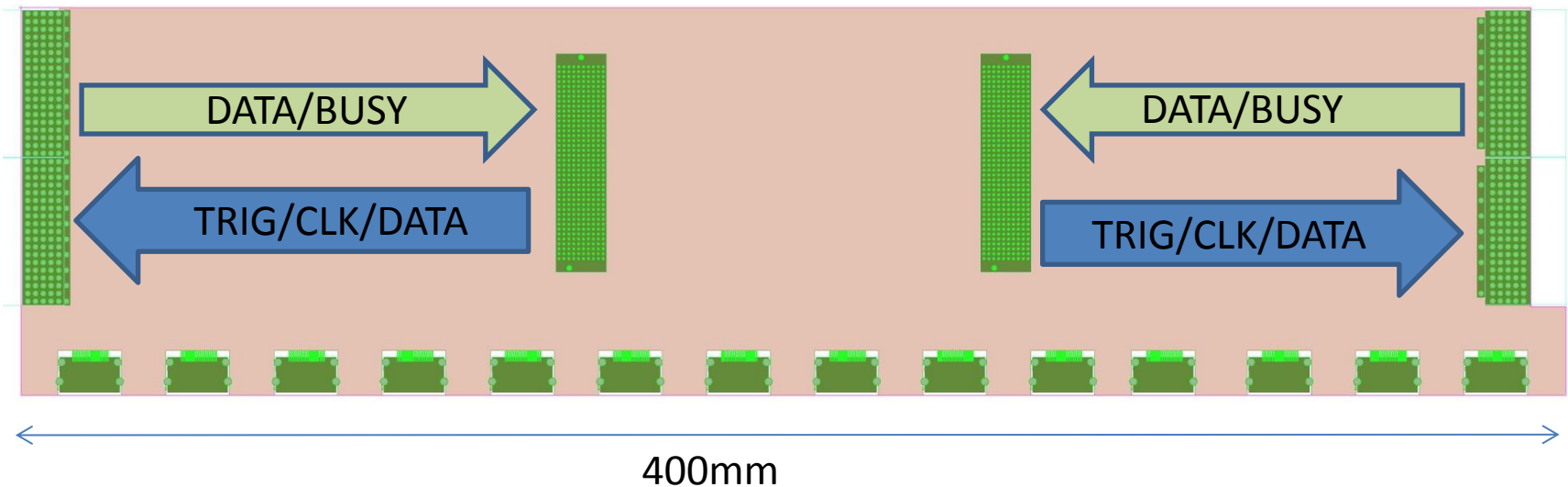
450mm

Wing-LDA

old ideas

The second PCB:

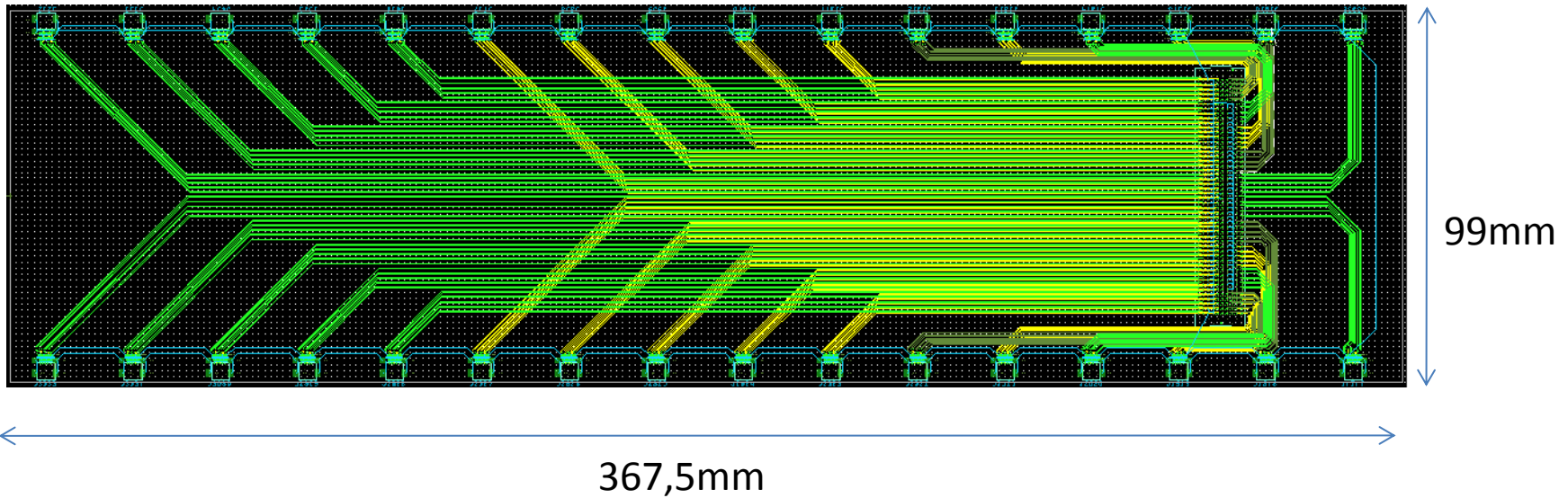
2. Center PCB with 12 HDMI-connectors:



LDA Layout

Passive PCB:

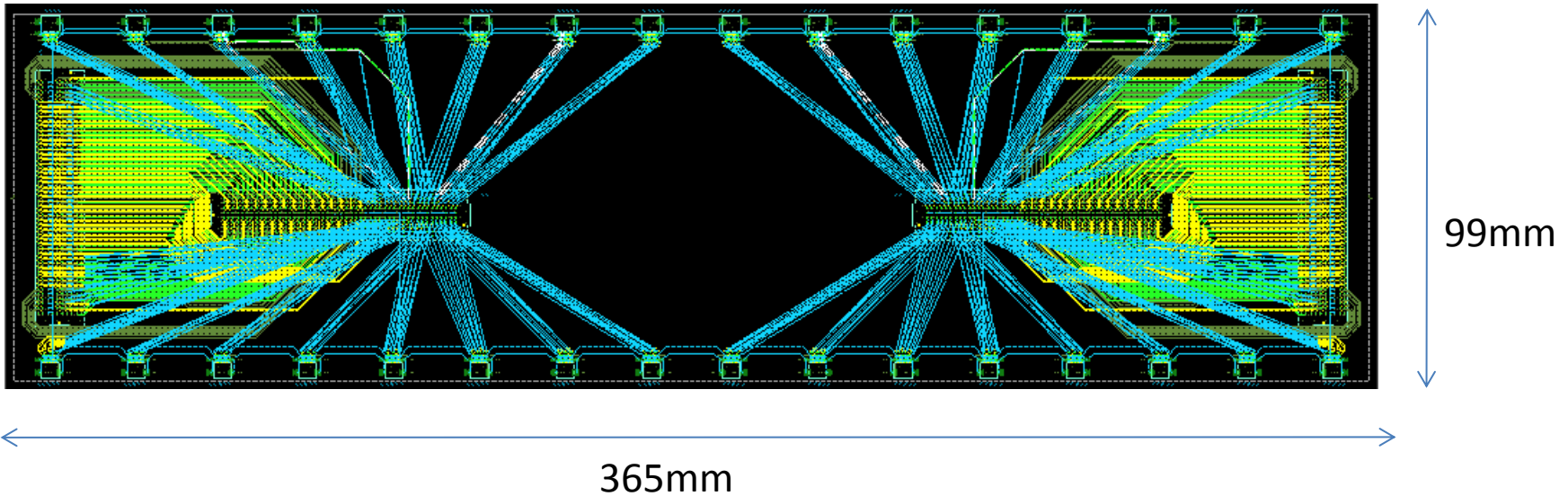
1. Wing with 32 HDMI connectors:



LDA Layout

Passive PCB:

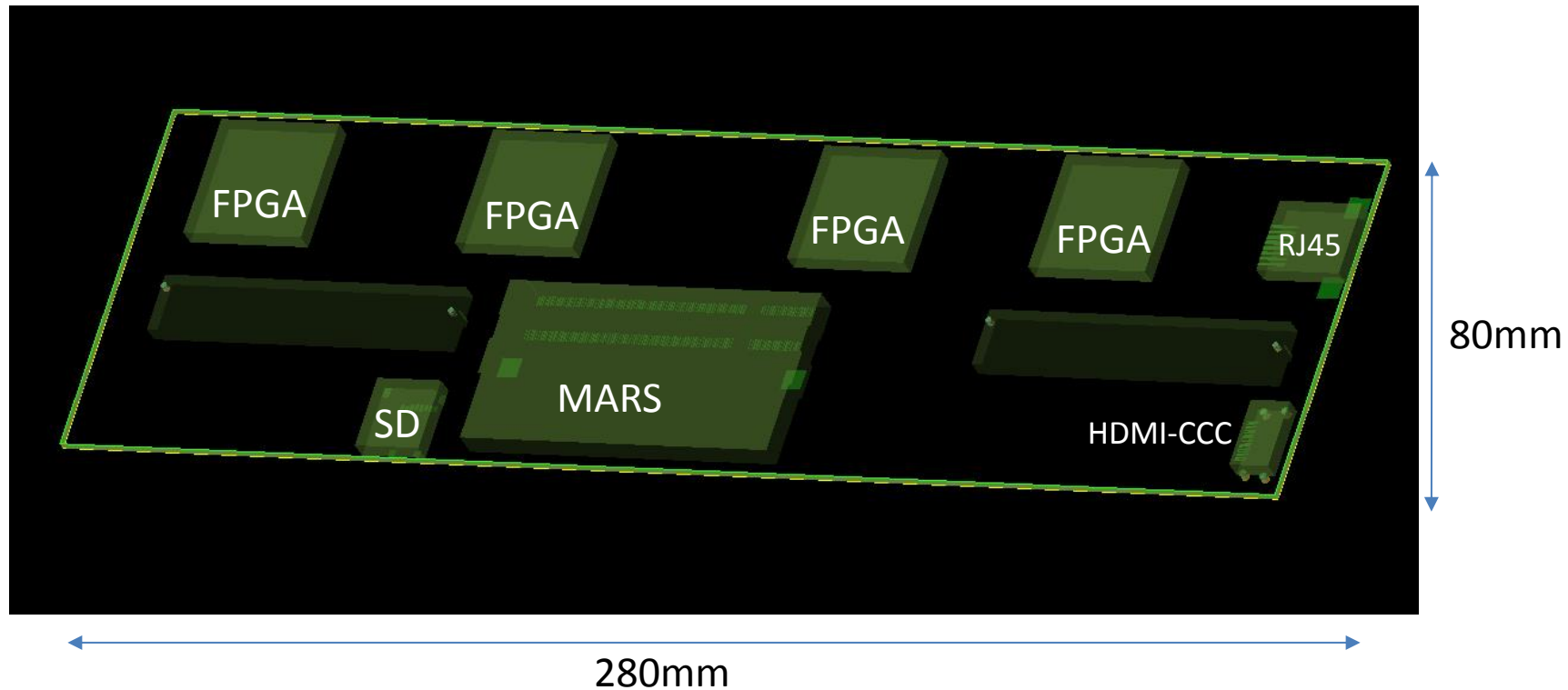
2. Central module with 32 HDMI connectors:



LDA Layout

Active PCB:

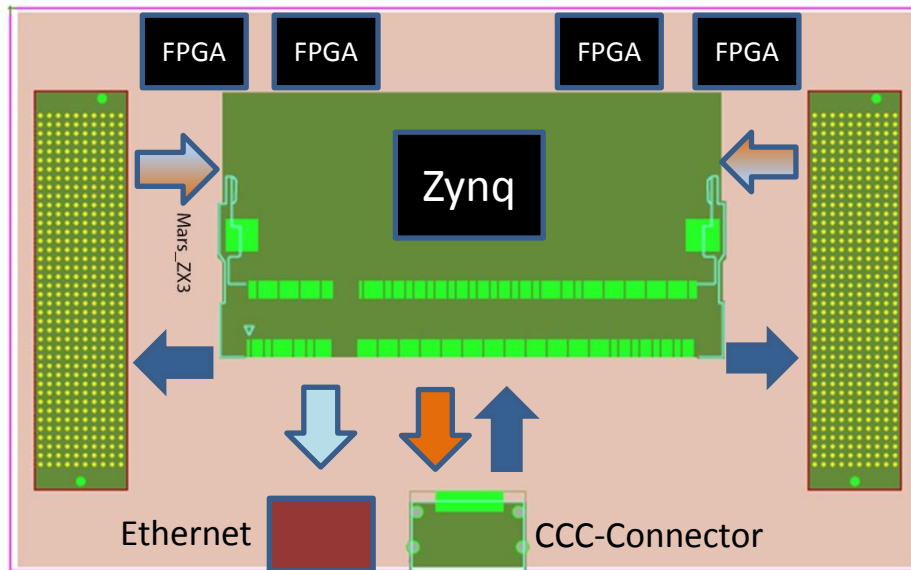
3. Daughter module with 4 FPGAs and a Mars module:



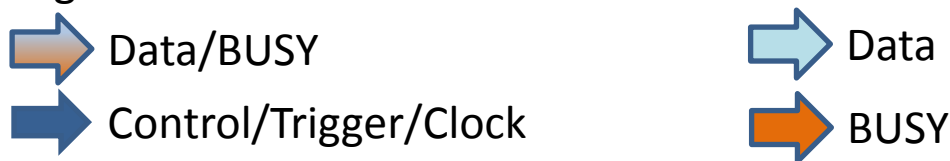
LDA

Active PCB:

3. FPGA daughter module



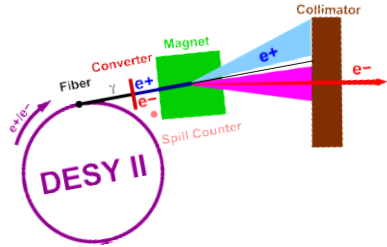
Legend: 280mm



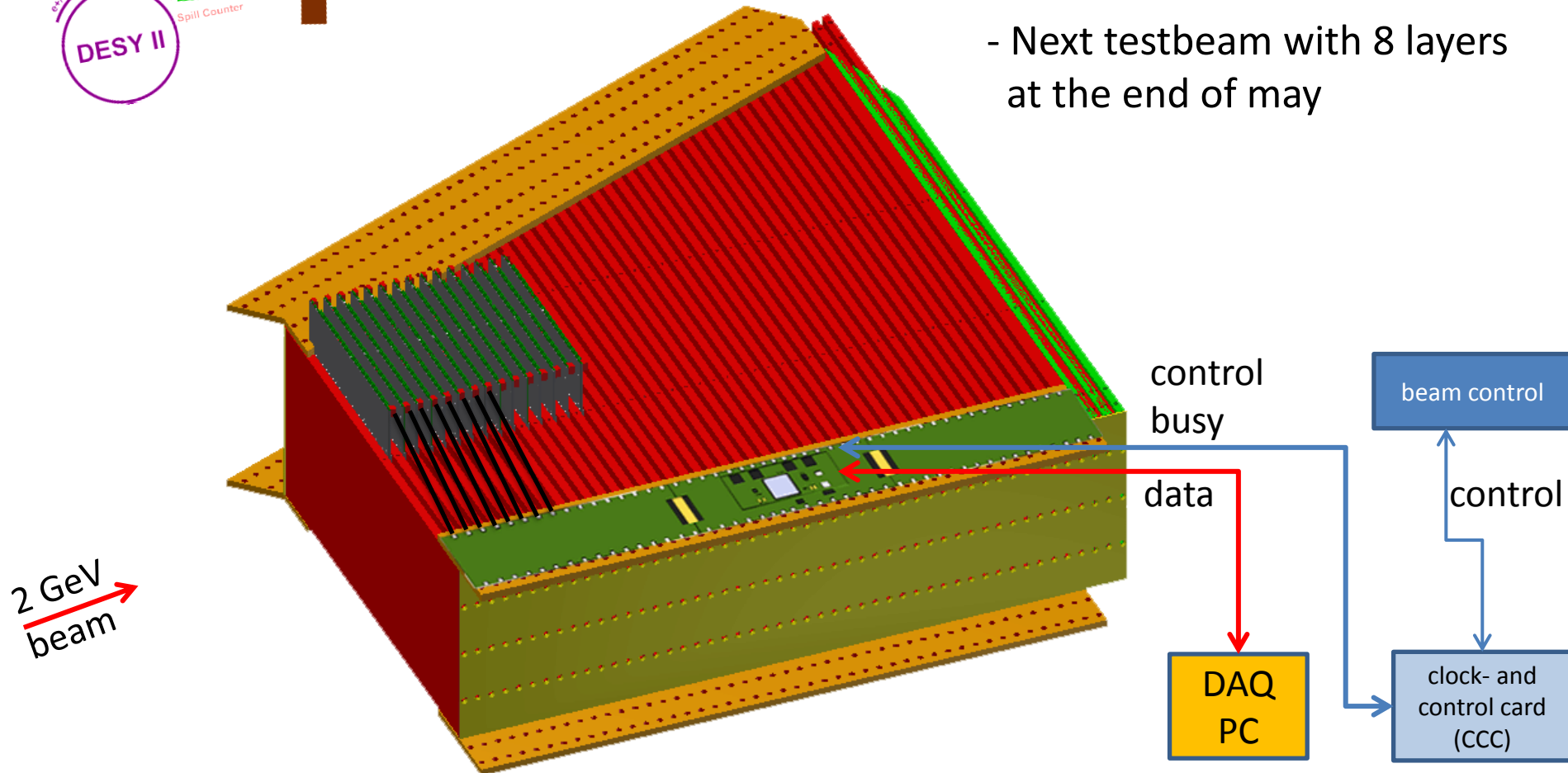
Peculiarity:

- Manages 1100 signals and sends them over the Ethernet
- Has a Zynq processor who
 - has implemented an Arm9 dual core (with Linux)
 - and one FPGA
- Same module as CCC

May 2013 Testbeam (DESY)



- Next testbeam with 8 layers at the end of may



LDA Status

- **LDA collects parallel data from 96 detector layers and leads the clock to each of them without a timing delay**
- **80% of the LDA design is finished**
- **Order the PCBs in 1 week**
- **Firmware will be finished in 1 month**
- **Software is finished**
- **Ready to readout two full ILD detector segments with 48 layers each**

Integration of CCC and LDA

Steps:

1. Read-out data and send slow control data from the HBU layers as before over USB, but integrate the CCC for clock, trigger and busy signals
2. Read-out data by USB but send slow control data, clock, busy, trigger over the CCC
3. Integrate the LDA for data read-out instead of the USB, without interference from us in the regular data acquisition
4. Firmware and software will be written by us, so we don't interrupt the manpower on the DIF side

**Thank you for your
attention!**