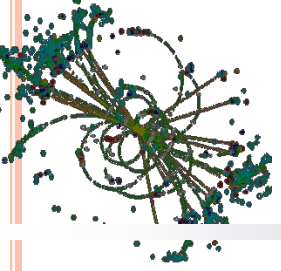# STATUS OF THE CHRONOPIXEL PROJECT

N. B. Sinev

University of Oregon, Eugene

In collaboration with J.E.Brau, D.M.Strom (University of Oregon, Eugene, OR), C.Baltay, H.Neal, D.Rabinovitz (Yale University, New Haven, CT)
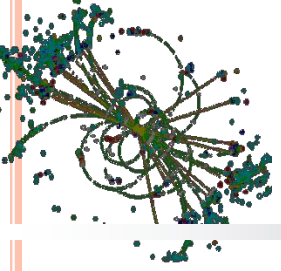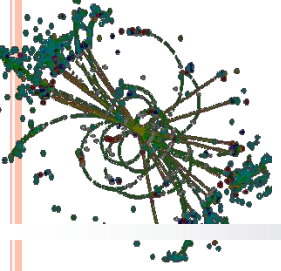
EE work is contracted to Sarnoff Corporation

1

- Just reminder: what is chronopixel?
- Project timeline
- Prototype 1 design and problems
- What is new in prototype 2
- Results of the second prototype tests.
- Conclusions and plans

2

WHAT IS CHRONOPIXEL?

- Need for pixel detector with good time resolution:
  - Background hits density in ILC environment is of the order of 0.03 hits/mm² per bunch.
  - Bunch train at ILC, which lasts only 1 ms, has about 3000 bunches ⇒ 100 hits/mm² – too high for comfortable track reconstruction.
  - So we need to slice this array of hits into at least 100 time slices, and reconstruct tracks from hits belonging to the same slice. To do this, we need to know time of each hit with at least 10 µs accuracy.
- CCDs, often used as pixel detectors, by the nature of their readout, are very slow. Row by row readout takes tens if not hundreds of ms to read image. So we would integrate the entire bunch train in one readout frame.
- There is a number of pixel sensor R&D addressing this problem – CPCCD, different types of monolithic designs (readout electronics on the same chip as sensor), 3D technology. Neither of them (except 3D) allows assigning time stamp to each hit.
- Chronopixel project was conceived to provide such ability.
- Chronopixel is a monolithic (unlike 3D) CMOS pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and record the time (time stamp) of each hit.

3

TIMELINE

- 2004 – talks with Sarnoff Corporation started.
  - Oregon University, Yale University and Sarnoff Corporation collaboration formed.
- January, 2007
  - Completed design – Chronopixel
    - **2 buffers, with calibration**
- May 2008
  - Fabricated 80 5x5 mm chips, containing 80x80 50 µm Chronopixels array (+ 2 single pixels) each
  - TSMC 0.18 µm $\Rightarrow$ ~50 µm pixel
    - Epi-layer only 7 µm
    - Low resistivity (~10 ohm*cm) silicon
- October 2008
  - Design of test boards started at SLAC
- August 2009
  - Debugging and calibration of test boards
- September 2009
  - Chronopixel chip tests started
- March 2010
  - Tests completed, report written

- May 2010
  - Second prototype design started
- September 2010
  - contract with Sarnoff for developing of second prototype signed.
- February 2012
  - Submitted to MOSIS for production at TSMC.
  - Modification of the test stand started as all signal specifications were defined.
- June 6, 2012
  - 11 packaged chips delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
  - Tests at SLAC started
- January 2013 – discussion with Sarnoff about design of prototype 3

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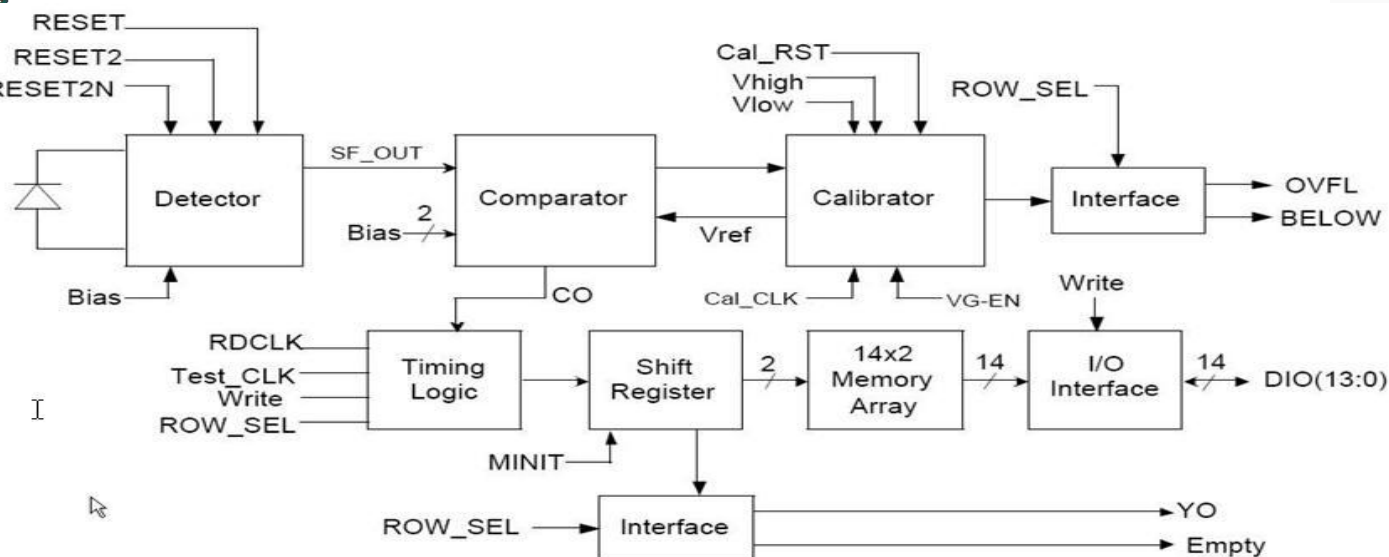
- Monolithic CMOS pixel detector design with time stamping capability was developed in collaboration with Sarnoff company.

- When signal generated by particle crossing sensitive layer exceeds threshold, snapshot of the time stamp, provided by 14 bits bus is recorded into pixel memory, and memory pointer is advanced.

- If another particle hits the same pixel during the same bunch train, second memory cell is used for this event time stamp.

- During readout, which happens between bunch trains, pixels which do not have any time stamp records, generate EMPTY signal, which advances IO-MUX circuit to next pixel without wasting any time. This speeds up readout by factor of about 100.

- Comparator offsets of individual pixels are determined in the calibration cycle, stored in digital form, and reference voltage, which sets the comparator threshold, is shifted to adjust thresholds in all pixels to the same signal level.

- To achieve required noise level (about 25 e r.m.s.) special reset circuit (soft reset with feedback) was developed by Sarnoff designers. They claim it reduces reset noise by factor of 2.
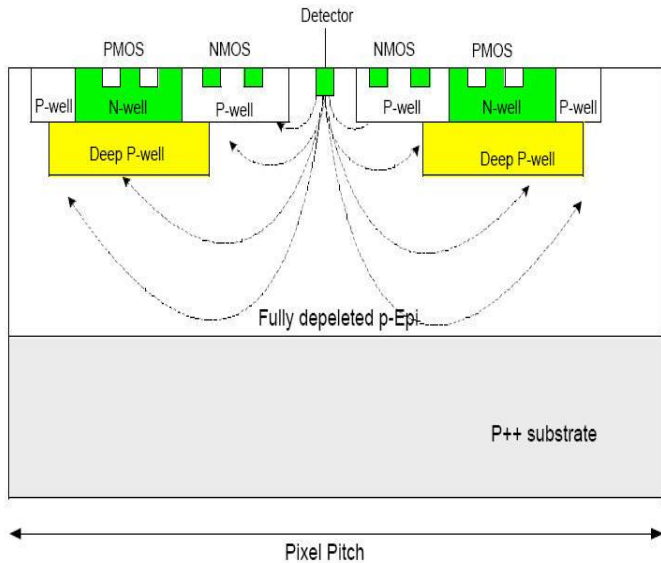
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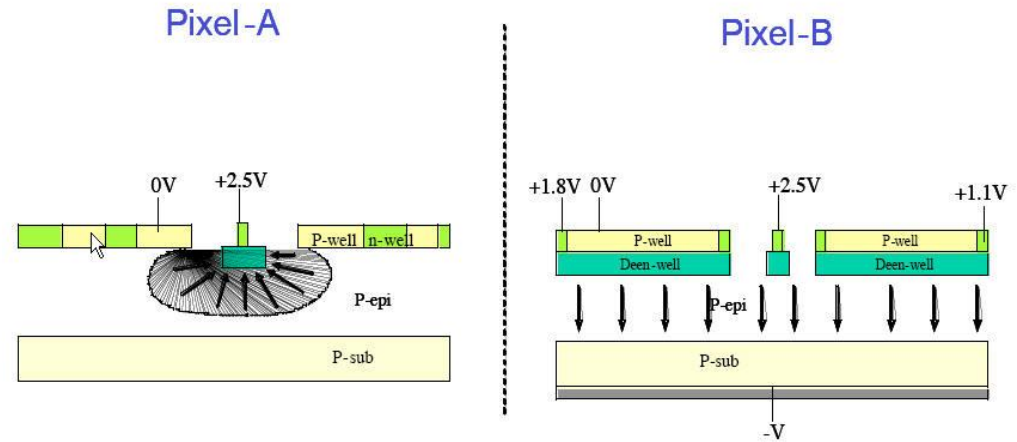Figure 11.1 Proposed pixel architecture employing the deep p-well layer

Figure 6.3 Comparison of the vertical cross section views of two pixels

**Ultimate design, as was envisioned   Two sensor options in the fabricated chips**

- TSMC process does not allow for creation of deep P-wells. Moreover, the test chronopixel devices were fabricated using low resistivity (~ 10 ohm*cm) epi layer. To be able to achieve comfortable depletion depth, Pixel-B employs deep n-well, encapsulating all p-wells in the NMOS gates. This allow application of negative (up to -10 V) bias on substrate.

6
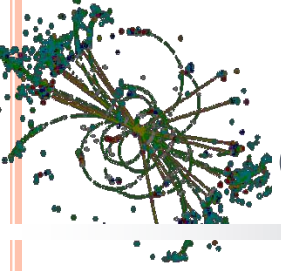
- Tests of the first chronopixel prototypes are now completed.
- Tests show that general concept is working.
- Mistake was made in the power distribution net on the chip, which led to only small portion of it is operational.
- Calibration circuit works as expected in test pixels, but for unknown reason does not work in pixels array.
- Noise figure with "soft reset" is within specifications (0.86 mV/35.7µV/e = 24 e, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is 2.7 times larger required (250 e).
- Sensors leakage currents ($1.8 \cdot 10^{-8}$A/cm^2) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz.
- No problems with pulsing analog power.

7
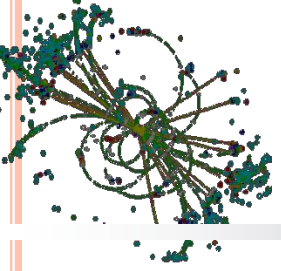
- Problem: need for deep p-well to prevent signal electrons collection by electronics n-wells

- Problem: large spread of comparator offsets requires very fine granularity in the offset compensating circuit

- Problem: pixels are too large (50x50 μ^2).

- Solution: make all electronics from NMOS transistors – their shallow p-well bodies reflect electrons

- Solution: use analog calibration circuit instead of digital. It eliminates problem with granularity.

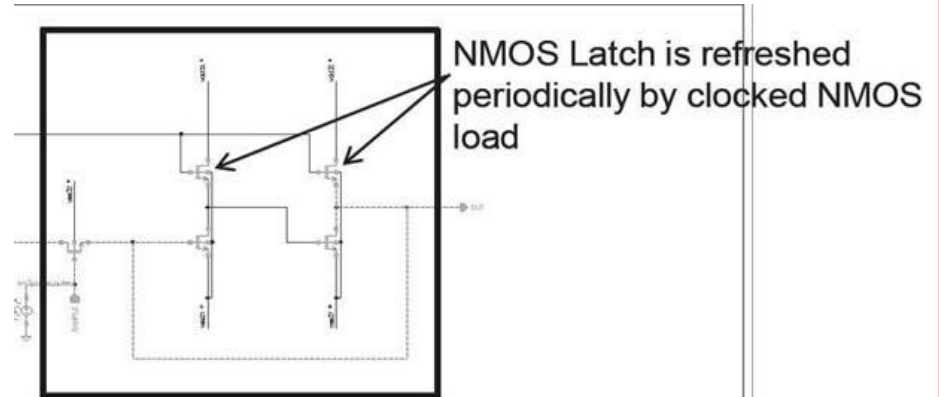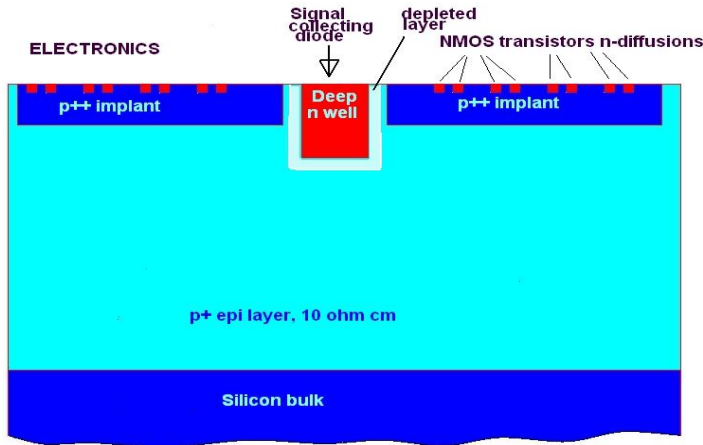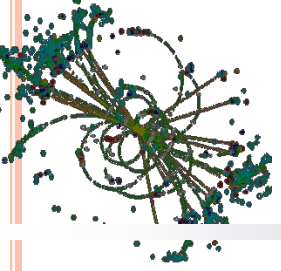- Solution: use 90 nm technology instead of 180 nm in first prototype

8
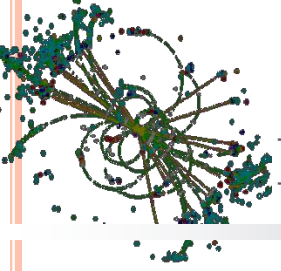
- Design of the next prototype was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all electronics inside pixels only from NMOS transistors. It can allow us to have 100% charge collection without use of deep P-well technology, which is expensive and rare. To reduce all NMOS logics power consumption, dynamic memory cells design was proposed by SARNOFF.

- New comparator offset compensation ("calibration") scheme was suggested, which does not have limitation in the range of the offset voltages it can compensate.

- We agreed not to implement sparse readout in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.

- In September of 2011 Sarnoff suggested to build next prototype on 90 nm technology, which will allow to reduce pixel size to 25μ x 25μ

- We agreed to have small fraction of the electronics inside pixel to have PMOS transistors. Though it will reduce charge collection efficiency, but will simplify comparator design. It is very difficult to build good comparator with low power consumption on NMOS only transistors.
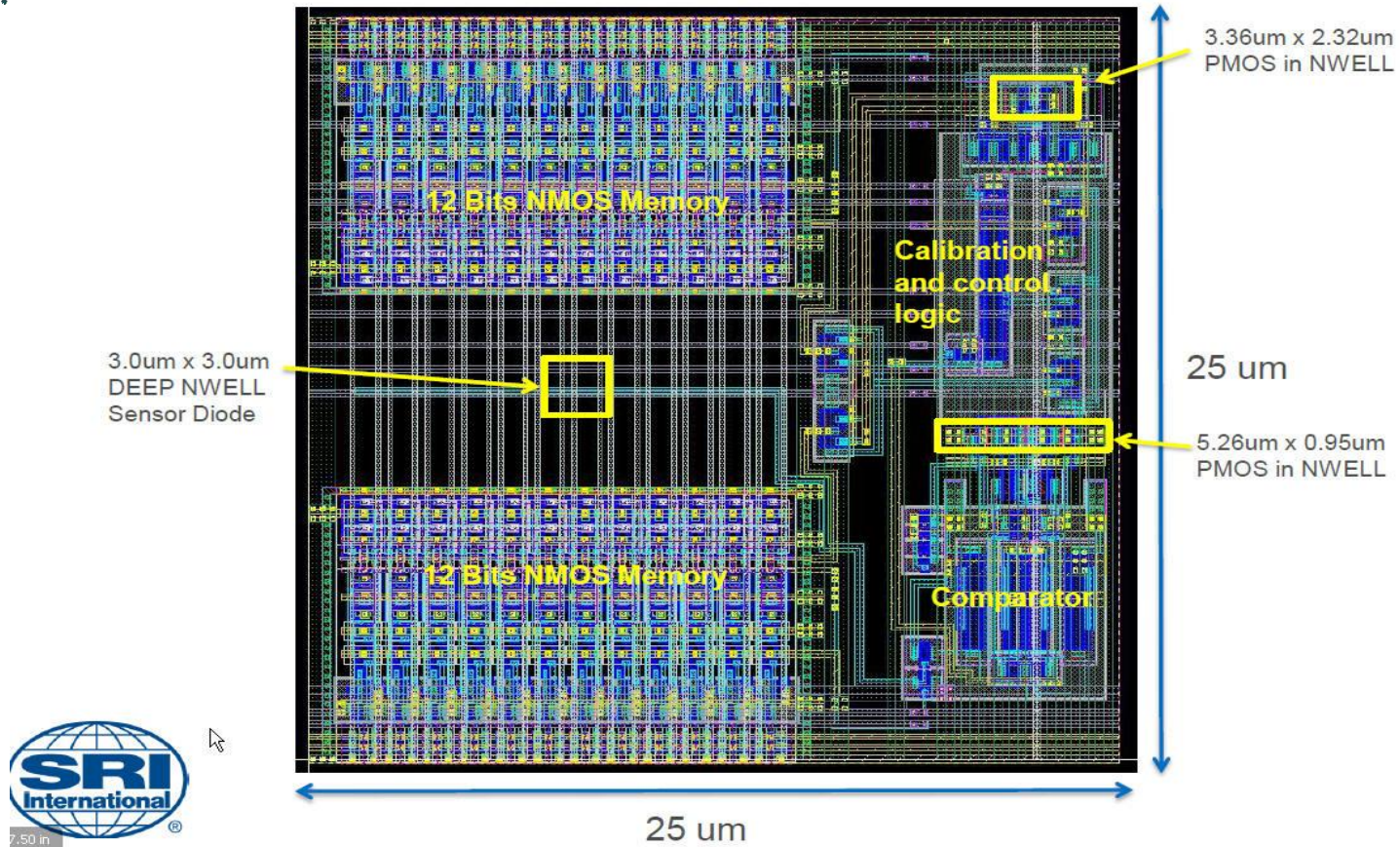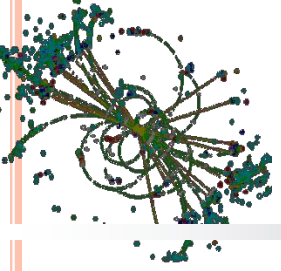
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ELECTRONICS

Signal collecting diode

depleted layer

NMOS transistors n-diffusions

Deep n well

p++ implant

p++ implant

p+ epi layer, 10 ohm cm

Silicon bulk

We expected that new prototype sensor cross-section will look like shown on the picture

NMOS Latch is refreshed periodically by clocked NMOS load

Clocked Dynamic NMOS Latch is a very efficient memory element. NMOS inverters and NOR gates can also be clocked to save on static power consumption.

Proposed dynamic latch (memory cell) has technical problem in achieving very low power consumption. The problem is in the fact, that NMOS loads can't have very low current in conducting state – lower practical limit is 3-5µA. This necessitate in the use of very short pulses for refreshing to keep power within specified limit. However, we have suggested solution to this problem, which allows to reduce average current to required value without need for short pulses.

10

3.36um x 2.32um
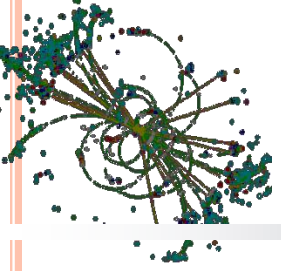PMOS in NWELL

25 um

5.26um x 0.95um
PMOS in NWELL

12 Bits NMOS Memory

Calibration and control logic

12 Bits NMOS Memory

Comparator

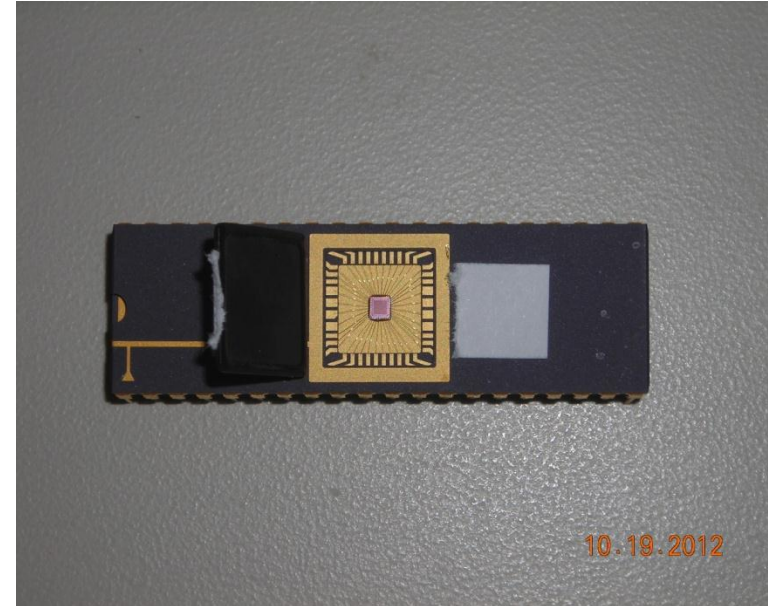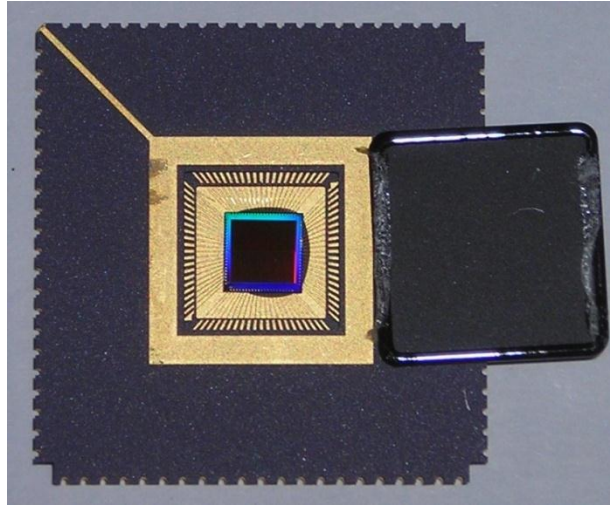3.0um x 3.0um
DEEP NWELL
Sensor Diode

25 um

12

All **N-wells** (shown by yellow rectangles) are **competing** for signal charge collection. To **increase fraction of** charge, collected by **signal electrode (DEEP NWELL)**, half of the pixels have it's **size increased to 4x5.5 µ²** .

11
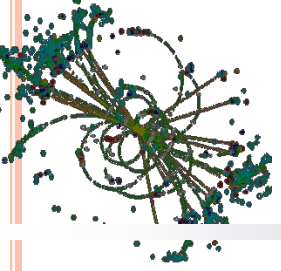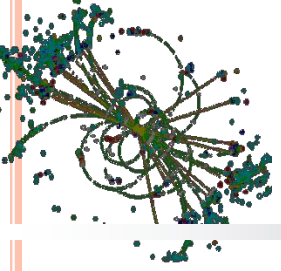
- Because of much smaller chip size for prototype 2, there is not enough room on chip periphery to make 84 pads, as it was in prototype 1. So, 40 pads and 40 pins package were used.
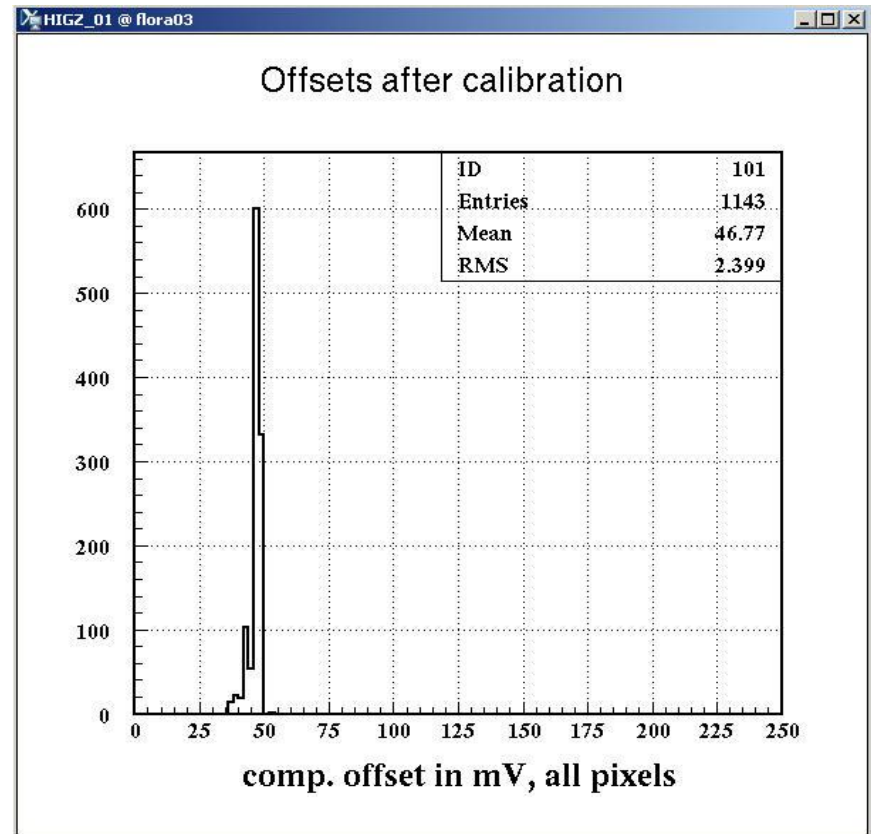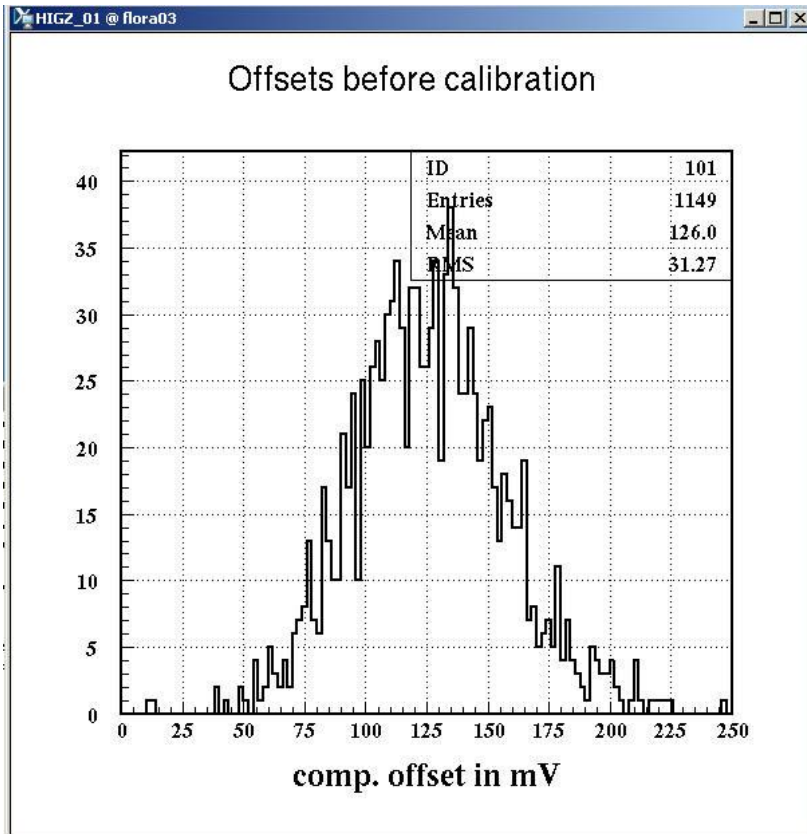
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PIXEL VARIATIONS

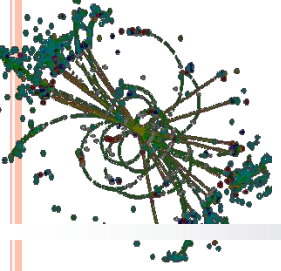- As soon as Sarnoff design manager gave me final schematics, I started SPICE simulation of it performance to double check their simulations. Suggested by them comparator design did not pass my check – it appeared very sensitive to the rise time of the latch signal. So I insisted that they use old (prototype 1) comparator, which did not have such a problem. But they also wanted to test their new design as they believed that with additional latch signal shaping it should work and it have better switching characteristics. So, we agreed to have half of the pixels have their new design.

- They wanted to have charge collection electrode only 3x3 μ^2 to have low noise level. However, with 12 μ^2 of PMOS transistors in the pixel it would lead to charge collection efficiency less than 50% . From my calculations of noise and charge collection efficiency the optimal (providing maximum signal/noise ratio) charge collection electrode should have about 22 μ^2 area. So, we decided to have half of the pixels with 9 μ^2 (in final layout it appeared to be 14 μ^2) charge collection electrode area (to check how much it helps with noise reduction), and half – with 22 μ^2 .

- That leads to 4 different variants of the pixel, which are implemented in each chip.

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Offsets before calibration

ID	101
Entries	1149
Mean	126.0
RMS	31.27

comp. offset in mV

Offsets after calibration

ID	101
Entries	1143
Mean	46.77
RMS	2.399

comp. offset in mV, all pixels
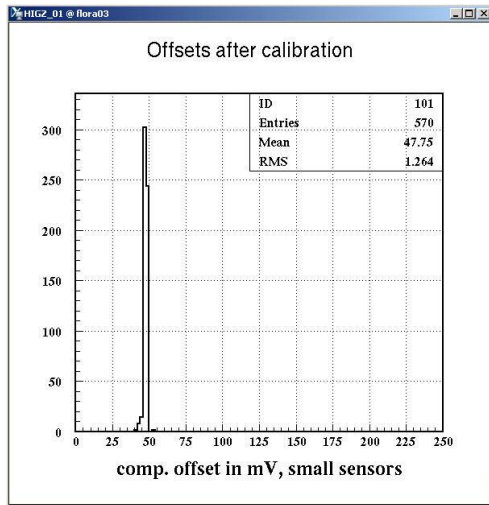
Before calibration voltage on the calibration capacitors were set to value that all comparators are in fired state at 0 threshold. During calibration this voltage changes to the point when comparators flip to non-fired state. To measure offsets I have used 50 mV pulse to get S-curves – probability of comparator be fired as function of threshold.
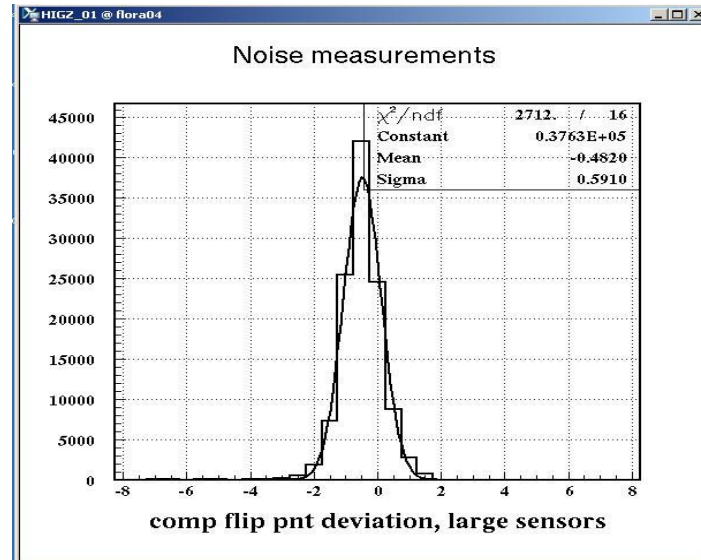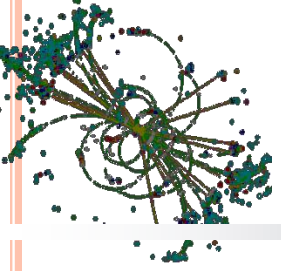
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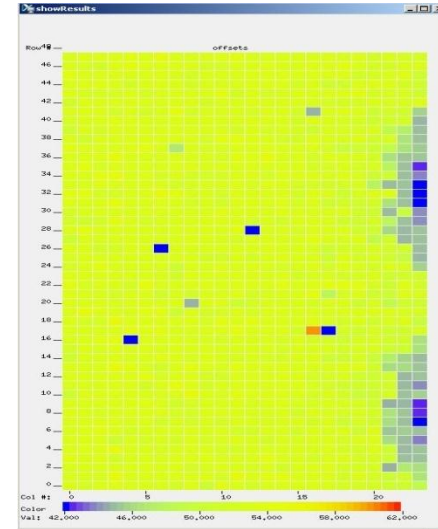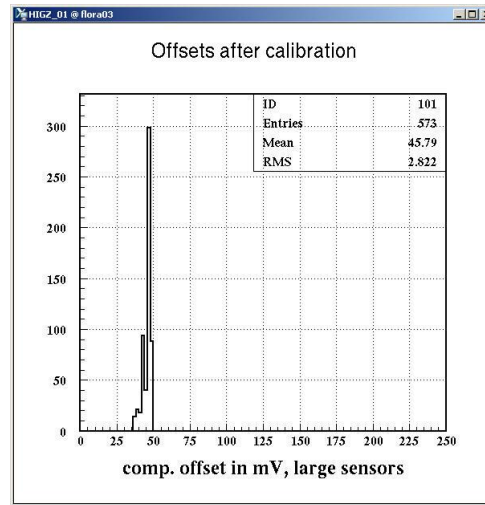
- Why calibration did not make offsets distribution like δ-function? On the left plot wee see this distribution for pixels in the left part of the chip (look at map at right). They have small sensor diodes, but what matters here is that they are far from chip periphery, where all drivers are sitting. This distribution is close to what we expect. Distribution on the plot in the middle is for 12 columns at the edge of the chip (large sensor diodes). And anomalous offsets, seen on the pixels map in bluish colors are in the pixels, close to clock drivers. So, there are some cross-talks from drivers. (4 completely blue pixels on this map – just "bad pixels", having memory problems, we don't care about them for now.) **15**

Noise measurements — comp flip pnt deviation, small sensors

χ^2/ndf = 1805. / 20
Constant = 0.3077E+05
Mean = -0.5062
Sigma = 0.7276

Noise measurements — comp flip pnt deviation, large sensors

χ^2/ndf = 2712. / 16
Constant = 0.3763E+05
Mean = -0.4820
Sigma = 0.5910
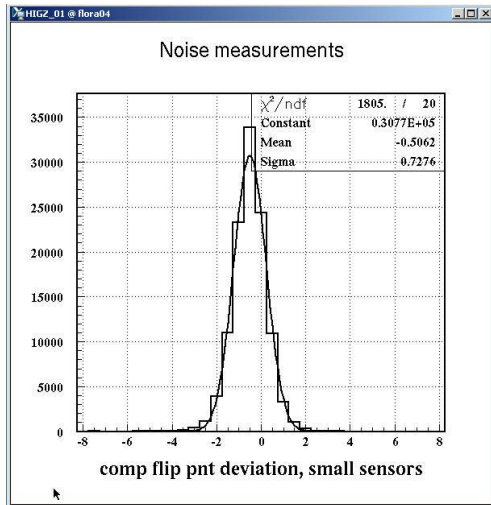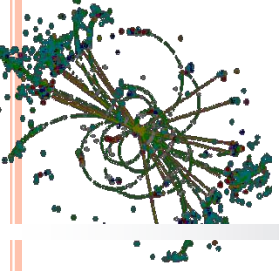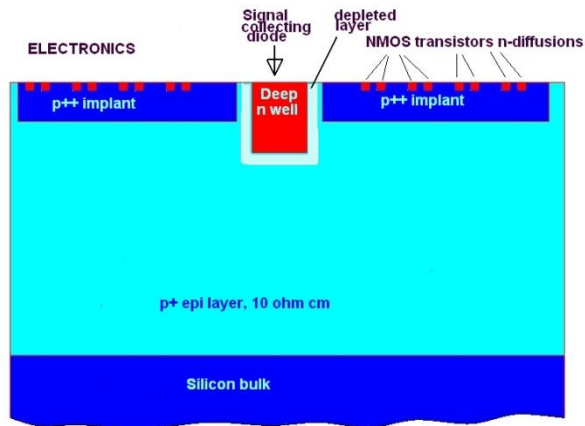
○ Noise distributions for pixels with smaller (on the left) and larger (right) sensor diode area. If we assume, that reset (KTC) noise is dominant, we can calculate the value of sensor capacitance is 7.6 fF and 11.5 fF. It is about 2 times larger than in prototype 1 (about 5 fF), and almost 10 times larger than we expected from sensor area.

16
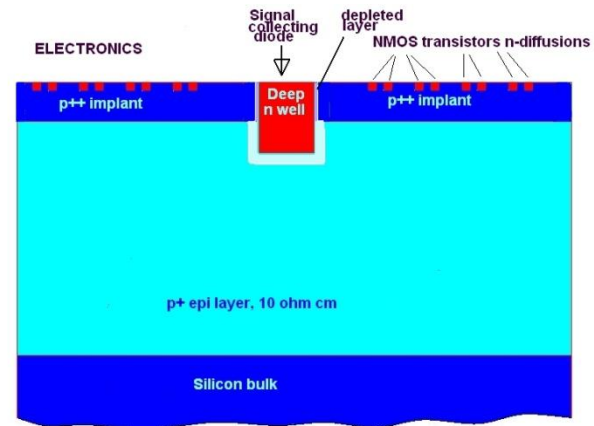
What we expected   **What 90 nm technology allows**

- The reason for that appeared to be in 90 nm technology – design rules prohibiting blocking p++ implant. That means that diodes are sitting in very low resistivity layer, not in 10 ohm*cm epi layer, as was in prototype 1. We don't know yet if this design rule is specific for TSMC process and if there are foundries allowing bypassing it. In principle we don't see fundamental reasons for this rule, as the sensor area does not contain parts requiring 90 nm feature size.

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- Comparison of the Fe 55 signal distributions for prototype 1 and 2. Prototype 2 has 2 sensor size options – 14 μ^2 and 22 μ^2 ("small" and "large" on the plot) . The maximum signal value is roughly in agreement with capacitance estimation from noise distributions, though we would expect larger difference in maximum signal values here. But statistics is very small here to do precise measurements.

Fe 55 test results in prototypes 1 and 2

hits above threshold prototype 1,2

18
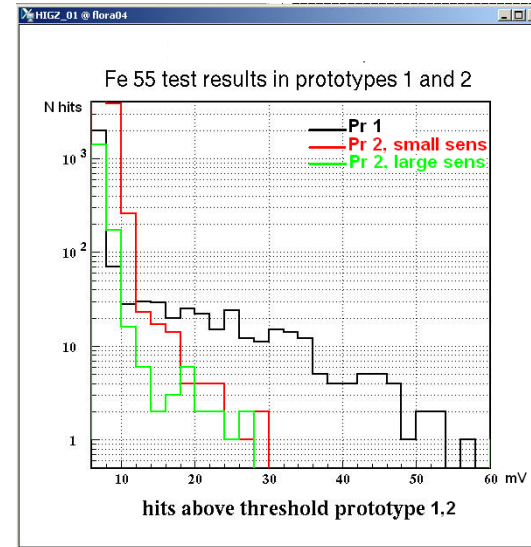
- On the slide 15 you have seen picture clearly showing cross-talks from the clock drivers. As they are clearly concentrates in the proximity of drivers, there is a way to eliminate them – just move drivers father from the pixel area.

- However, another effect also was observed – it appeared that comparator thresholds slightly (by few mV) changing depending on the timestamp value (more precise – on the number of ones in the timestamp code). Investigation led to the conclusion, that recording timestamp code (changing the state of memory bits) creates positive feedback on the comparator input. This is not surprising, because we have common power supply for the memory and comparators. Separating them should solve the problem. But as for now the problem seems to affect noise measurements. Distribution became narrower because firing of the part of comparators (leading to time stamp recording) stimulates firing of others.

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- As we observed, that noise distribution width can be affected by value of the time stamp recorded when comparator is fired (and reading back non-zero time stamp is the only way we can use to detect comparator firing), we can't anymore rely on the noise distribution measurement for sensor capacitance estimation.

- Another way – we can measure how much comparator threshold changes by feed-through from sensor reset pulse. Observed changes for "small" and "large" sensors are 22.38mV and 18.1mV. The ratio, 1.24 is close to the ratio of wells side wall lengths (13.64µ for small and 17.64µ for large, ration 1.29), but not to the ratio of sensor areas ($14µ^2$ and $22µ^2$, ratio 1.57). That corresponds to the explanation of the large sensor capacitance, shown on slide 17. However, it is difficult to estimate absolute value of the sensor capacitance using this measurements, as 90nm technology transistor modeling does not gives me accurate values of the gate to source capacitance.
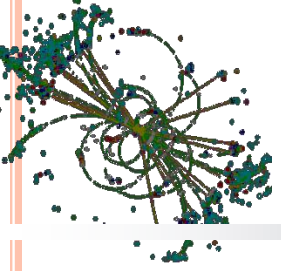
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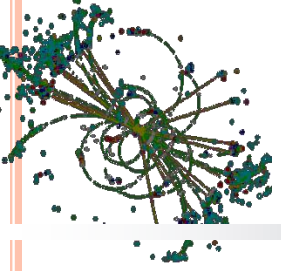
- We are using capacitor to store comparator offset compensating voltage. The concern is, will be the voltage on this capacitor stable within required precision (1 mV) for entire bunch train duration (1 ms). I have measured that these capacitors are discharging by 1 mV in about 30 ms. So, we have large safety margins here.

- Sensor diode leakage current will lead to the change of the bias voltage during the time diode is disconnected from reset rail. We need to do sensor diode reset every bunch crossing anyway, as we want to remove charge, generated by 1 particle before next particle can hit. So, we are concerned only about keeping voltage on the diode stable for about 1 μs. Measurements have shown, that for such period of time voltage on the sensor diode changes not more than by 0.2 mV.

21
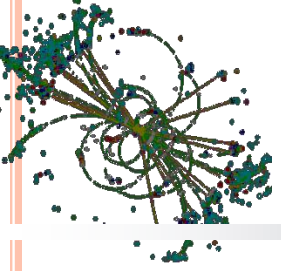
- The goal is to have no more than 0.1μW/pixel.
- Without any power pulsing prototype 2 has about 2μW/pixel.
- Power pulsing works well, there is no problem with it, as I could see. It allows reduction of the power consumed by analog par by factor of ~100. However, because of using all NMOS electronics, about half of the power in the chip goes to time stamp memory, which can't be turned off during readout. Nevertheless, there is solution how to reduce memory power consumption – we can turn off memory in the pixels where there is no hits. It will reduce memory power consumption proportional to sensor occupancy. For the inner layer it may be not enough (see Christian talk – occupancy here may be ~30-40%). But additional resource in the reduction of the memory power is to turn it off after it was read out. And here everything is under our control. So, power consumption can be kept within required limits, with some modifications to readout process.

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CONCLUSIONS AND PLANS

- From both, first and second prototype tests we have learned:
  - 1. We can build pixels which can record time stamps with 300 ns period (1 BC interval) - prototype 1
  - 2. We can build readout system, allowing to read all hit pixels during interval between bunch trains (by implementing sparse readout) - prototype 1
  - 3. We can implement pulsed power with 2 ms ON and 200 ms OFF, and this will not ruin comparator performance - both prototype 1 and 2
  - 4. We can implement all NMOS electronics without unacceptable power consumption - prototype 2. We don't know yet if all NMOS electronics is a good alternative solution to deep P-well option.
  - 5. We can achieve comparators offset calibration with virtually any required precision using analog calibration circuit.
  - 6. Going down to smaller feature size is not as strait forward process as we thought.

- As for the plans:
  - We need to prove that all NMOS transistors is a good solution for charge collection efficiency. Beam tests needed for that.
  - For the next prototype we may find the way to bypass design rules. Engineer from Sarnoff suggested to try implementing "native" transistor structure instead of deep n-well. He claims, that for such structures 90 nm technology allows creation of the window in top implant p++ layer. They are investigating if it will work, and if it will, it solves our problem with high sensor capacitance. And of course, we will try to fix all cross-talks issues.

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