3D Status

SiD Meeting, Ronald Lipton, Fermilab

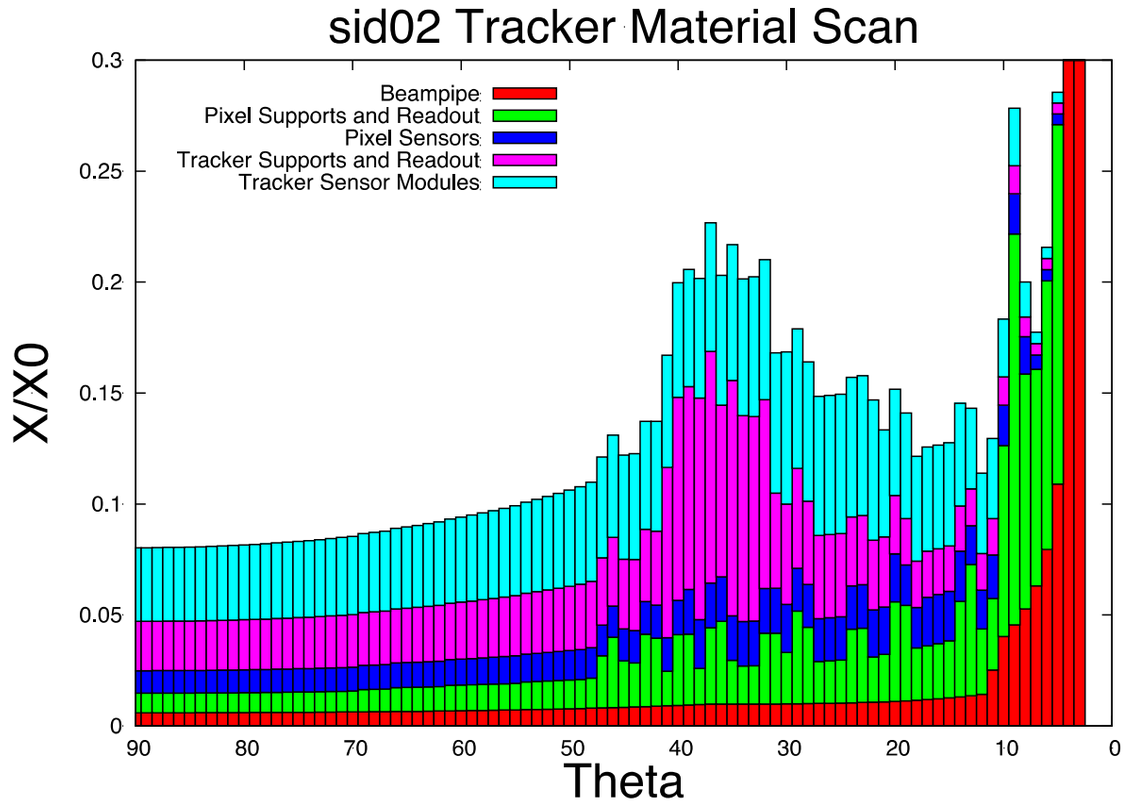
R&D on components of the sensor design:

- 3D Submission - VICTR and VIP testing
- Thinning
- Active edge devices

Vertex Sensor Development

Our initial work on 3D electronics was motivated by the extraordinary requirements for ILC vertex detectors

- ~0.1% radiation length/layer
- time stamping
- 5 micron resolution



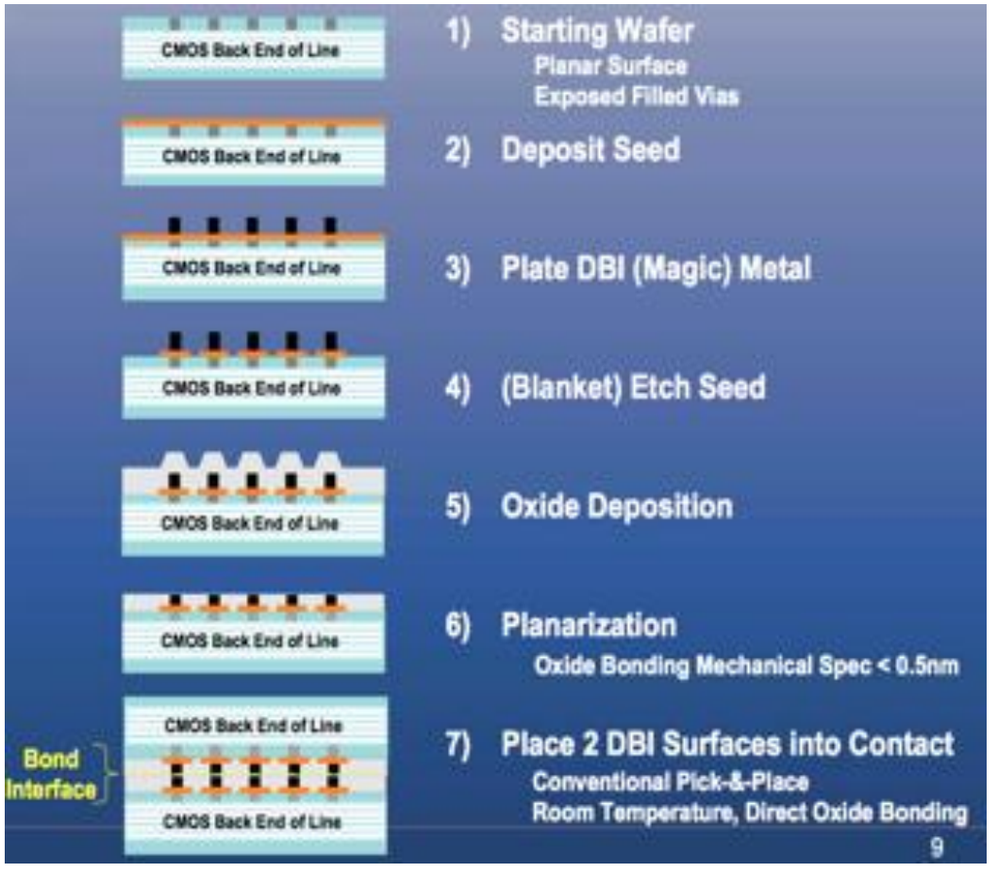
We realized that emerging IC technologies which offer a high density of electronics, fine pitch interconnects, and wafer thinning could offer a solution to the ILC vertex problem.

This led to work with:

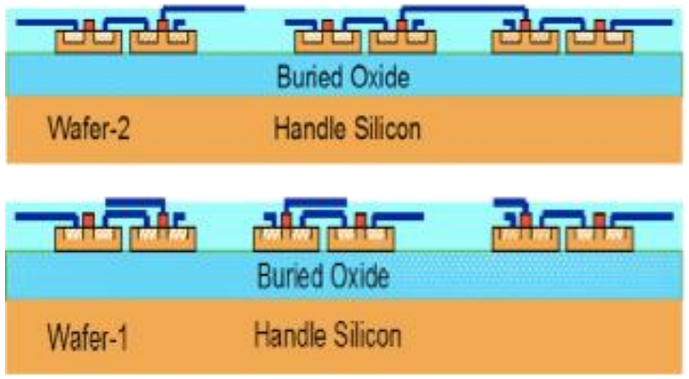
- MIT-LL on SOI based 3D ICs
- Tezzaron on bulk CMOS based 3D ICs
- Ziptronix on detector/sensor integration with oxide bonding
- Cornell on thinning and laser annealing

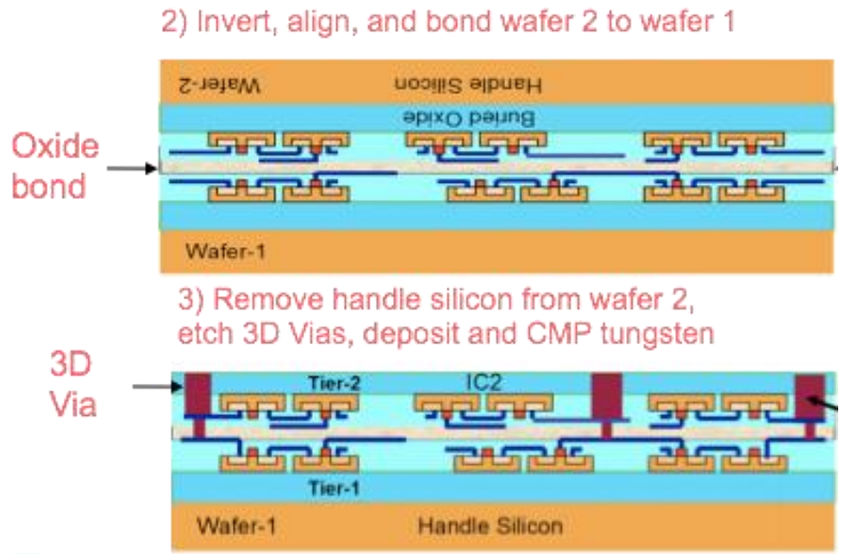
Processes Utilized

Ziptronix Oxide Bonding

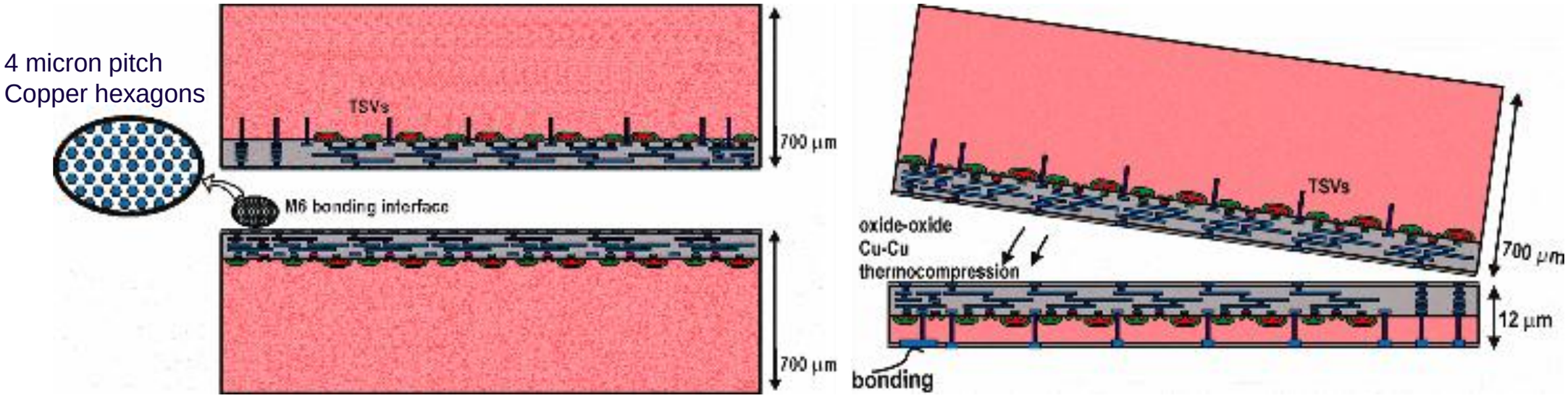


MIT-LL Oxide wafer bonding





Tezzaron cu-cu bonding

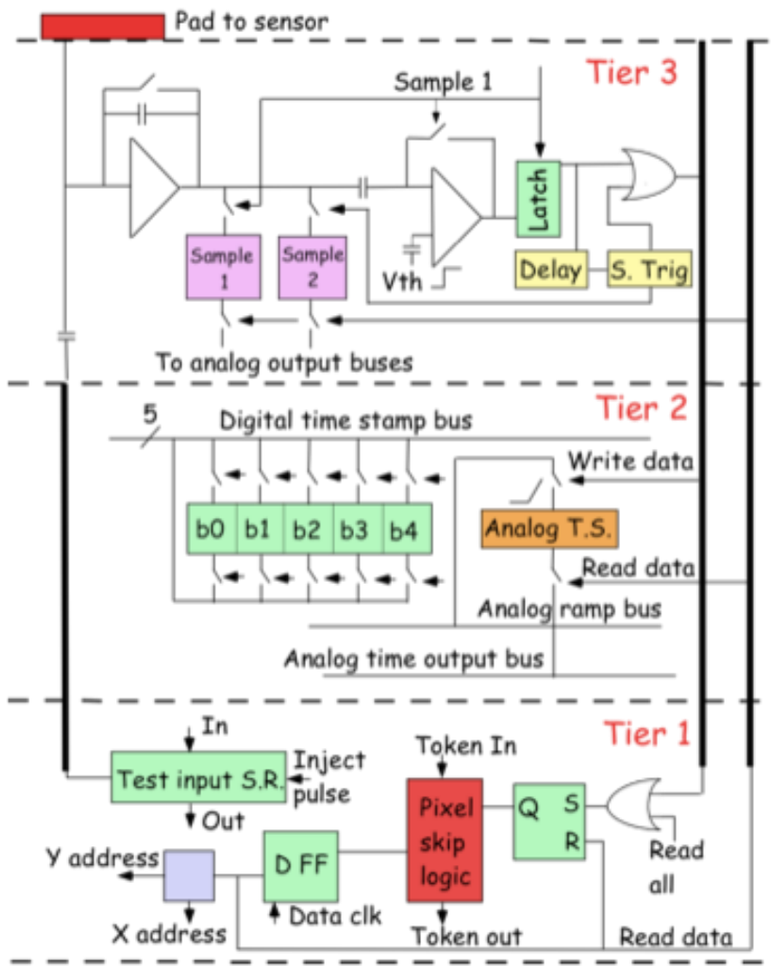


VIP Chip

Chip designed for ILC Vertex

- Low power front end
- Digital and and analog time stamp
- Sparse scan readout
- 20(VIP1), 24(VIP2a) micron pitch

Initial submission had low yield and marginal functionality due to MIT-LL process issues.

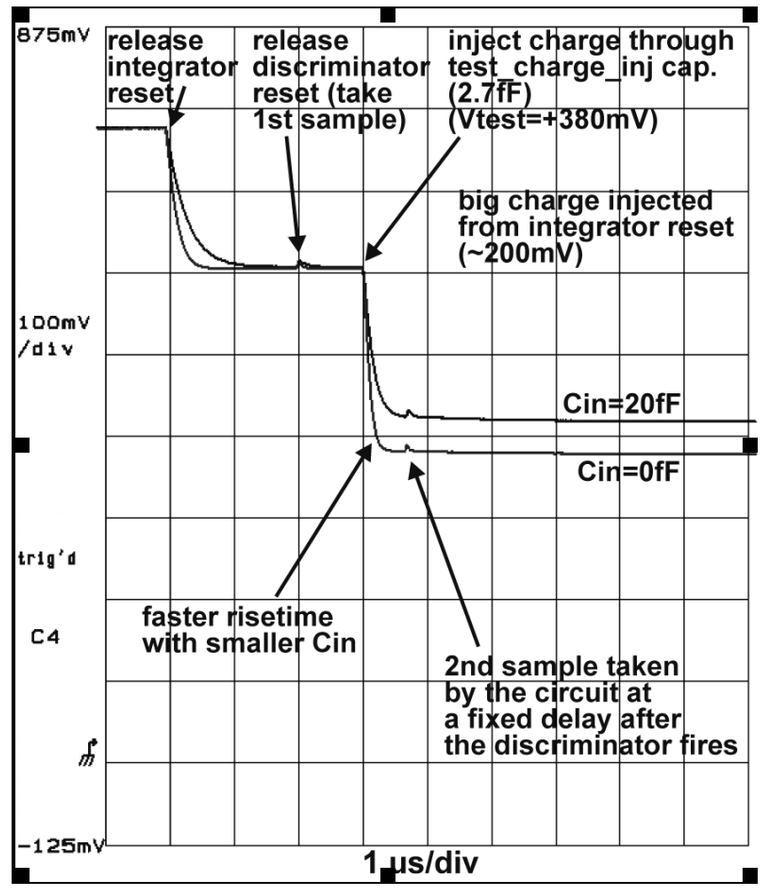


Second submission with a more conservative design worked well. Converted to 0.18 micron CMOS for 3D Tezzaron run VIP2b. Analog performance of the 2D VIP was tested and reported last year.

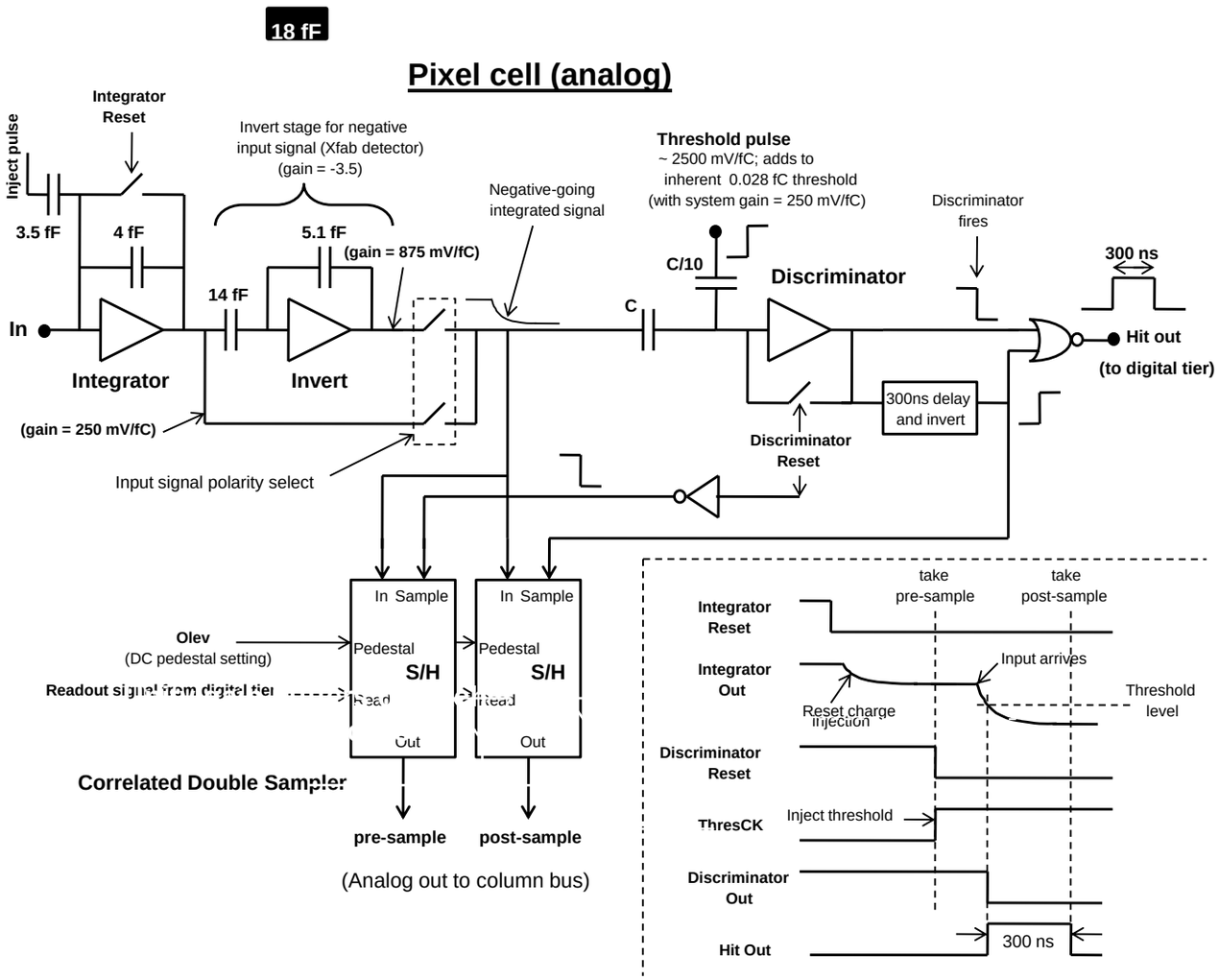
Full 3D VIP2b is received at Fermilab – testing waiting for new IC test system (Spring)

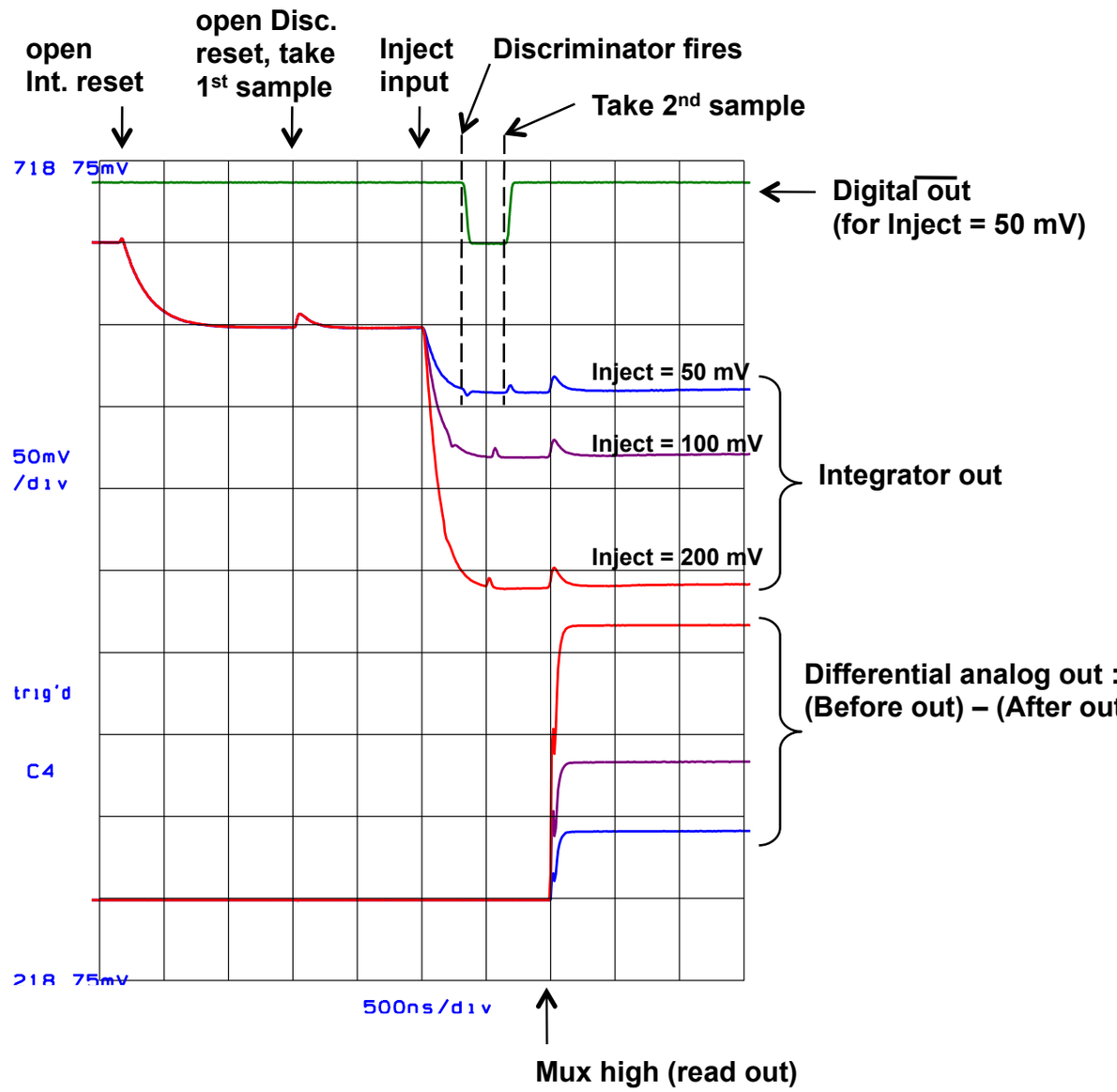
We have tested the VICTR CMS 3D chip and VIPIC X-ray imaging chip – both work!

I will describe these ..



VIP2b tests





Measured response with charge injection

Measured noise (DCS)

Csel	Cin added	Cin + Cinstray	Noise at Inv. Out (mV)	Noise at Inv. Out (e)	Noise at Int. Out (mV)	Noise at Int. Out (e)
111	0	12.5 fF	2.26 mV	16 e	0.74 mV	19 e
110	4 fF	17 fF	2.58	18	0.79	20
101	8	21.5	2.84	20	0.82	21
100	12	26	3.11	22	0.87	22
011	16	30.5	3.38	24	0.93	23
000	28	44	4.09	29	1.04	26

Bandwidth not very sensitive to Cin

Bandwidth varies with Cin

8e + 0.5 e/fF

Measured speed

(T = one RC time constant)

Both sample caps on the output

One sample cap on the output

Csel	Cin added	Cin + Cinstray	T_{before} Int. out	T_{after} Int. out	T_{before} Inv. out	T_{after} Inv. out
111	0	12.5 fF	115 ns	73 ns	135 ns	65 ns
000	28 fF	44 fF	215 ns	125 ns	140 ns	80 ns

At integrator out; speed varies due to varying Csample <u>and</u> varying Cin.

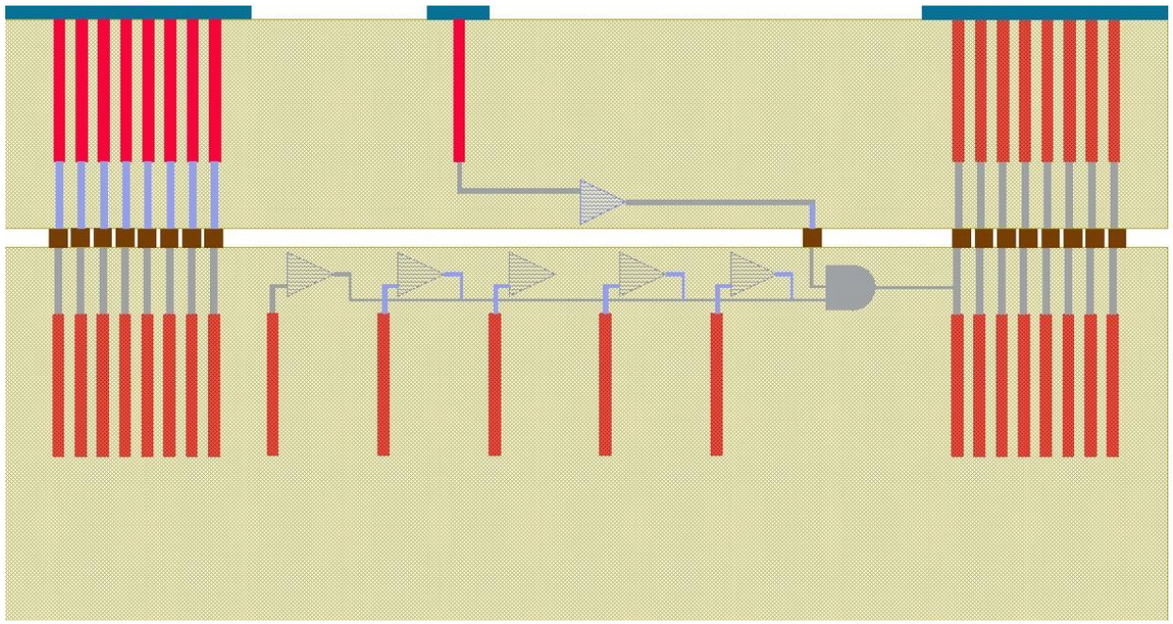
At invert stage out; varying Cin has much less effect on bandwidth.

We will perform testing of the full readout and chip performance in September
Given the good analog performance we have hopes that the chips will be fully operational. We have tested VICTR, on
the same wafer with similar technology.

Measured speed is somewhat slower than simulated – probably due to somewhat lower gm

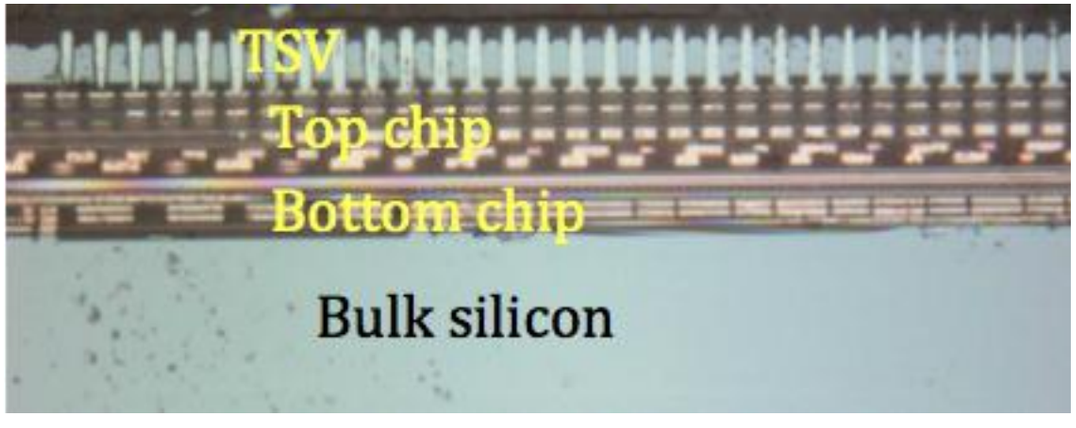
VICTR Chip

(Cornell, Brown)



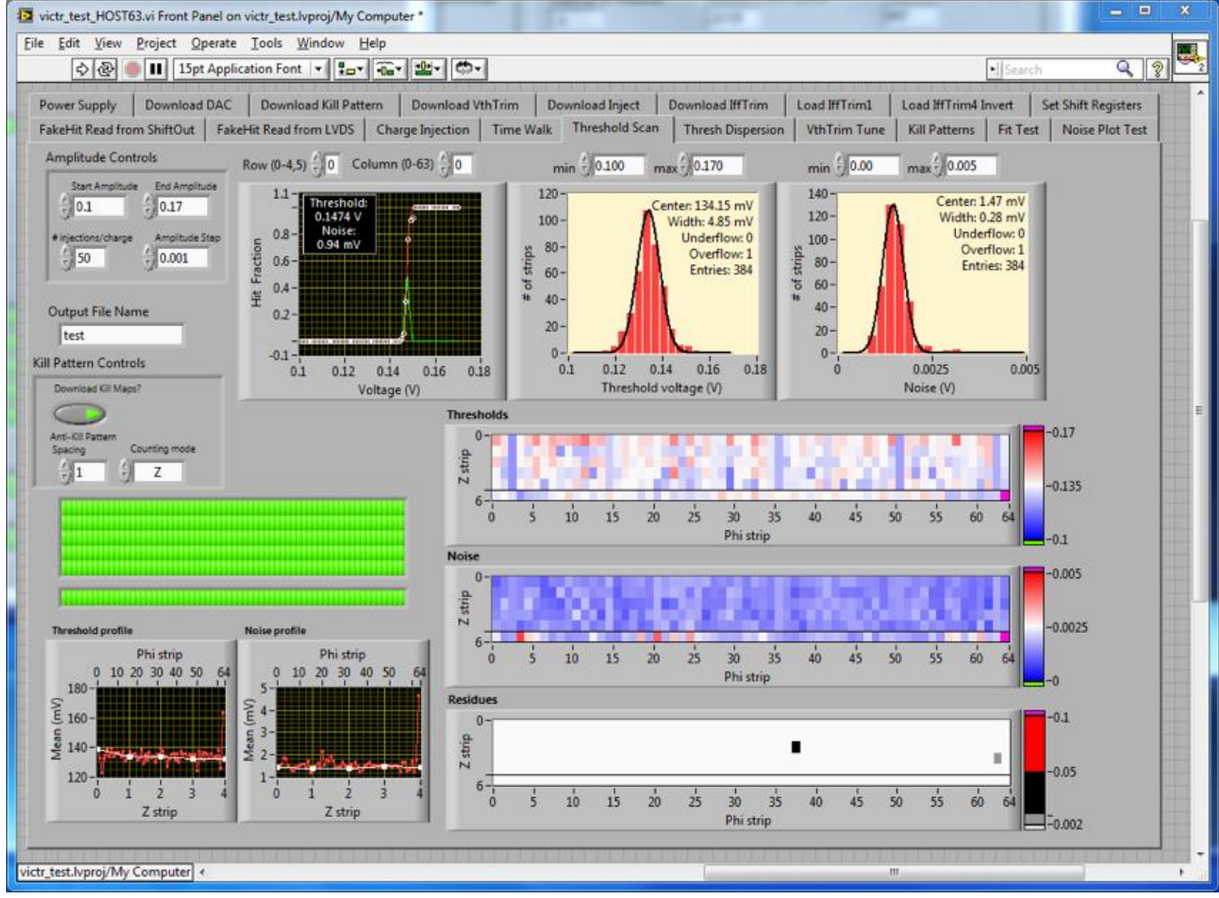
The VICTR chip is designed to demonstrate the principles of a track trigger integrated sensor/ROIC

- **Part of Fermilab 3DIC run**
- **Modified FEI4 (Atlas) front end**
- **First chips delivered last Sept had alignment problems but other processes worked well.**
  - **backside thinning**
  - **TSV contact**
  - **Backside metalization**
- **We now have well-aligned functioning chips from wafers delivered in June Communication of hits from top to bottom tier on all channels**
  - **Detailed testing of several chips in progress**
  - **9/11 functional after visual inspection**
  - **Now being bonded to sensors**
- **18 "recovery" wafers received at Tezzaron**



VICTR Test results

See top and bottom tier fast and slow outputs as well as coincidences between tiers – indicates good 3D bonding



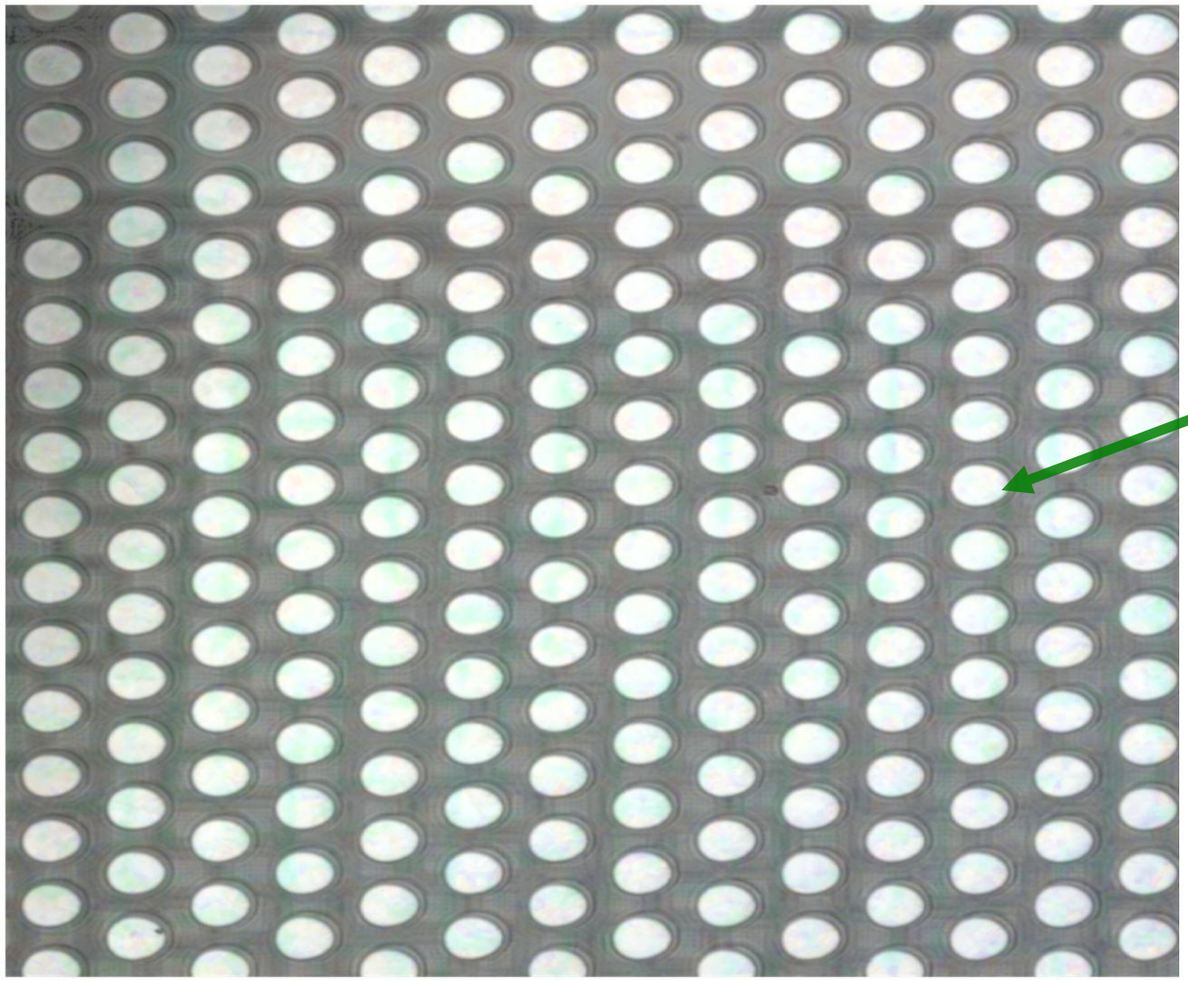
Test scans

Short strip tier

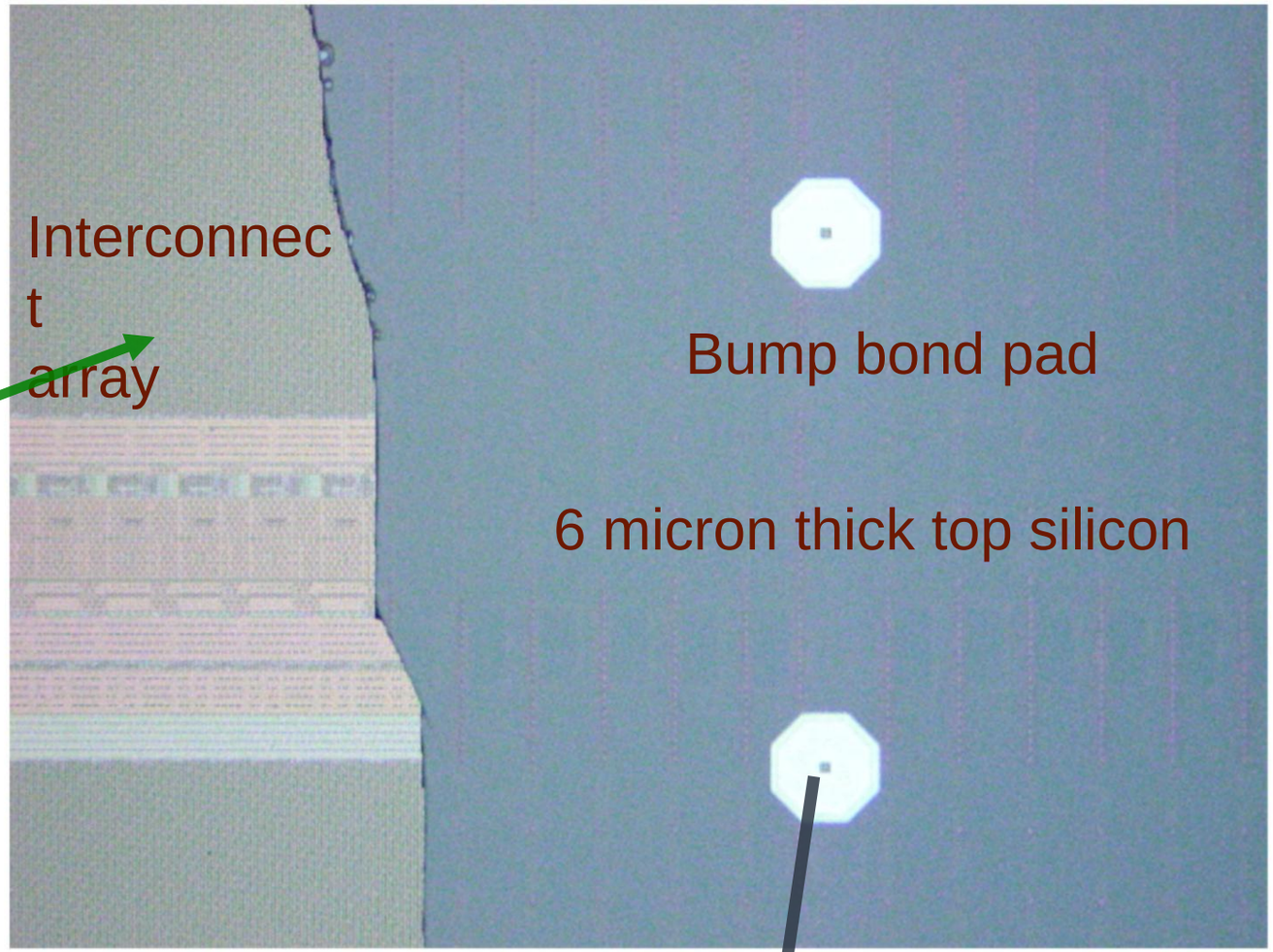
Long strip tier

Coincidence

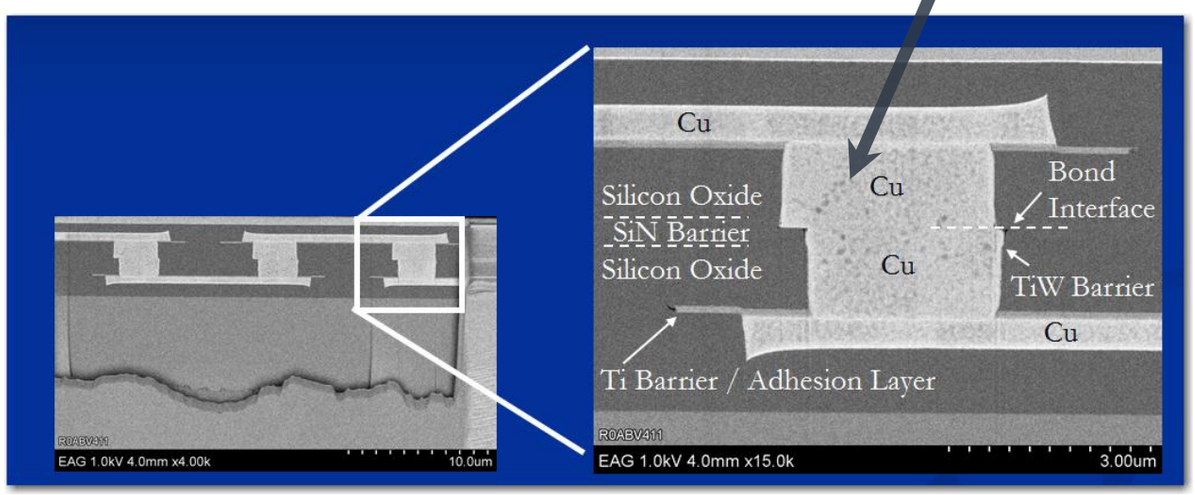
Test Results

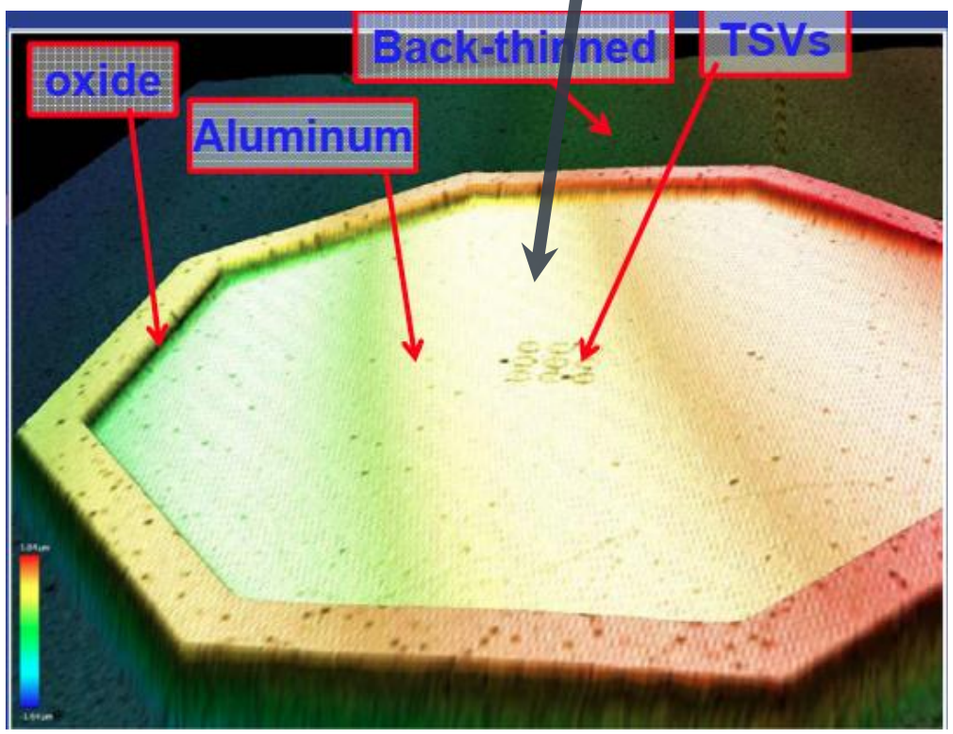


4 micron pitch



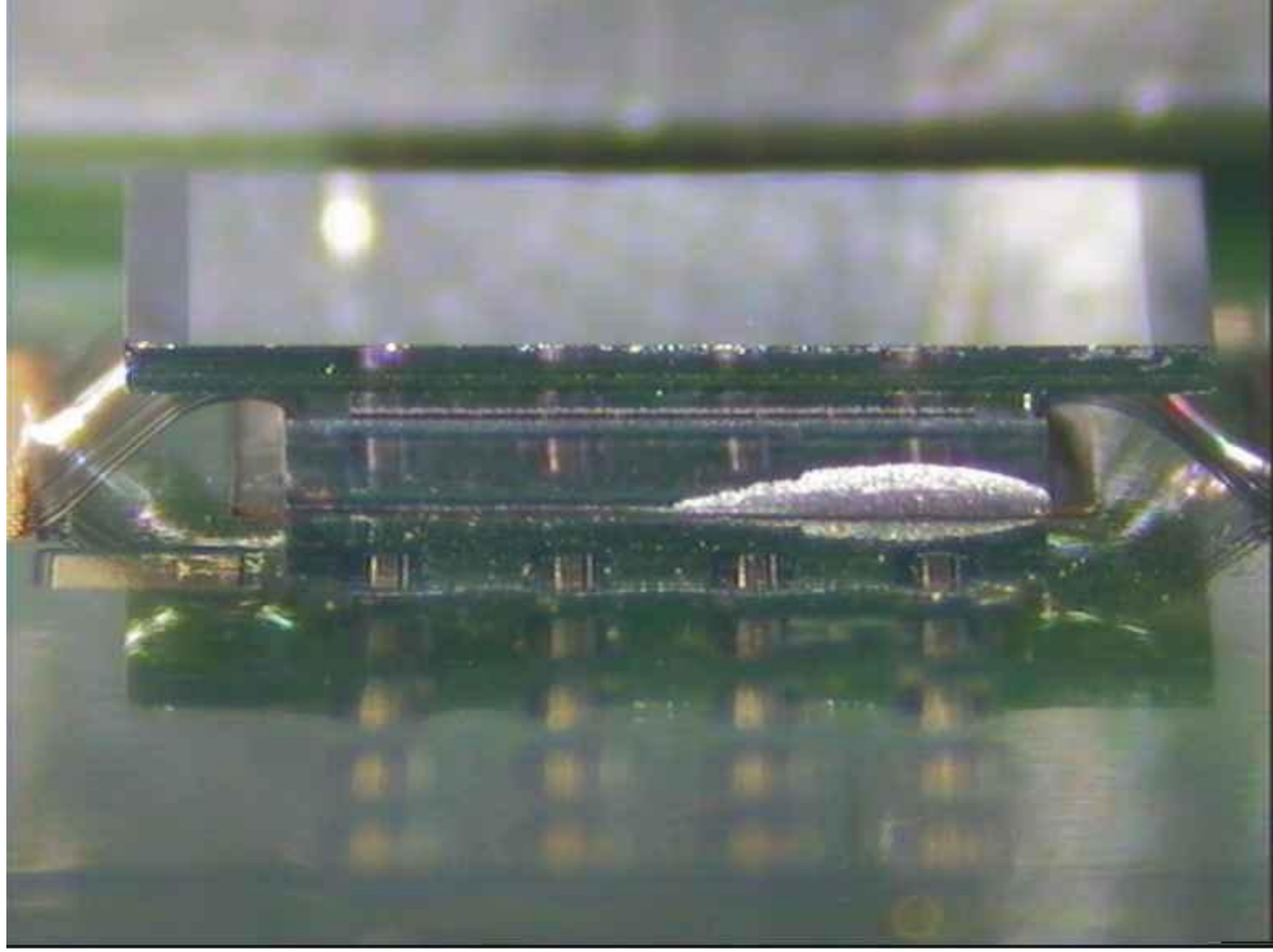
DBI Copper pillars





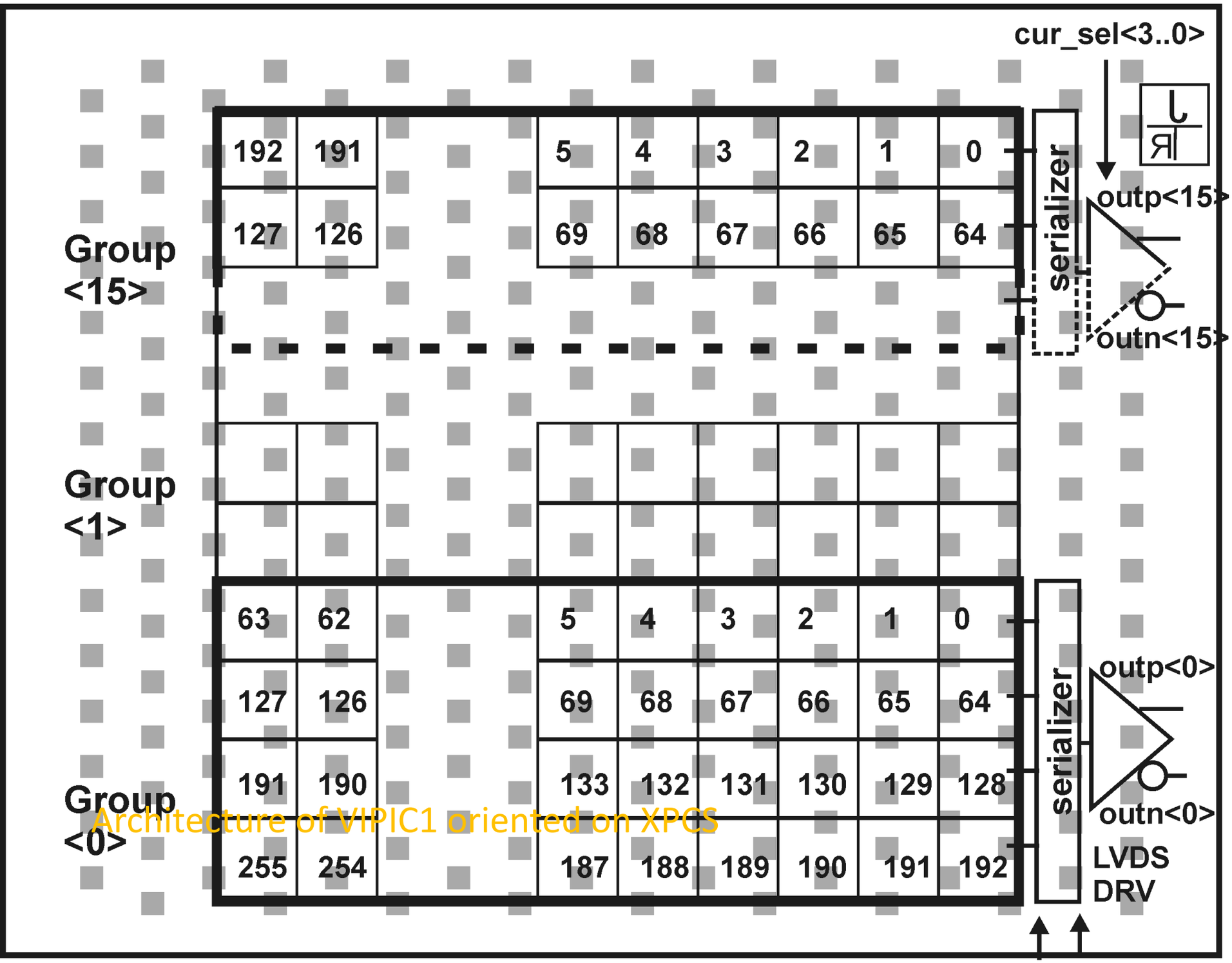
Sensor Bonding

a



VIPIC Chip

Designed for x-ray correlation spectroscopy



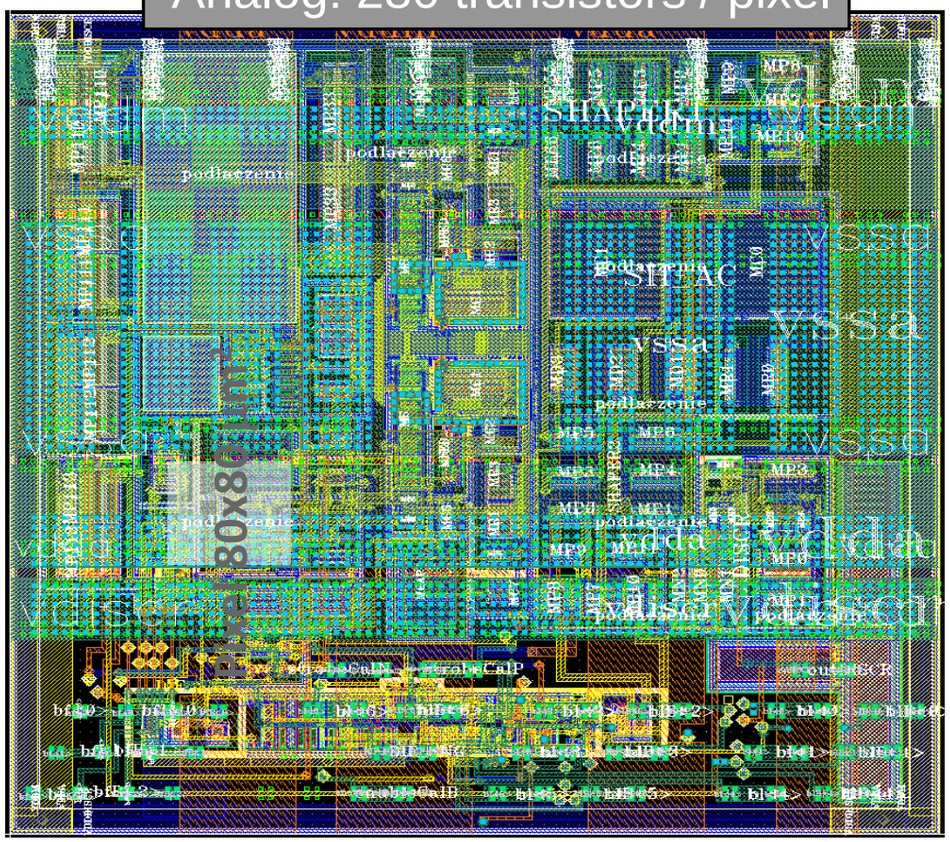
Top view - bump bonding pads on the back of the digital tier

How it works:

- Continuously, in dead-time-less way outputs hits on 16 parallel outputs from 64×64 matrix of pixels using priority encoder based sparsification method
- 5 bit long content of pixel counters followed by 8 bit long address of hit pixel
- Die size: 5.5×6.3mm^2

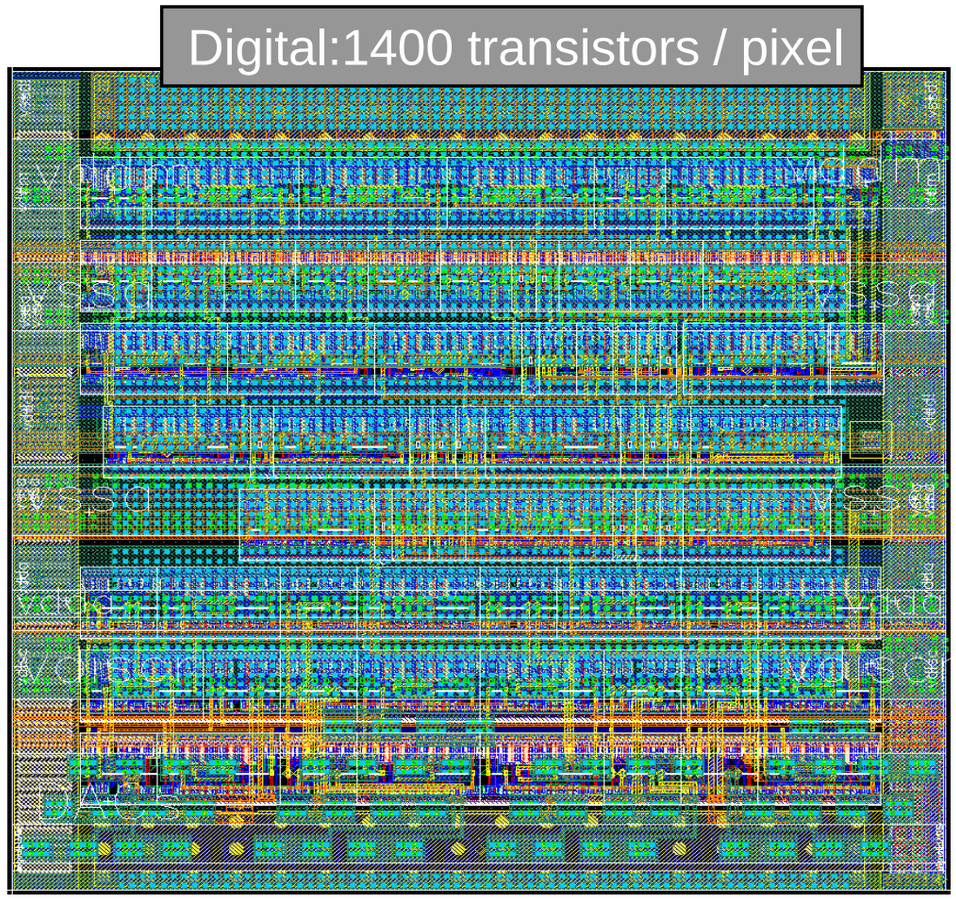
VIPIC 1: Pixel architecture and layouts

Analog: 280 transistors / pixel



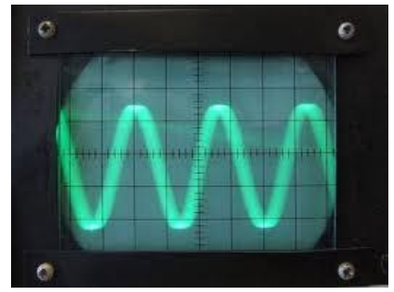
- Pseudo-differential CSA-shaping filter-discriminator
- shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <150 e^- ENC, optimized for 8 keV
- 12 bit/pixel DAC adjustments
-

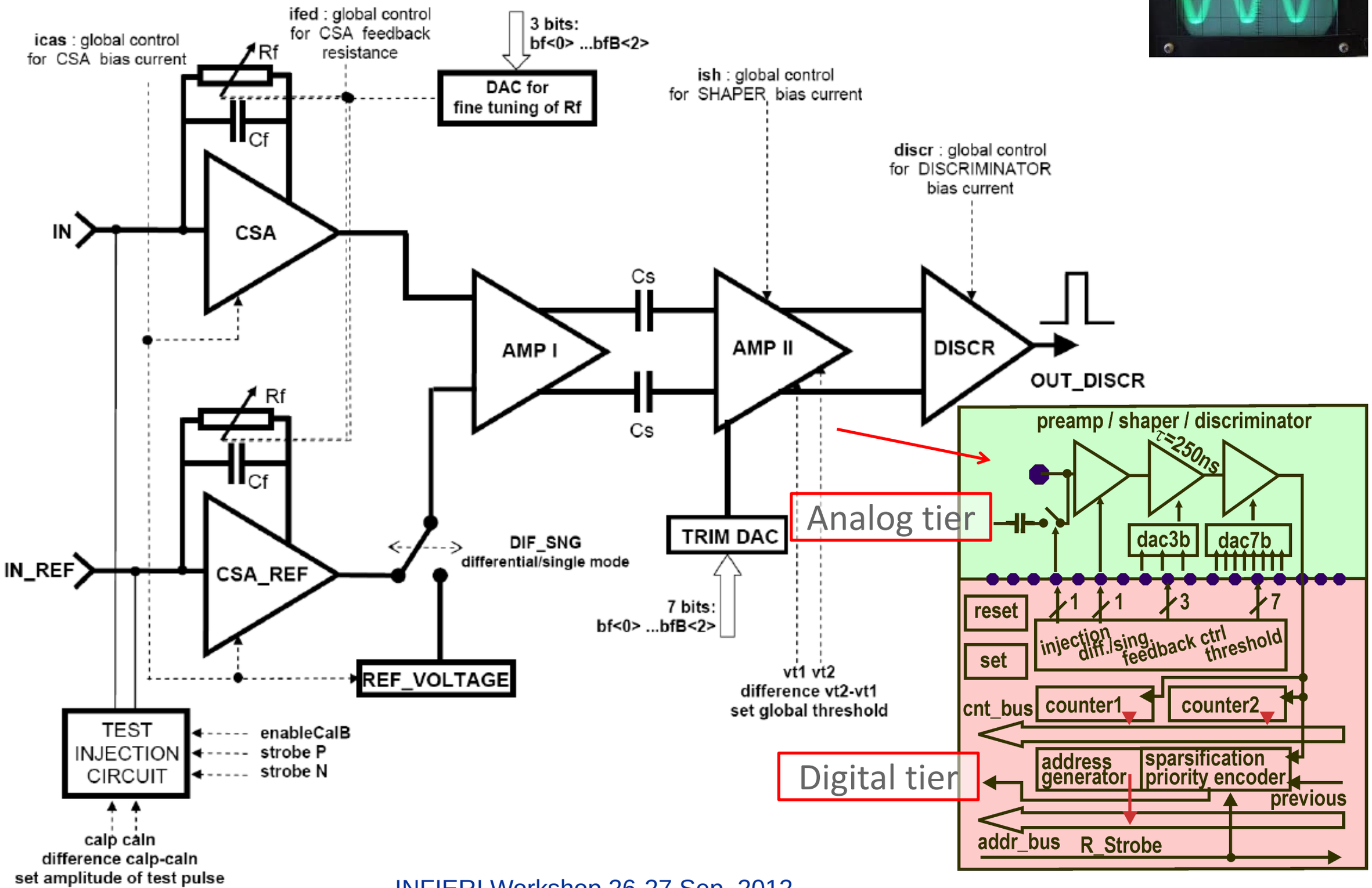
Digital:1400 transistors / pixel



- 2 dead-time-less modes:
  - timed readout address and hit count σ_t=~ 10μs
  - imaging – counting of events
- 2 5 bit-long counters / pixel *(counting limited by duration of analog signals)*, RO with sparsification but clamping addresses: $t_{read}= (f_{clk})^{-1} \times (3+5)$ bits $\times 4 \times 64$<20μs
- 'Set' + 'Kill' bits/pixel

VIPIC 1: Pixel analog details



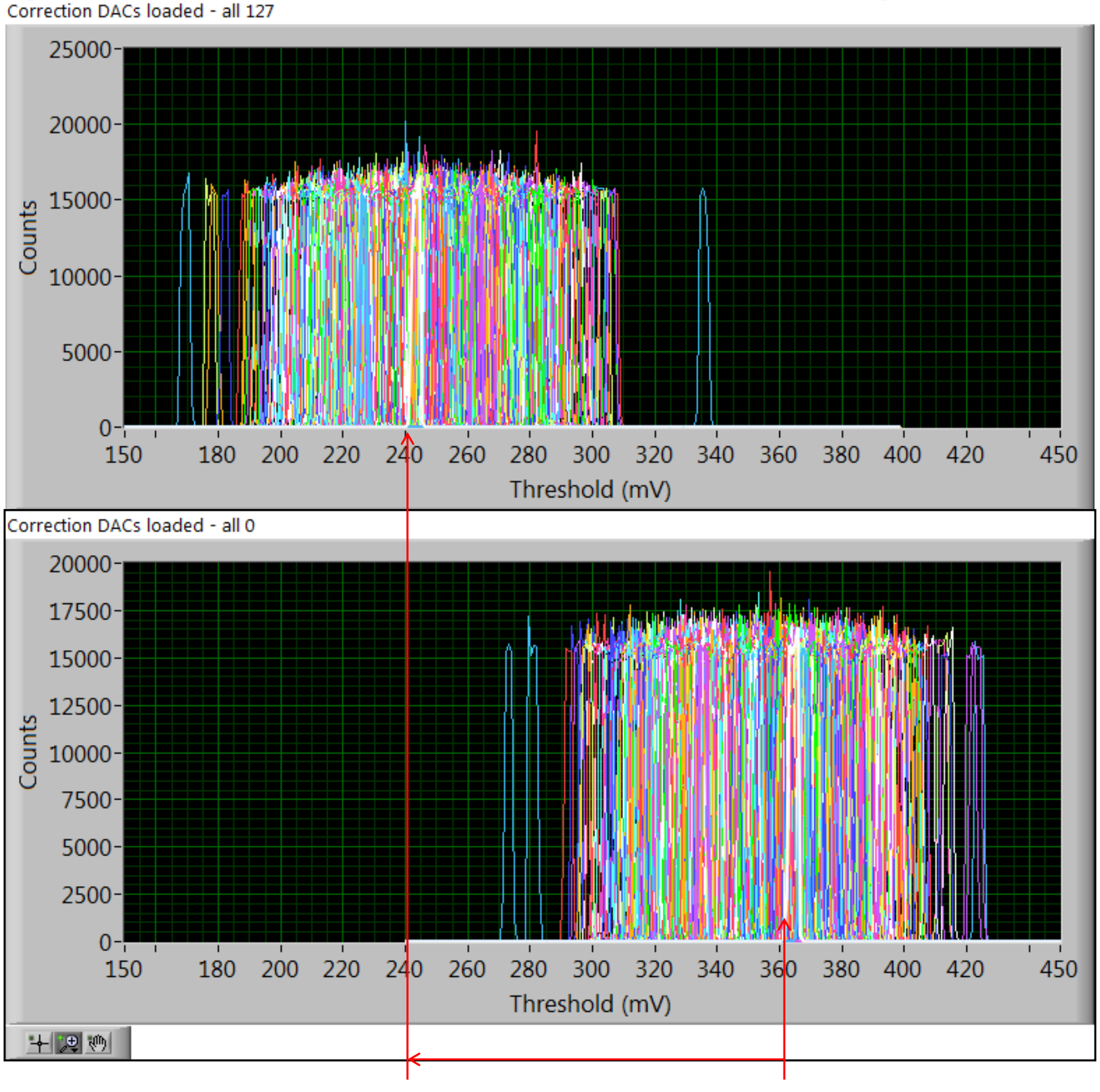


VIPIC 1 (communication between tiers)

two unambiguously resolving groups resulted from noise hits at extreme DAC settings

All pixels respond

Communication between tiers does not show any misses. Of the 25 connections/pixel between tiers, 19 appear to be working and 6 haven't been tested yet (77,824 total)

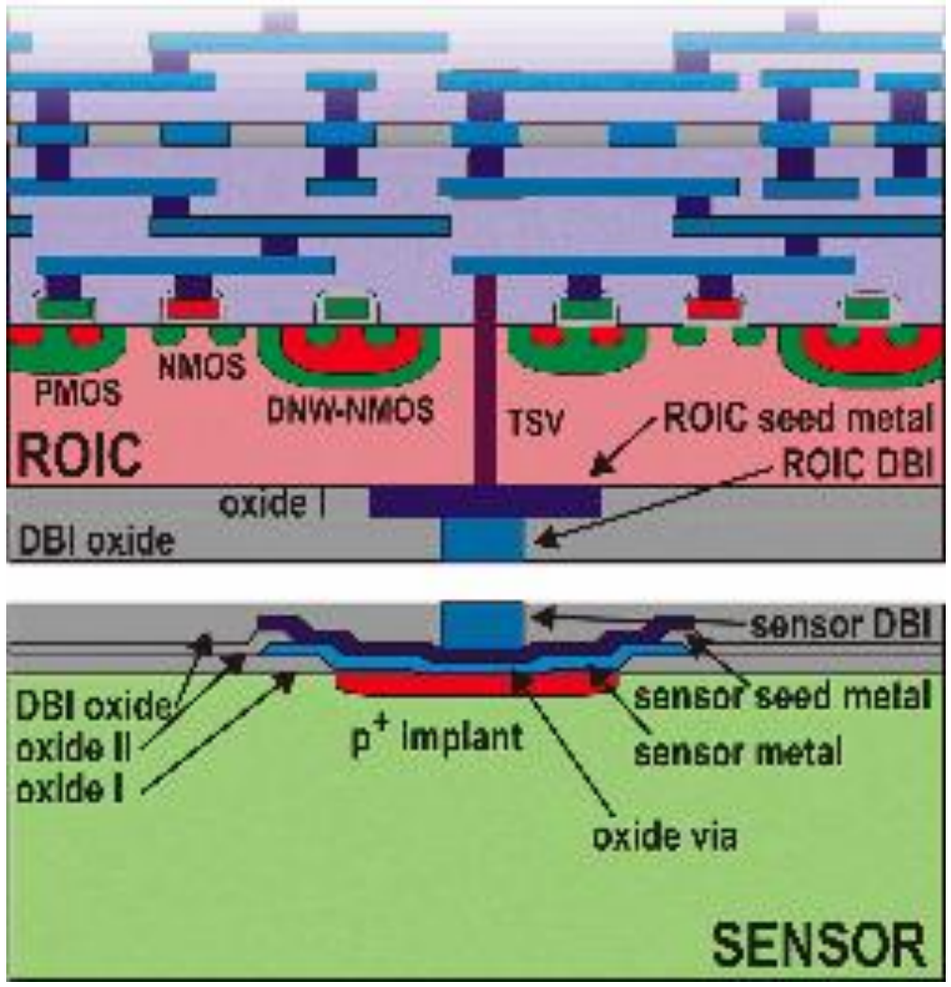


Oxide Bonding

In our studies the most promising fine pitch bonding technology was (and is) the direct bond interconnect (DBI) process from Ziptronix

- No bump bonds -
- Very fine pitch - 4 microns used for 3D Tezzaron wafers
- Mechanical strength enables aggressive post-bond thinning
- Uses standard IC processes - CMP and metalization
- Can withstand high temp.

In principal can be low cost

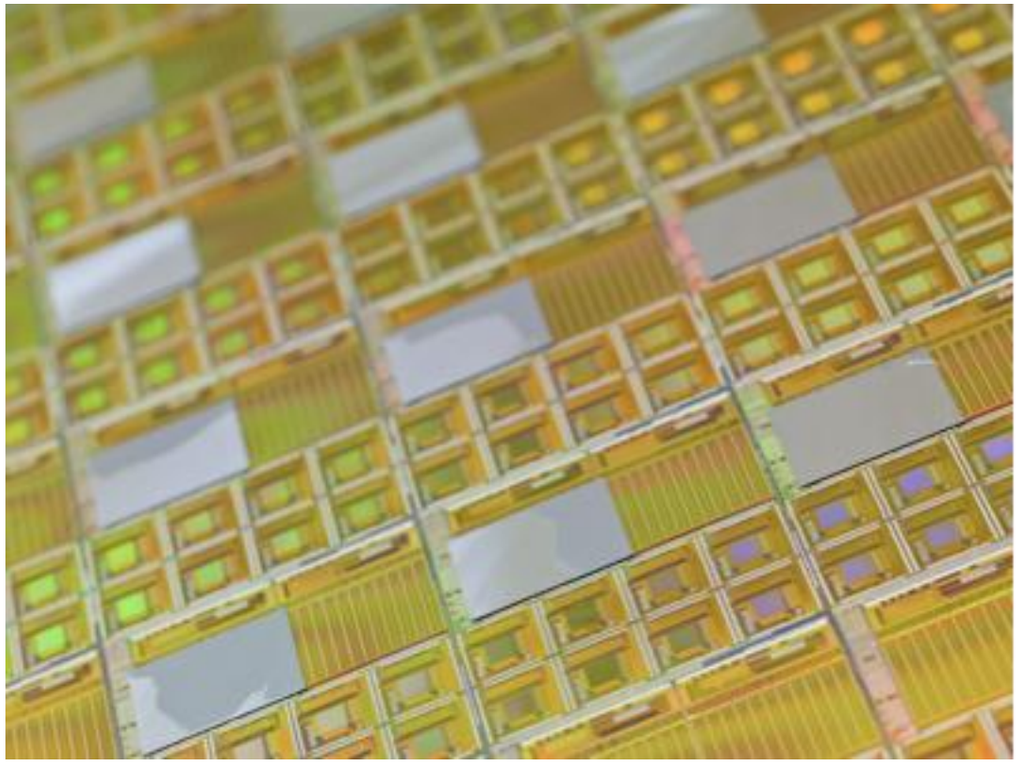


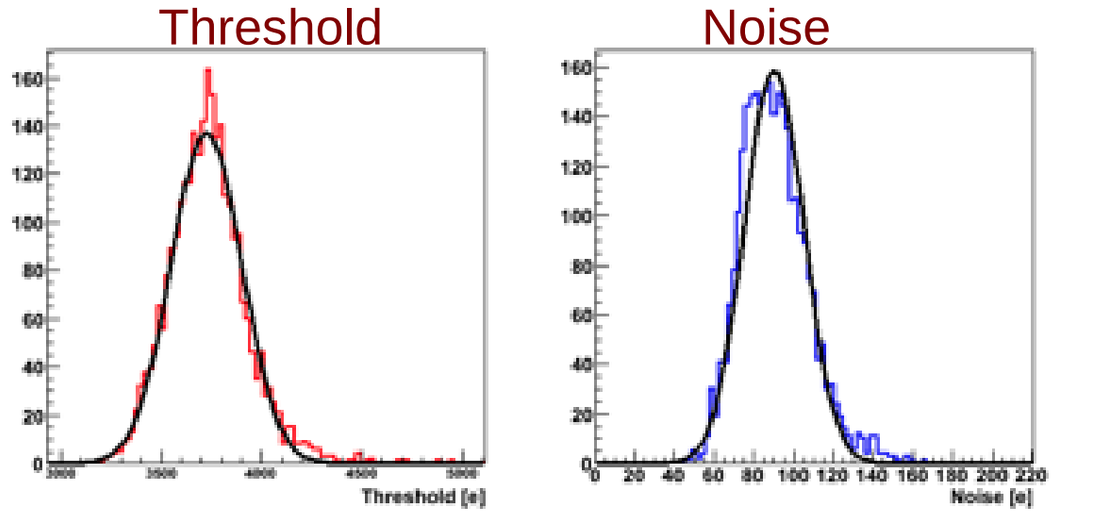
Oxide Bond Testing

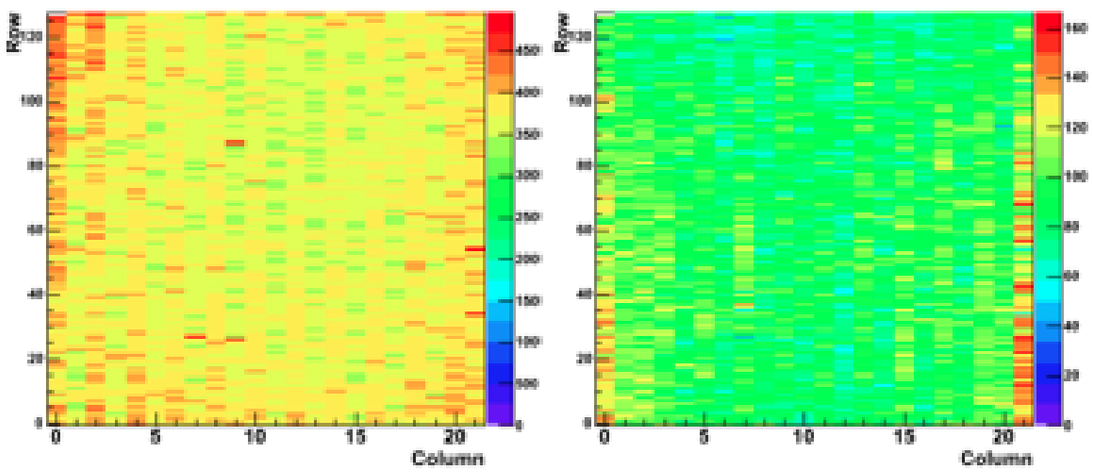
Initial work was based on existing ROIC wafers from BTeV and sensor wafers from MIT-LL.

- Sensor chip to FPIX wafer bond
- Sensors ground to 100 microns - 8 V depletion
- 100% connectivity on sensors without obvious bond voids
- No degradation in s/n
- Radiation hard to >10 MRad

Process used for 3D wafers (iphone camera), planned for track trigger, active edge, x-ray imaging work

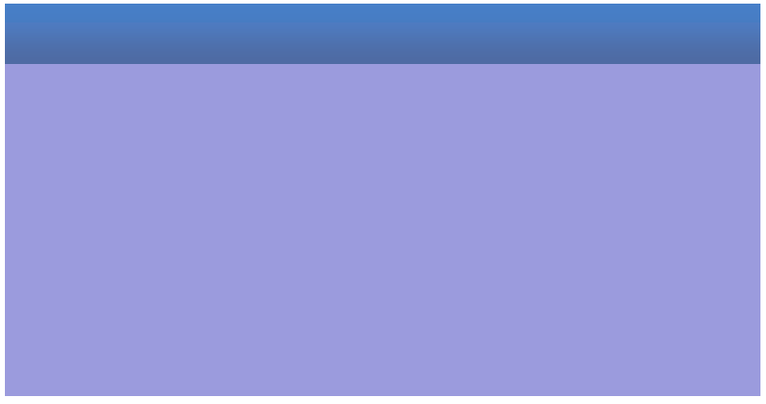






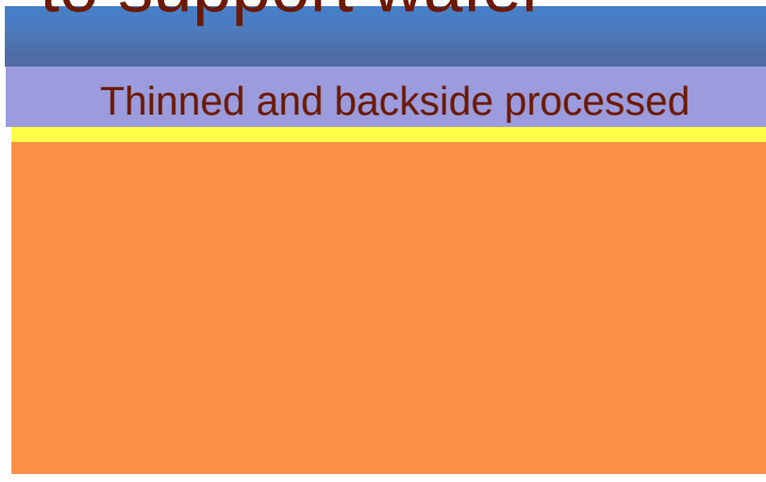
Thinning Alternatives

Bulk CMOS/SOI
bonded to sensor

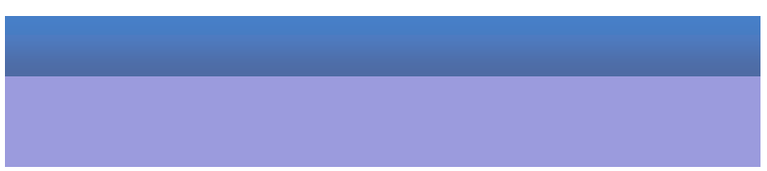


CMOS MAPS
epitaxial layer

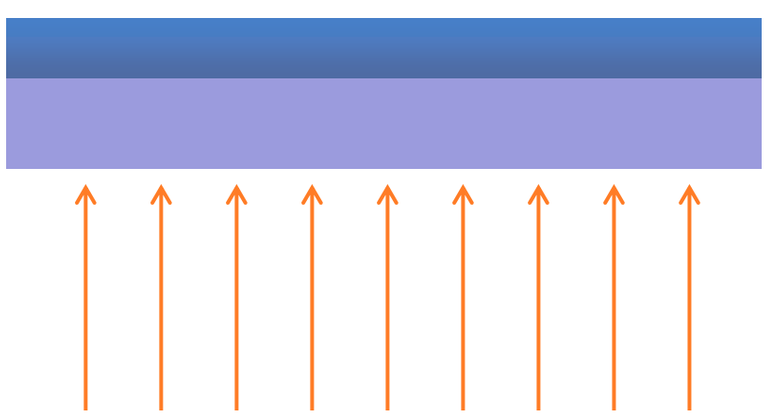
Sensor oxide
bonded
to support wafer



Backgrind

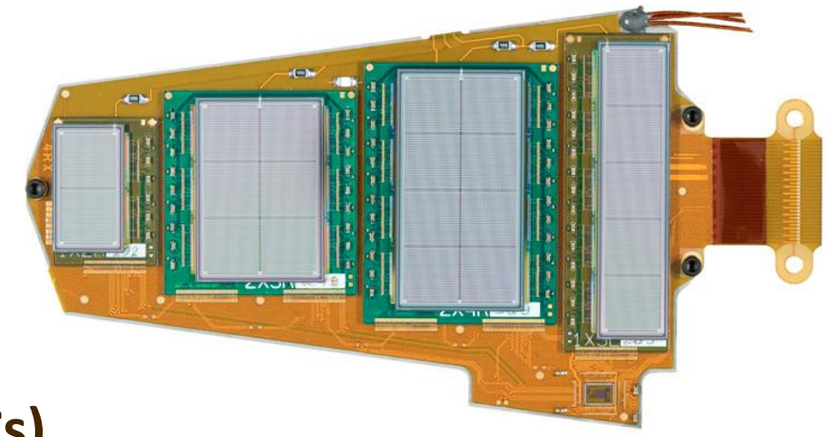


Polish, implant and
Laser anneal



Etch backside silicon

Large Area Array Development



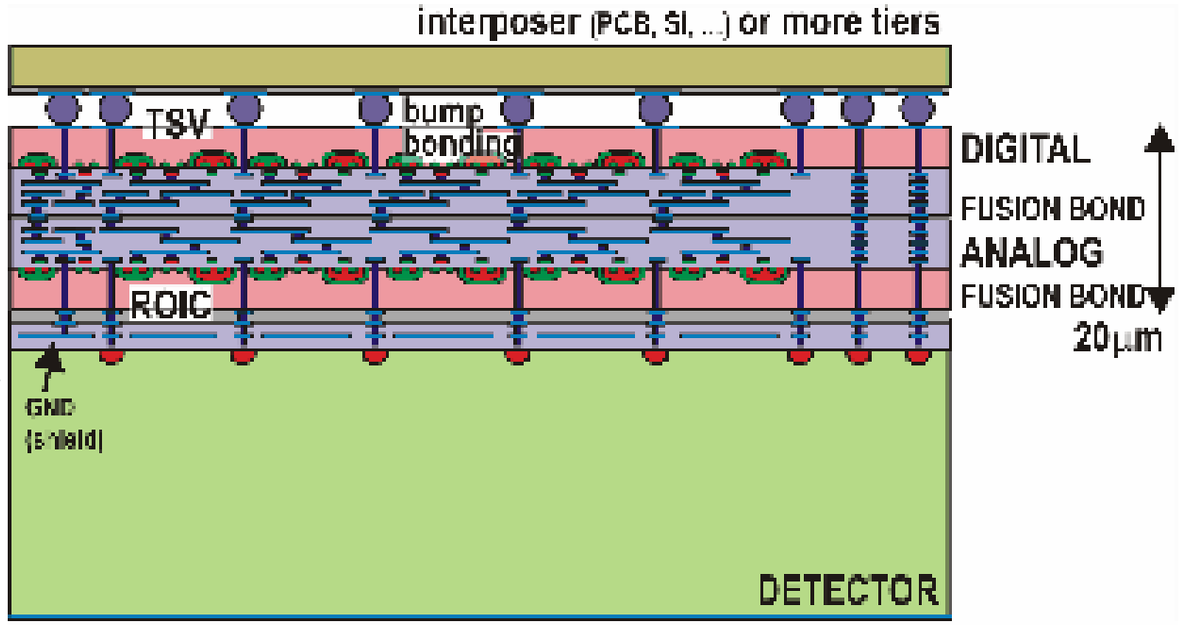
The Problem: Build large area arrays of highly pixelated detectors with minimal dead area and reasonable cost

Current pixel detectors have dead areas arising from:

- **Sensor Edges**
- **Wirebond connections for Readout Integrated Circuits (ROICs)**

A reticule-based sensor/readout has instrinsic size limitation of ~2x2 cm

- **3D #2 - 3D or vertically integrated electronics provides a backside path for extraction of signals**
- **3D #1 - Active edge sensors remove dead area at the edges**



Combine active edge technology with 3D electronics and oxide bonding with through-silicon vias to produce fully active tiles.

- **These tiles can be used to build large area pixelated arrays with good yield and reasonable cost**
- **Tiles can populate SiD forward disks with optimal tiling and low dead area**
- **Only bump bonds are large pitch backside interconnects**
- **The density and geometrical flexibility means this is exactly what is needed for forward disks at SiD**

Costs and Yields

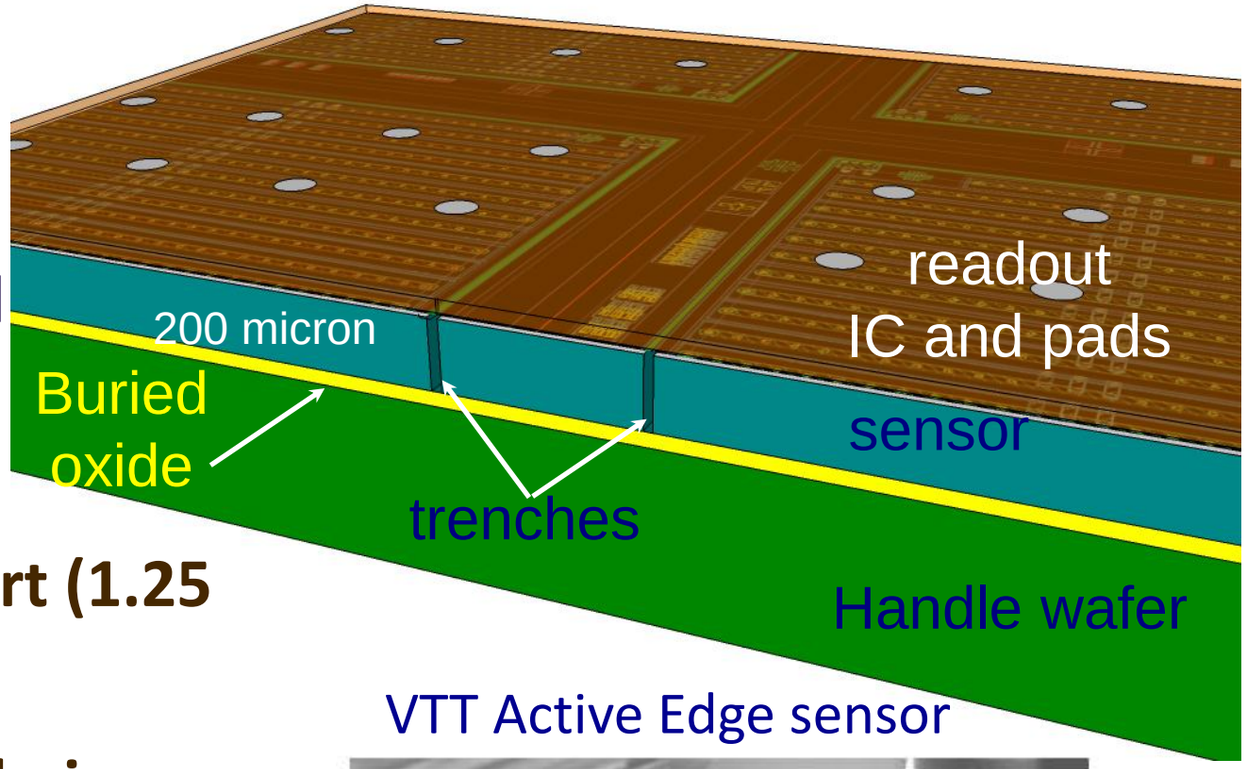
Component	Current or projected cost	Yield	Comment
Readout IC	\$8/cm^2[6]	65-70% [7]	Current 3D wafers and FEI4 prototype yield
Active Edge Sensors	\$53/cm^2	-	Current cost for prototype 150 mm wafers
Silicon Strip Sensors	\$10/cm^2	100%	CMS tracker costs
Bump bonding	\$213/cm^2	98%[8]	CMS forward pixel costs (2007) Yield ≡<20 bad bumps/chip
DBI bonding	\$0.04/cm^2	90%	Projected by Yole Development [9] for high volume production
Target Costs (2020s)	\$10/cm^2	90%	Assuming 200 mm sensor wafers and batch active edge process

Current and projected costs and yields for sensor/readout integration technologies

Active Edge Project

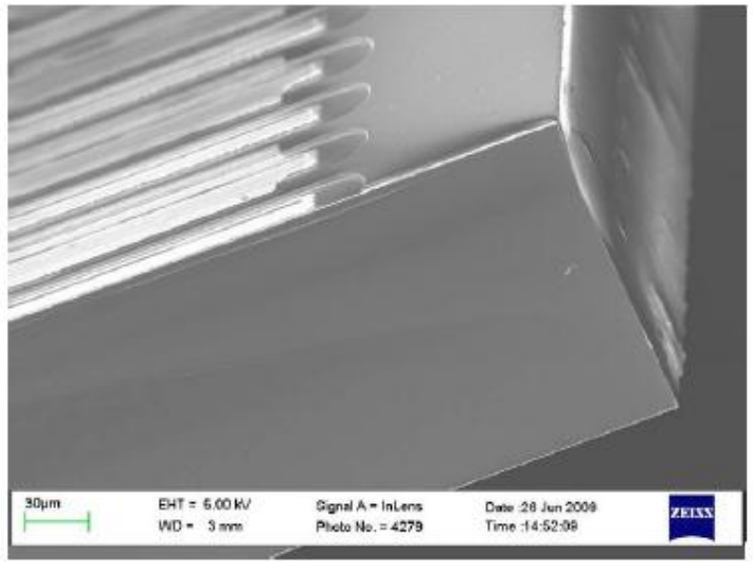
(Cornell, SLAC, Hawaii, Brown, UCSC, NRL)

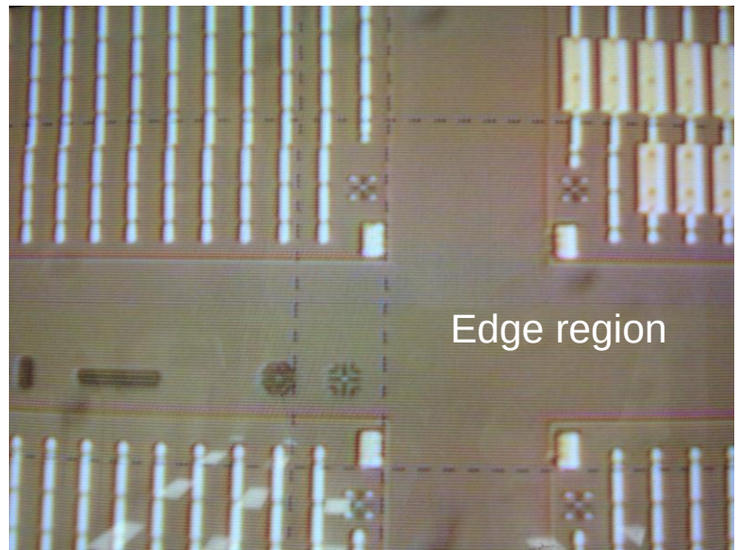
We are building a demonstration array including active edge sensors, oxide bonded wafers, dummy readout wafers



- **Sensors match the geometry envisioned for CMS track trigger long (1 cm) and short (1.25 mm) strip sensors.**
- **Top tungsten plug "damascene" wafer is being fabricated at Cornell - designed to readout either long or short strips with single reticule.**
- **Wafer bonding top thinning and etch and interconnect at Ziptronix**
- **Singulation and handle wafer removal will be done at**
  Stanford in collaboration with SLAC
- **There are no trenches on the edge reticules to allow test of the UCSC/NRL "slim edge"process**

VTT Active Edge sensor





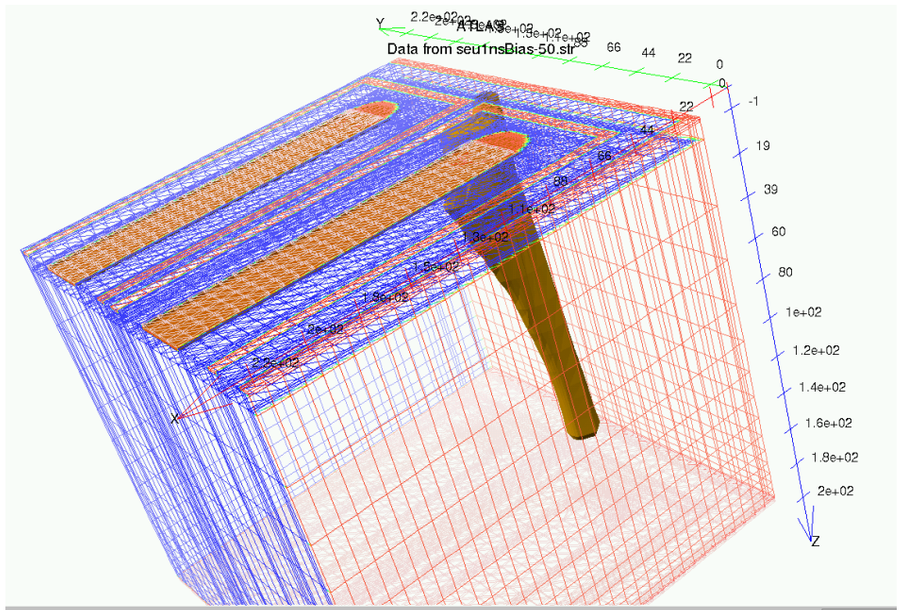
VTT wafers received. Cornell process has had issues with tungsten adhesion.

Active Edge Wafer Tests

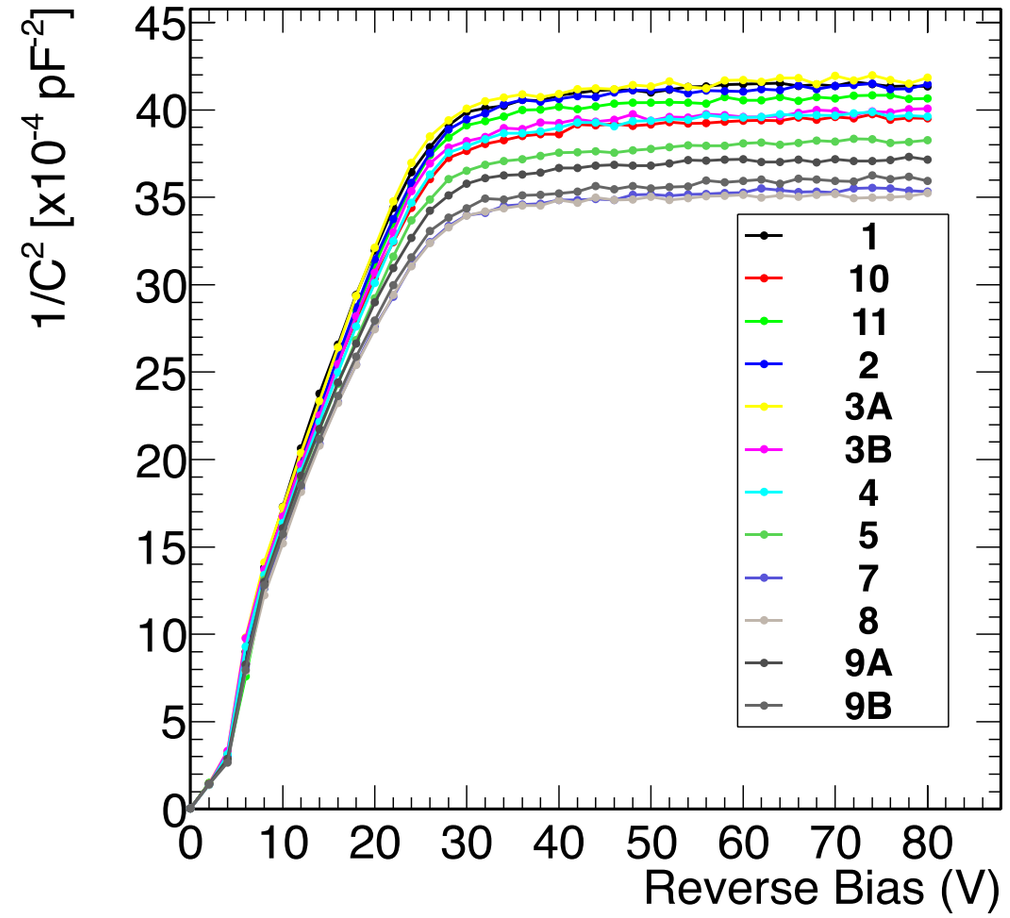
One wafer was processed with top metal for testing – others will be wafer bonded.

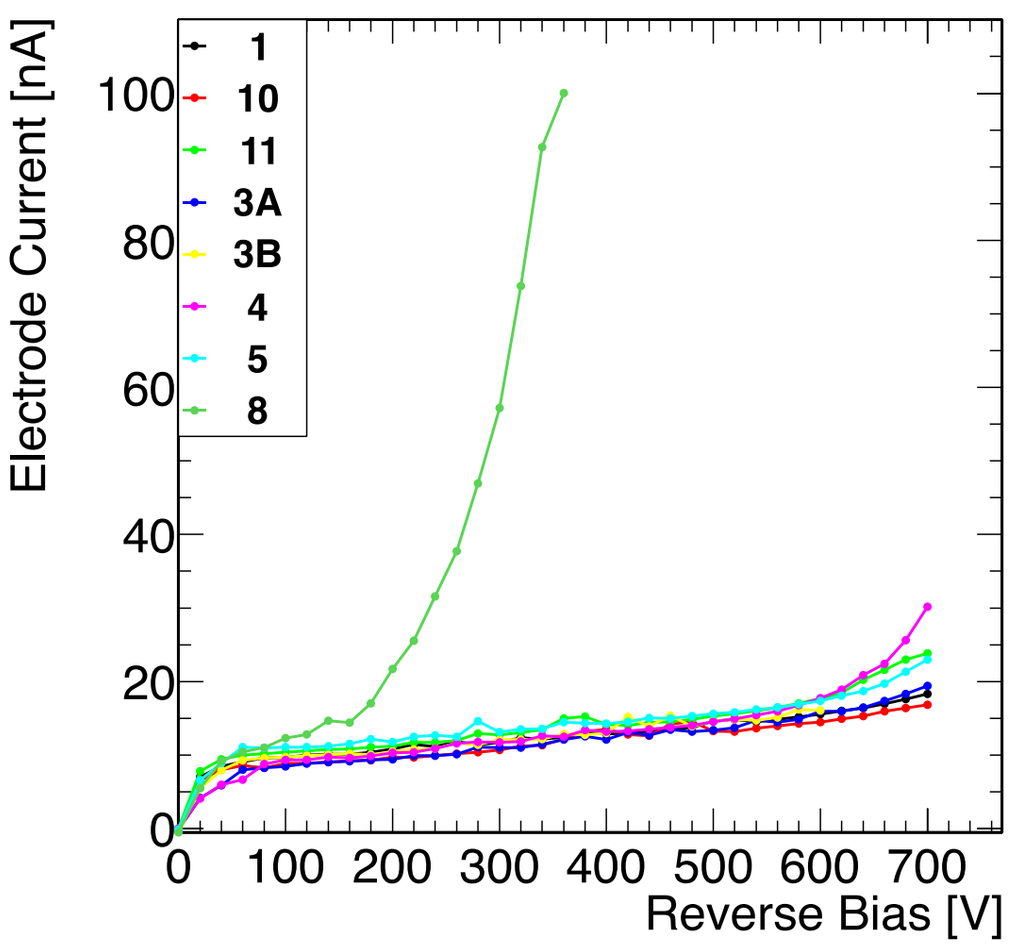
Test Structure results:

- Depletion around 30 V
- Some have early breakdown but most break down beyond 700 V

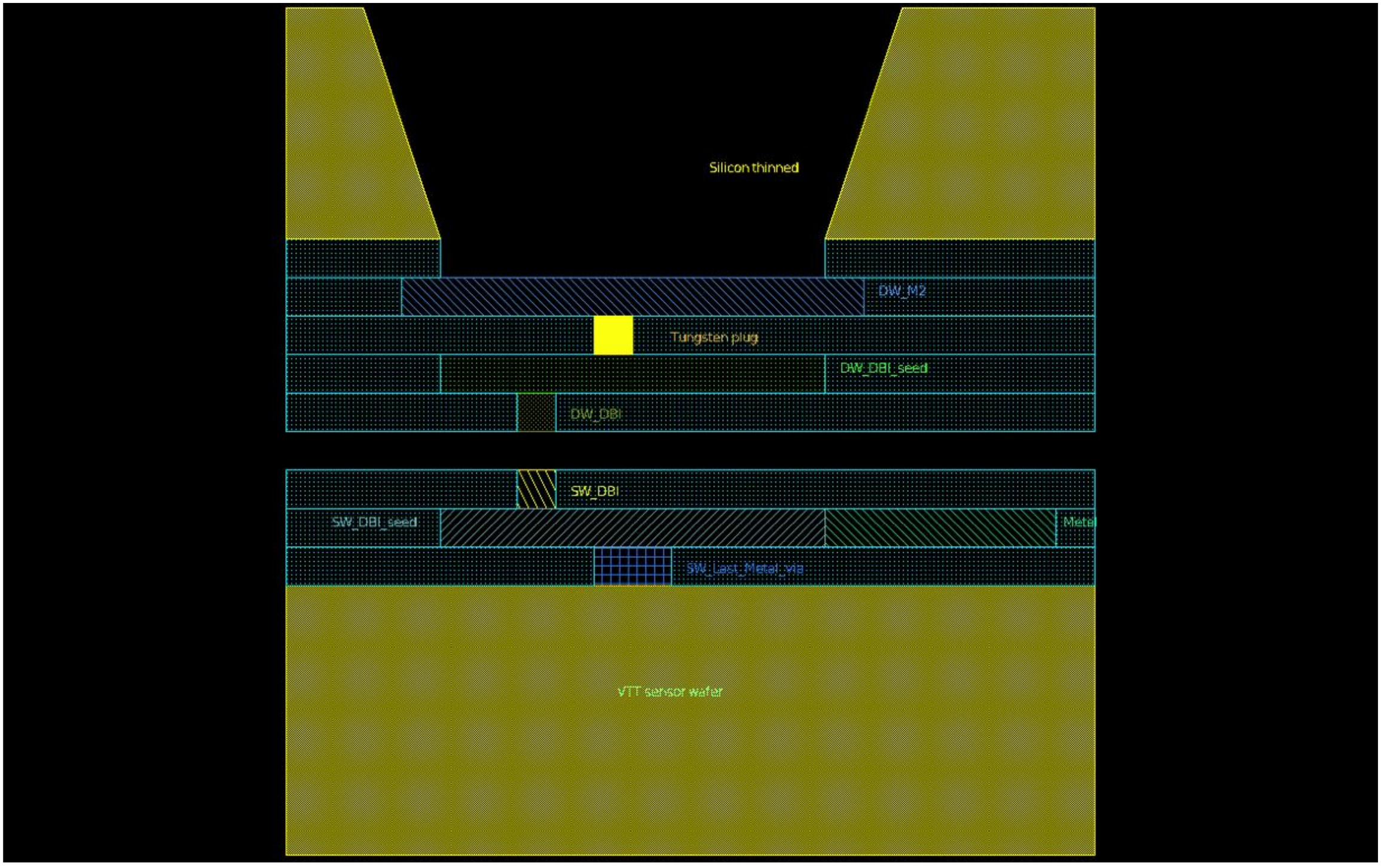


Simulation of charge density due to 3.5GeV muon hitting near the edge- study charge collection and edge effects.





Layer Stack


Silicon thinned
DW_M2
Tungsten plug
DW_DBI_seed
DW_DBI
SW_DBI
SW_DBI_seed
SW_Last_Metal_via
VTT sensor wafer

Basic Parameters

The variety of inner radii is awkward, requiring many reticule designs

Barrel	R		
Layer 1	14		
Layer 2	22		
Layer 3	35		
Layer 4	48		
Layer 5	60		

Disk	R_{inner}	R_{outer}	z_{center}
Disk 1	14	71	72
Disk 2	16	71	92
Disk 3	18	71	123
Disk 4	20	71	172

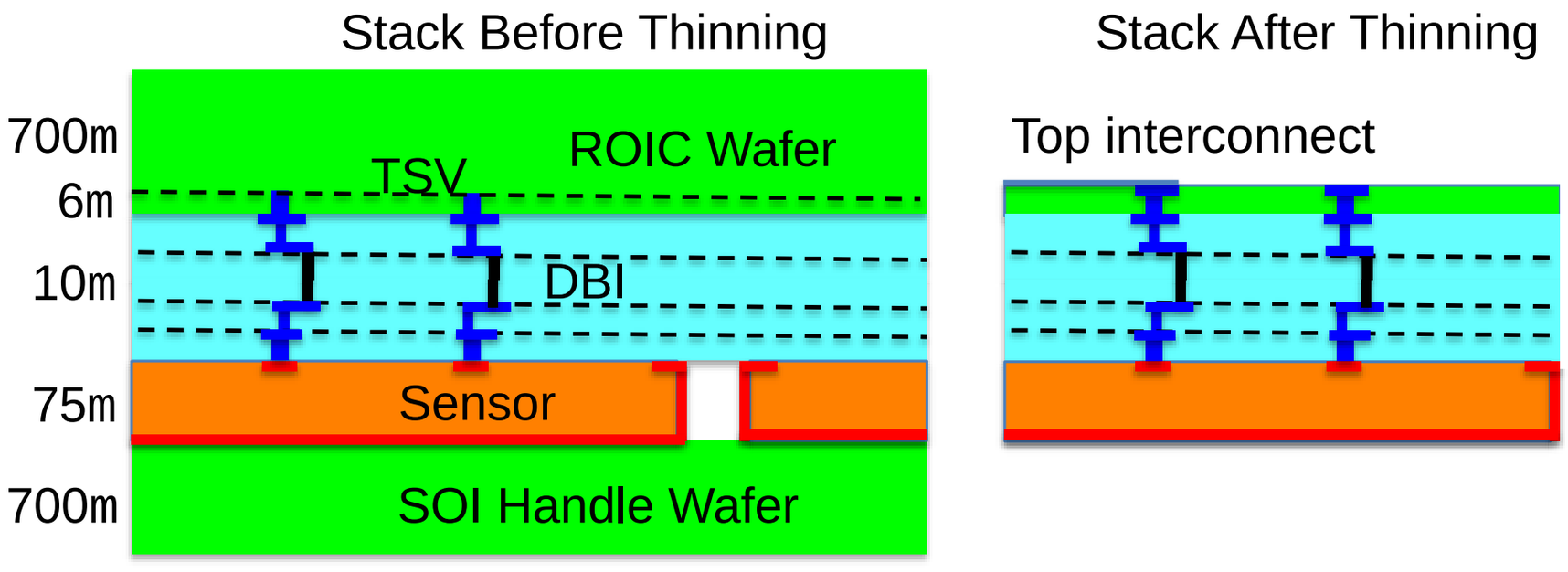
Forward Disk	R_{inner}	R_{outer}	z_{center}
Disk 1	28	166	207
Disk 2	76	166	541
Disk 3	117	166	832

This is OK (later Slide)

Tiling

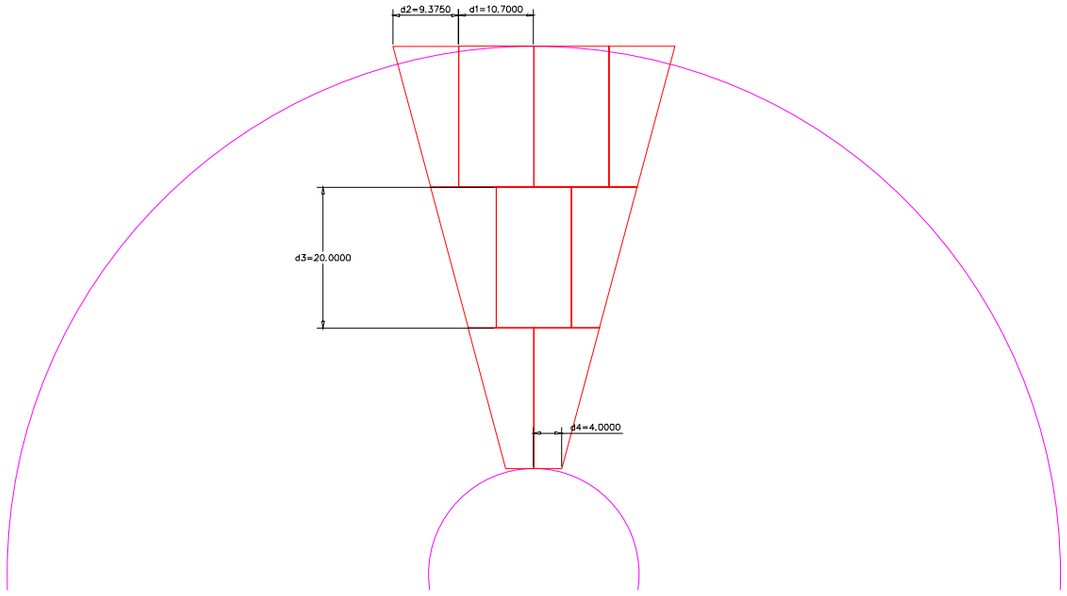
The all-silicon mechanical design. This is difficult to achieve in pixel detectors (other than CCDs) because the natural size unit is the reticule (2.5x2.5 cm)

With a 3D process this can be achieved by matching the sensor spacing to reticules and taking the yield loss requiring 6 working chips. A nice feature is that all of the top interconnect can be done in the final topside aluminum patterning with low mass. Cables are bump bonded to the ends of the ladders.

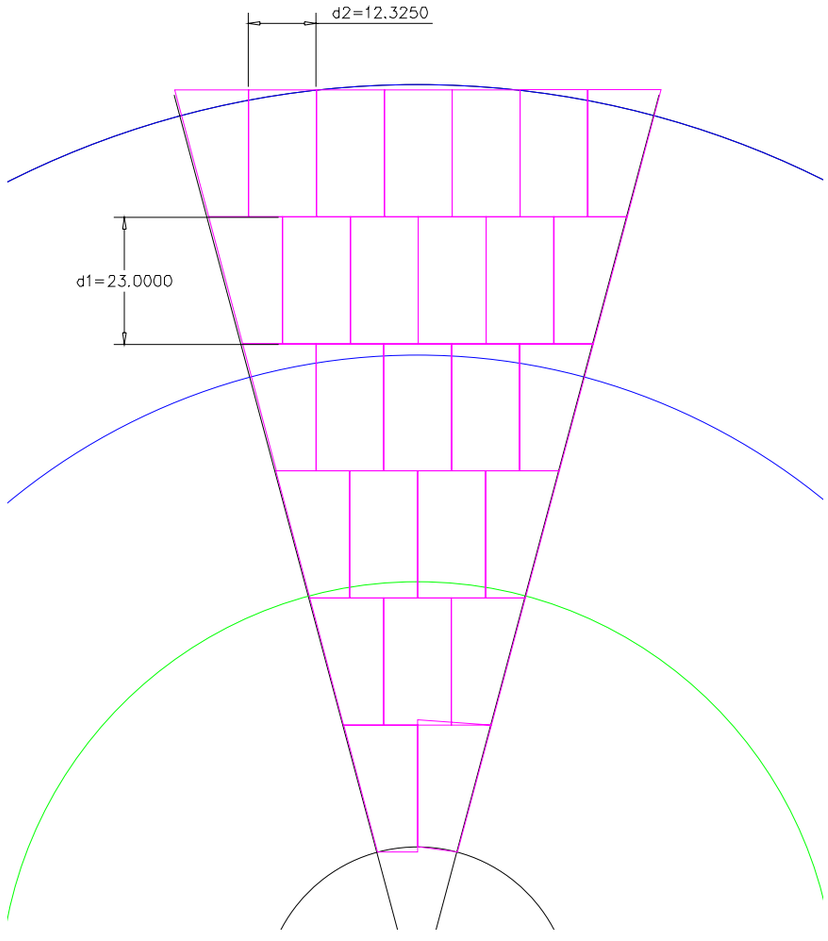


Disk Tiling

The active edge devices are a natural fit for pixelated disks. Only two reticule shapes are needed for the forward disks. More are needed for the inner disks if the keep the small step in radius.



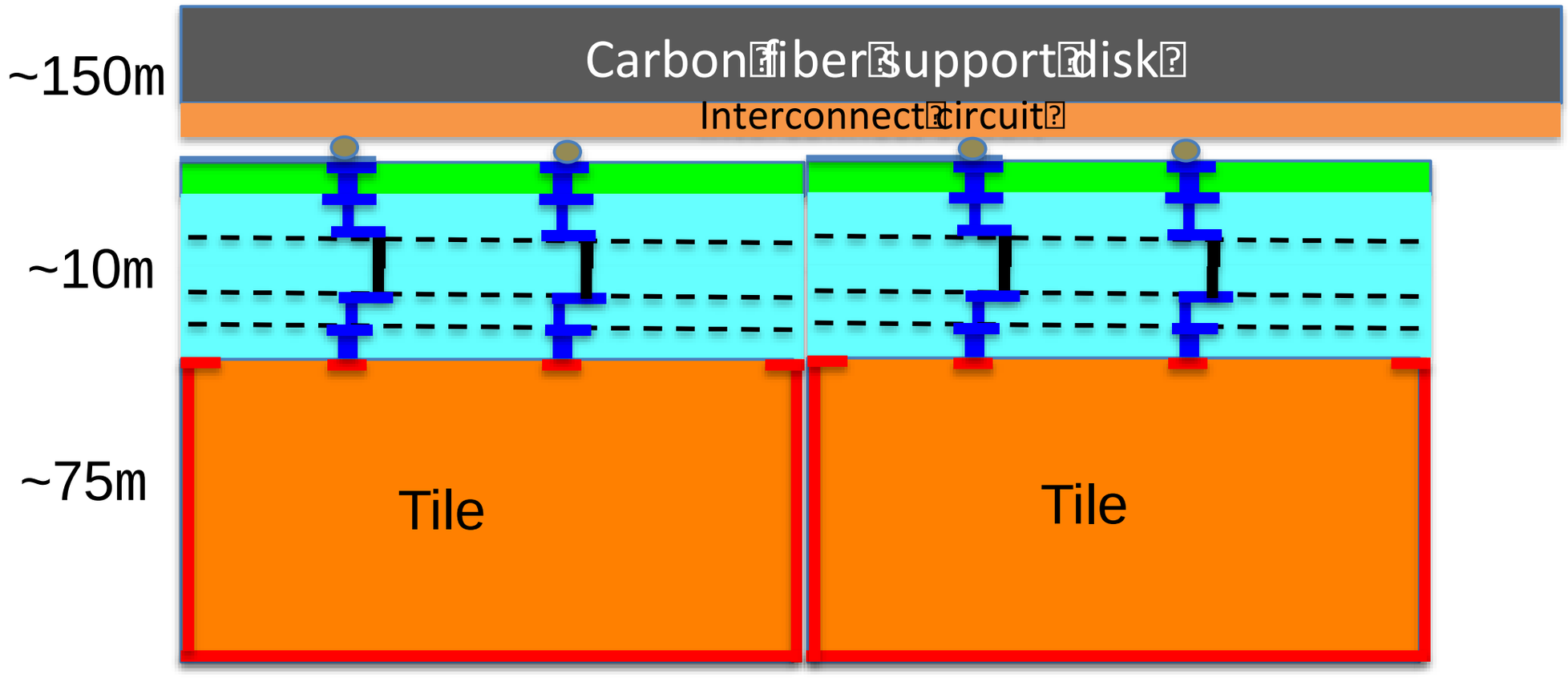
Inner pixel disk



Outer pixel disk radii

Disk Assembly

I assume a slightly higher mass budget for the disks, which allows for carbon fiber supports, still only ~0.35% RL assuming 10 micron average copper trace thickness



This technique can be used for the barrel ladders at some cost in mass.

Summary

- VIP in hand, testing awaiting new test system, manpower at FNAL. VICTR, VIPIC and VIP analog all work
- Active edge sensors in hand – waiting for “simple” dummy ROIC wafers
- Still waiting for the second set of wafer for sensor integration