

# Design of new FEV9 board

FEV9 status report & remaining work

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# FEV9 Status report & remaining work

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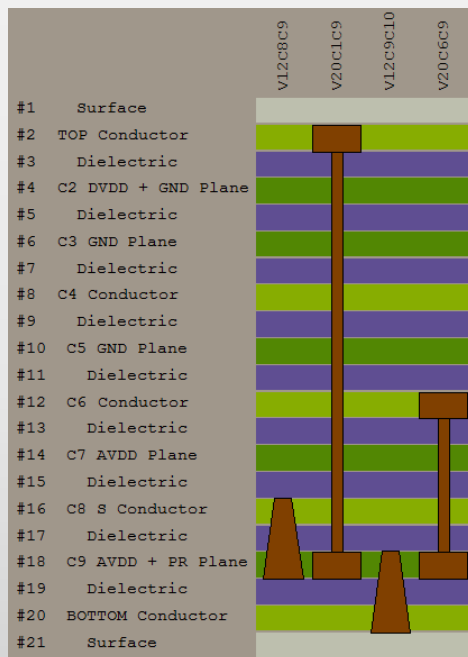
- ▶ FEV9 Status report
  - ▶ Conservative design from fev8\_cip (Chip-On-Board)
  - ▶ Rectifications from fev8\_cip failings
  
- ▶ Remaining work
  - ▶ Adding hottest modification
  - ▶ Manufacturing
  - ▶ Tests



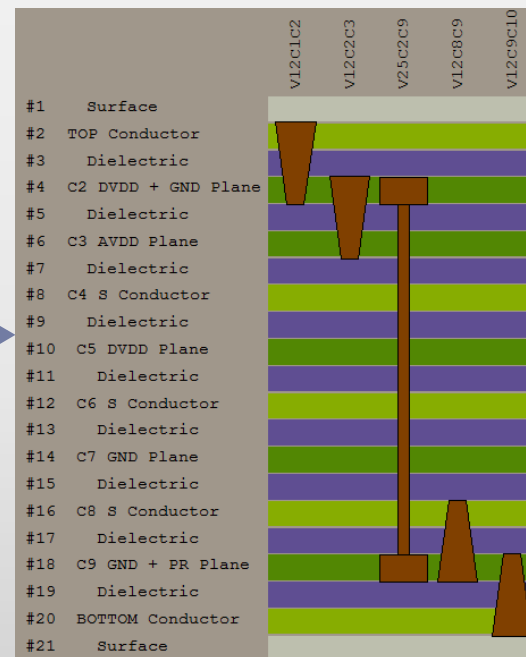
# FEV9 Status report

- ▶ Conservative design from fev8\_cip (Chip-On-Board) but
  - ▶ FEV8 → 4 SKIROC2 in PQFP (35mm<sup>2</sup>) for 1 Si Wafer
  - ▶ FEV9 → 16 SKIROC2 in BGA (17mm<sup>2</sup>) for 4 Si Wafers
- ▶ Rectification from fev8\_cip failures
  - ▶ Cross section & drilling modified → Reliability

FEV8

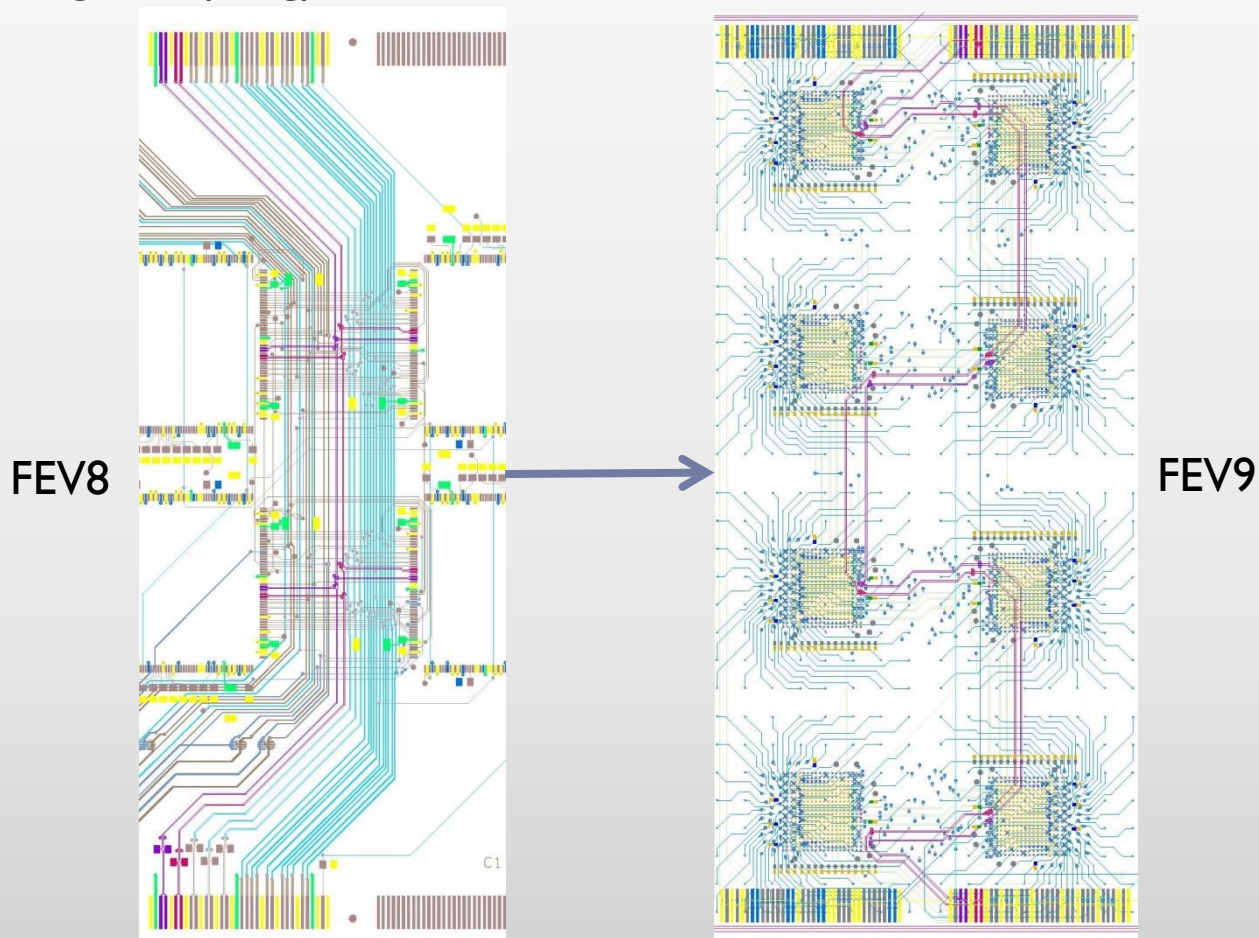


FEV9



# FEV9 Status report

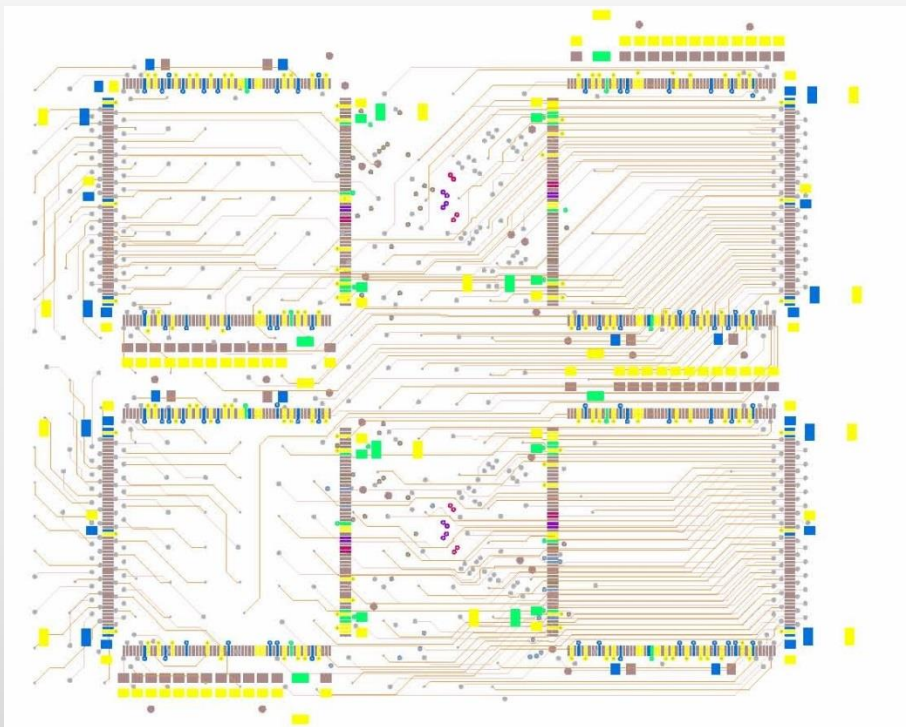
- ▶ Rectification from fev8\_cip failures
  - ▶ LVDS signals topology modified → Avoid wave reflexions



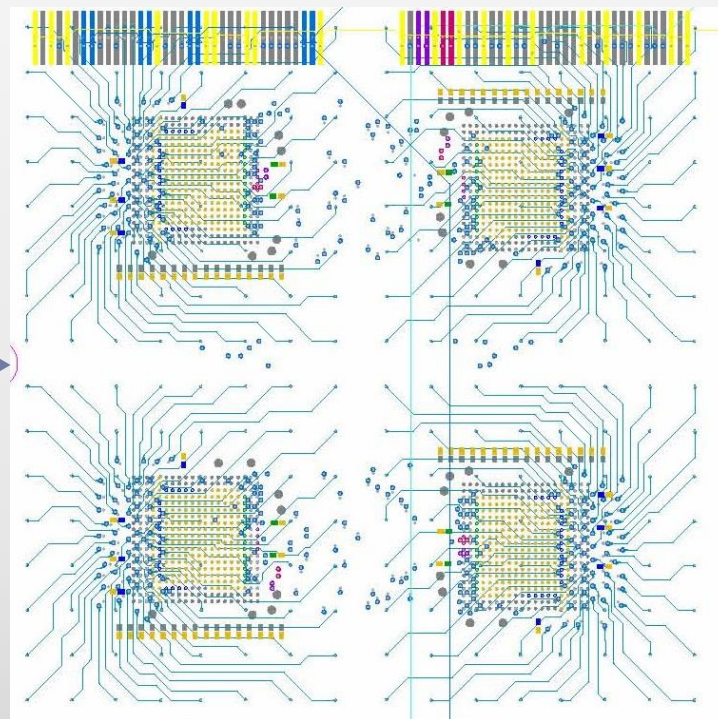

# FEV9 Status report

- ▶ Rectification from fev8\_cip failures
  - ▶ Line length homogenization → Accuracy

(All in mm)	Min Length	Max Length	Standard Deviation	Average Length
FEV8_CIP	2.246	117.576	28.19327	40.32330078
			/5	/2.75
FEV9_CIP	3.072	24.752	5.600527	14.65732813



FEV8



FEV9



# Remaining work

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- ▶ Add hottest modifications → a couple of week
  - ▶ Study if straight lines for LVDS can be done
  - ▶ Add strap for up side down board capability
- ▶ Manufacturing and assembly → 10 boards FEV9 for september
- ▶ Tests → On september.



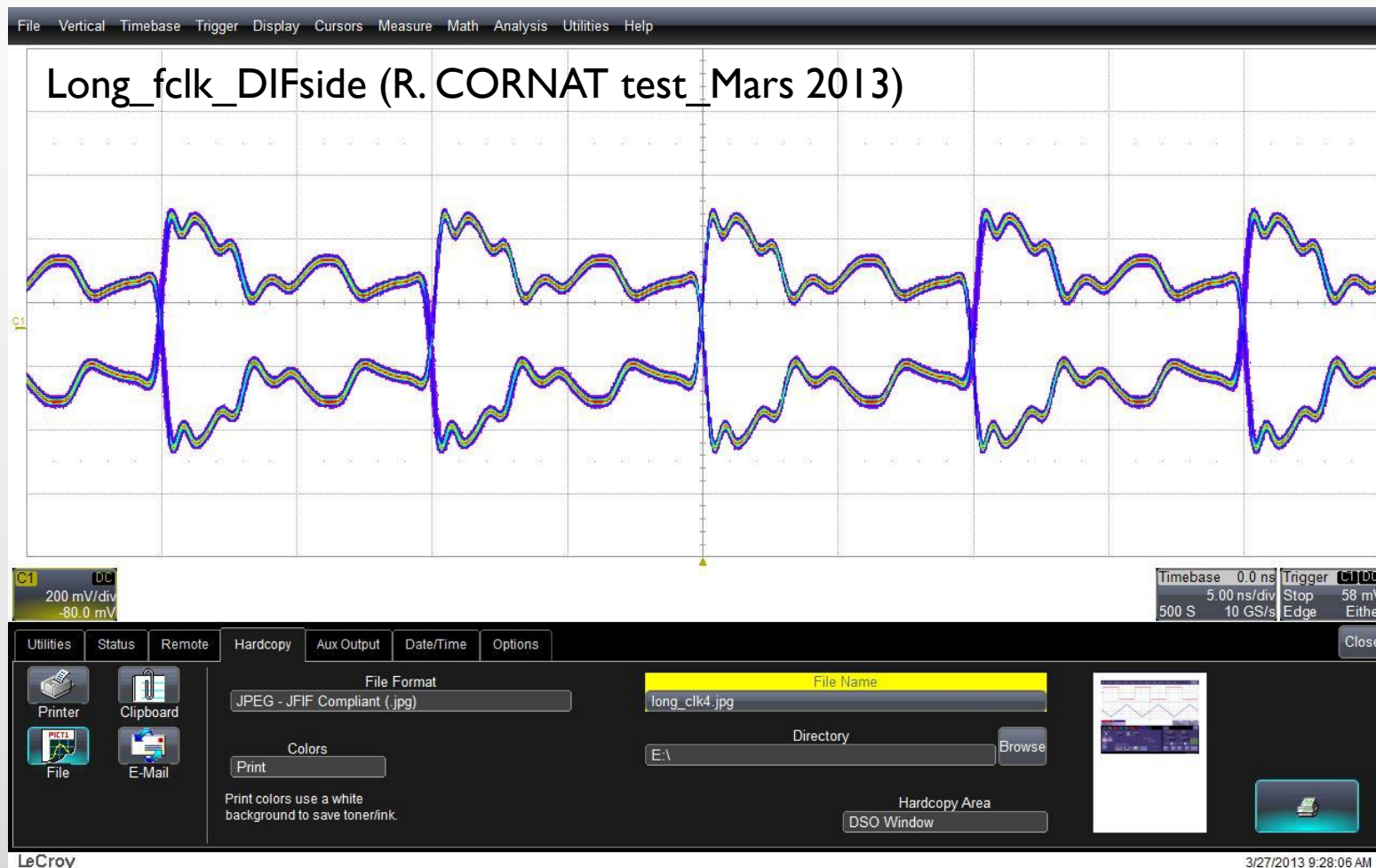
# Questions ?

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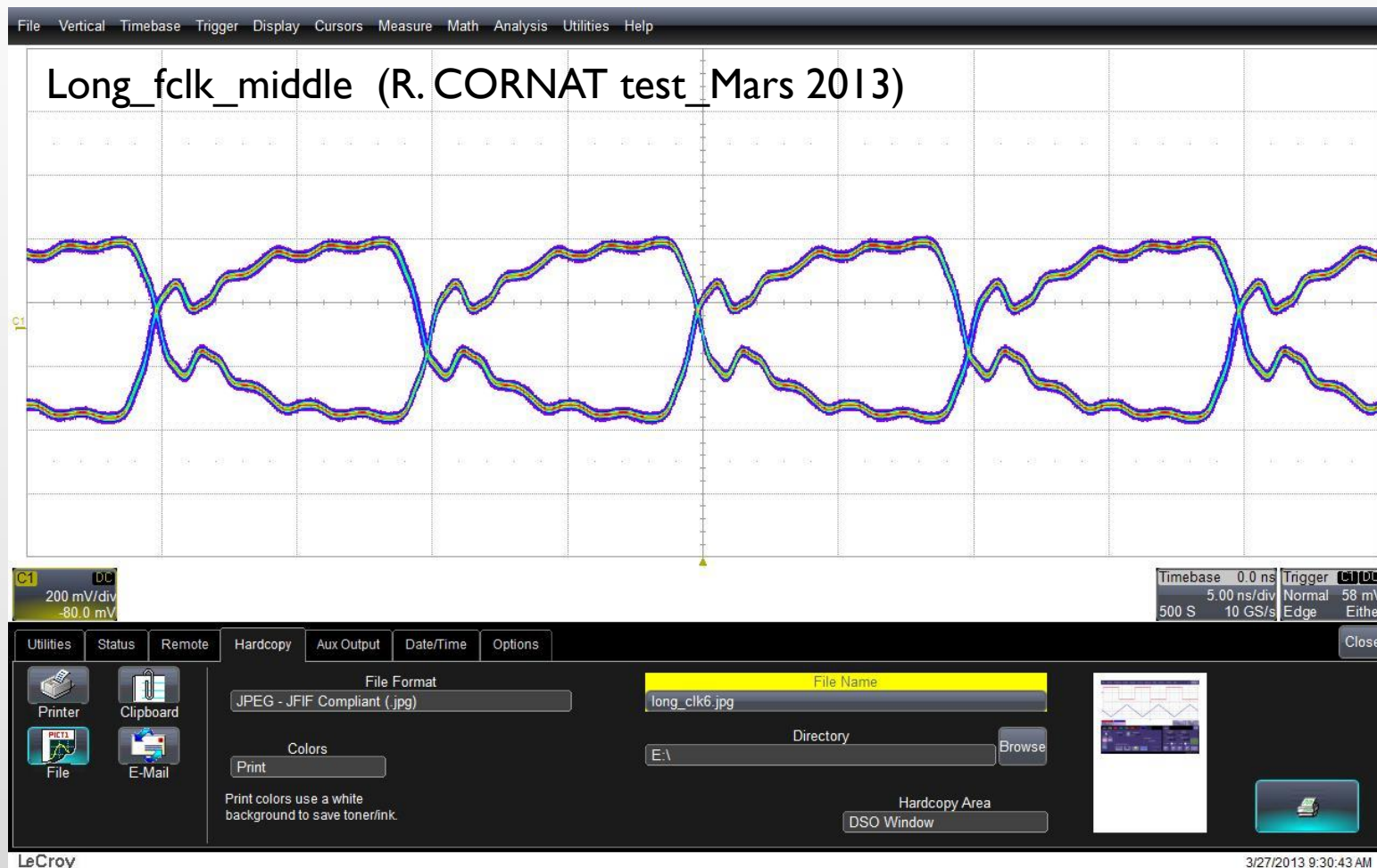


# Back up slides

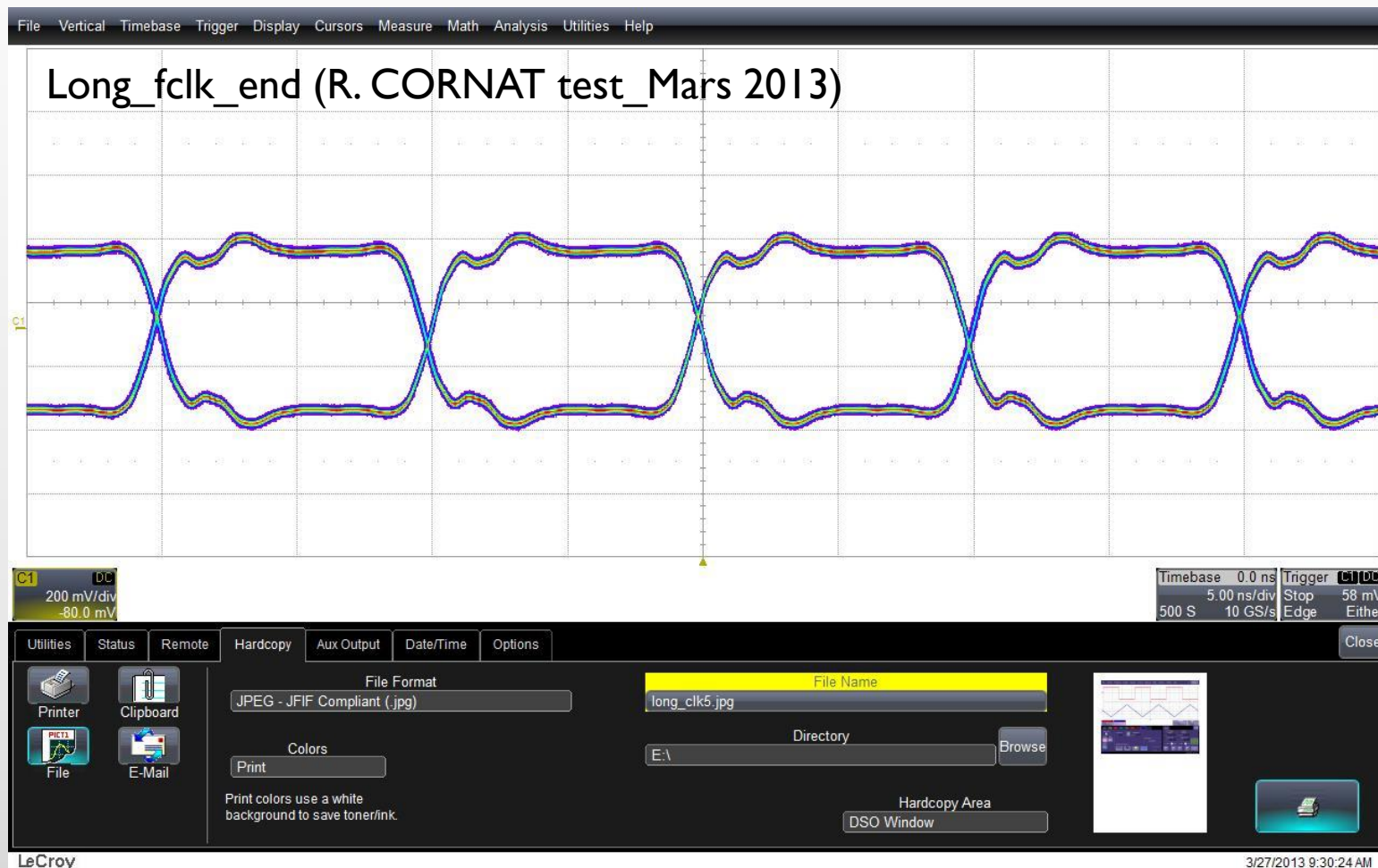





# Back up slides




# Back up slides



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