# Understanding of SKIROC performance

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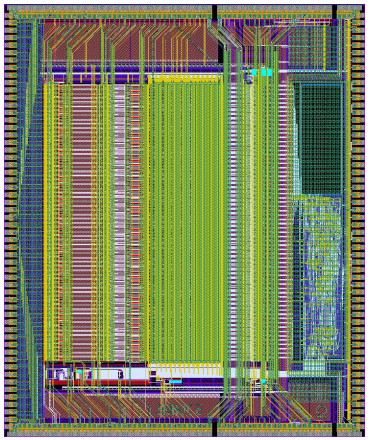
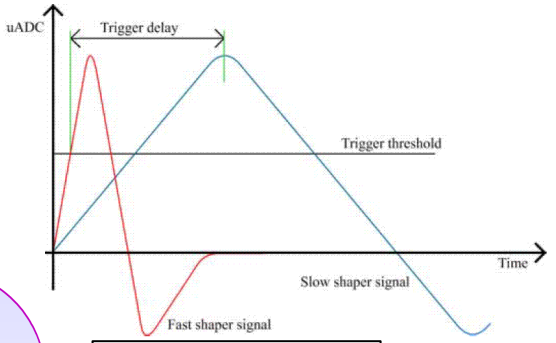
Special thanks to the electronic and DAQ experts:
Stéphane Callier, Rémi Cornat and Frédéric Magniette
And to:
Romain De Abreu (Internship student)

# Front end electronics: SKIROC

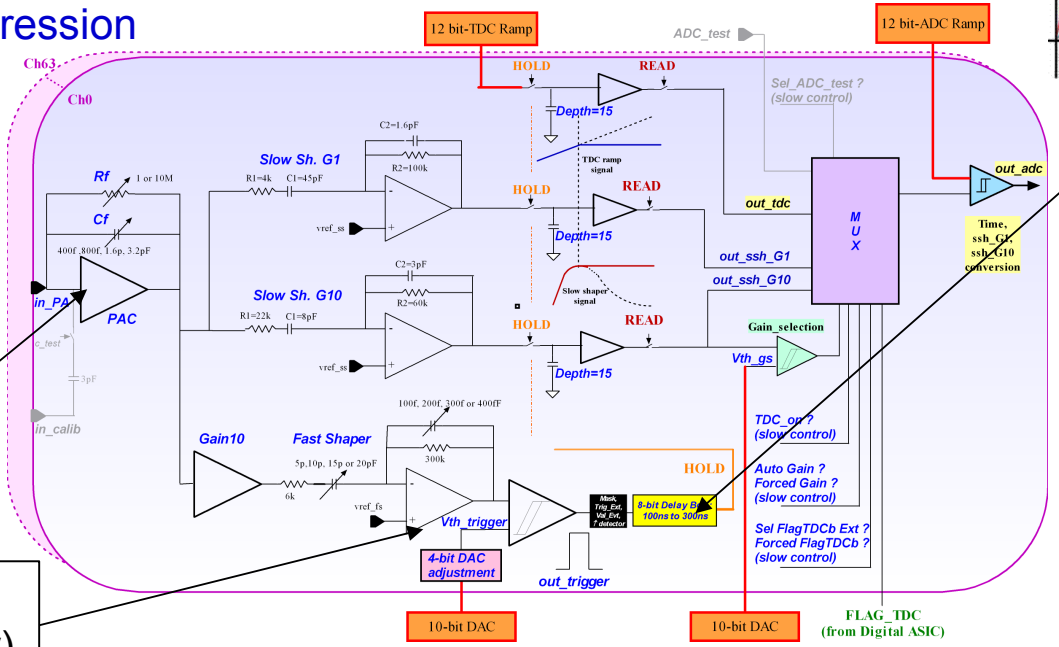
SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- SiGe 0.35µm AMS
- 7.5 mm x 8.7 mm
- High integration level (variable gain charge amp, 12-bit ADC, digital logic)
- 64 channels
- Large dynamic range (~2500 MIPS), low noise (0.4 fC – 10 pC)
- Auto-trigger at ½ MIP
- Low Power: (25µW/ch) power pulsing
- On chip zero suppression






Trigger delay




Preamplifier (adjustable gain)

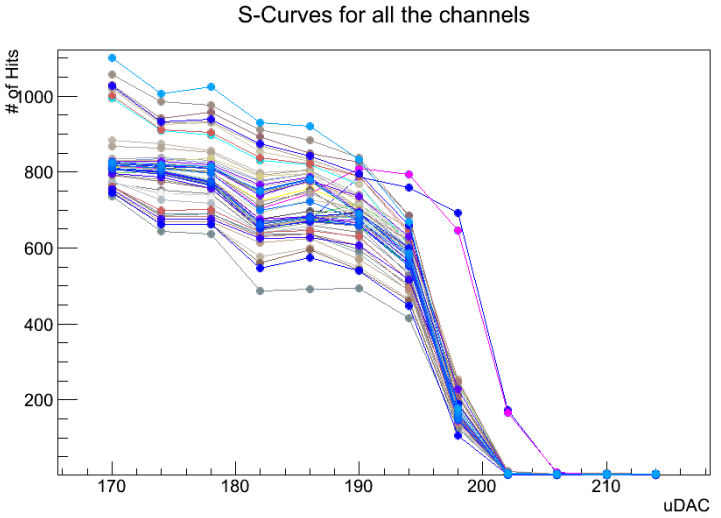
Internal trigger (self-triggering capability)

# Calibration of SKIROC

Establishment of calibration procedure for a large number of cells

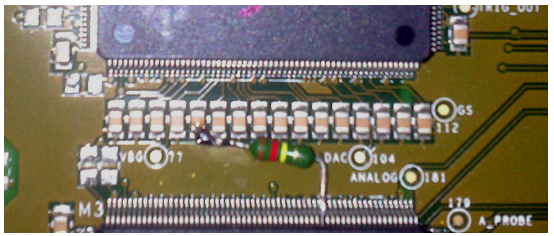
## Trigger threshold

- depends on the gain



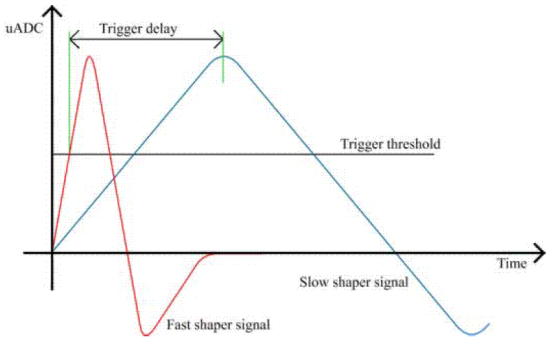

- Individual channel threshold adjustment

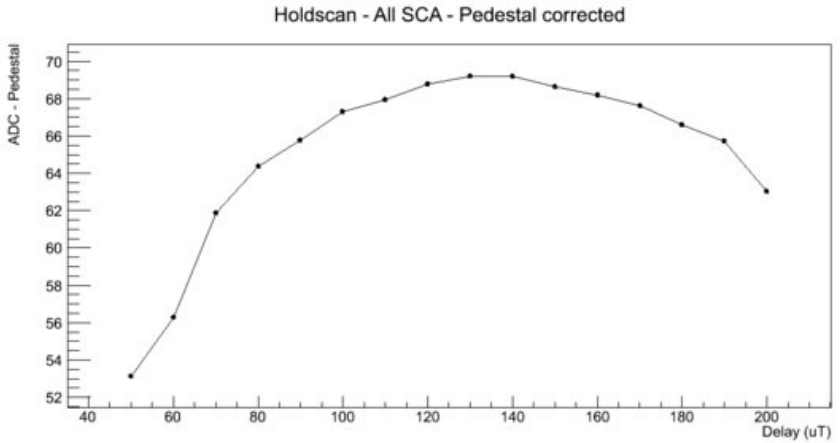
Range too small → R to increase current in the 4-bits DAC adjustment




OK on test bench → to be tested in beam (need new calibration procedure)

## Trigger delay

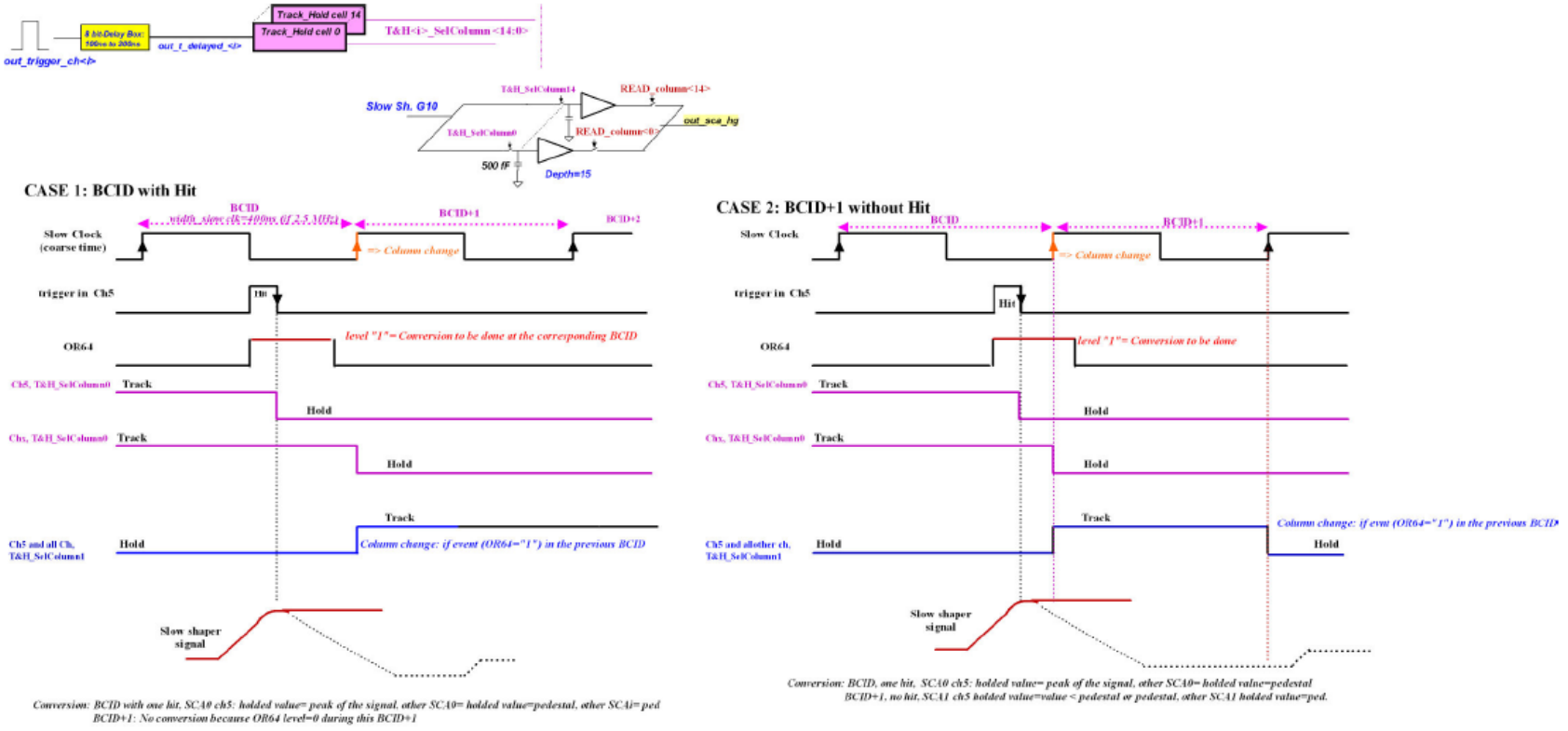


# BCID+1 effect

Retriggering of the ASIC without hit

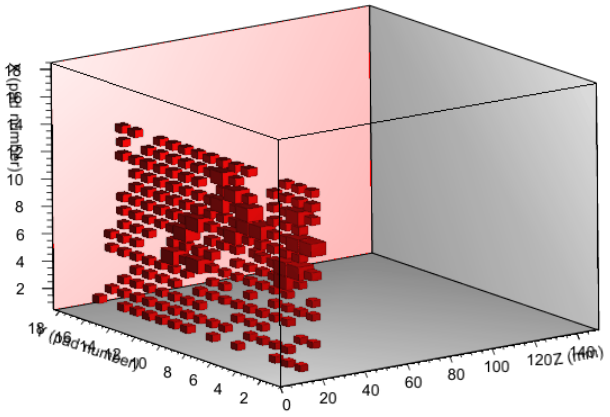
- Understood (see October 2012 Electronic meeting)
- ~13% of the events (for $T_{slowclock}$ = 2.5 MHz):
  - ➔ Calculated: $T_{slowclock}/T_{nor64}$
  - ➔ Measured with test bench and test beam
- Easy to cut off-line

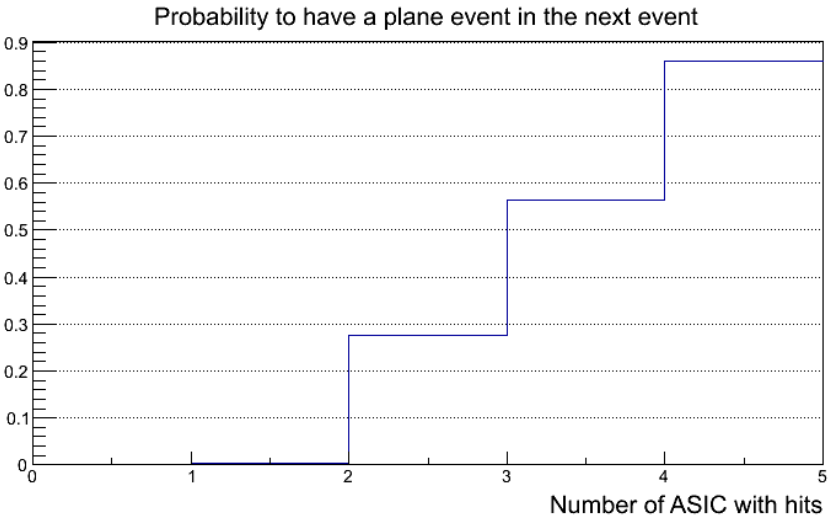


# Plane events

PA is referenced to the analog power supply level
Instabilities of  power supply level → fake events

- VDD_delay/sca plugged on analog power supply → increase instabilities of power supply level
- Analog power supply common to the 4 ASIC
- Self-sustained → sometimes filled all the 15 ASIC memories
- Highly dependant of the number of ASIC with hits, dependant of the number of triggered channels

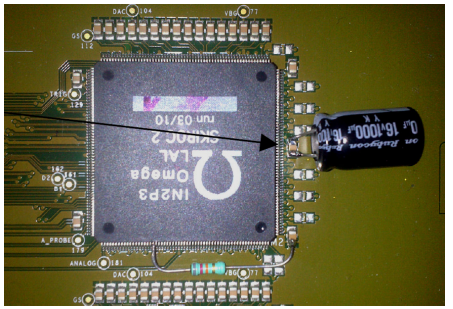




# Plane events

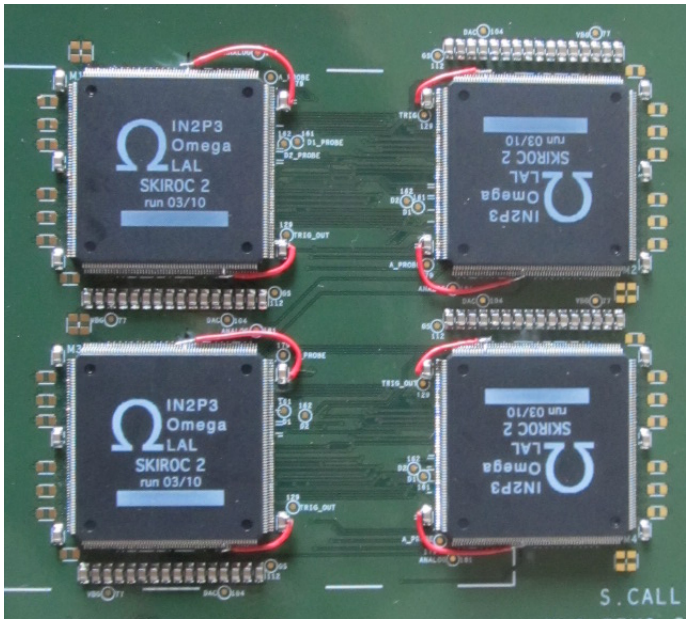
Proposed patchs

- Bigger capacitances close to the ASIC to stabilize power supply



First tests @ LAL ( Nov 2012)

- 2 power supply lines: Modify VDD_delay/sca routing to protect PA power supply (pin-clipping)




First tests @ LAL (November 2012):

- Injection in the 4 ASICs
- Reduction of the plane events: ~80% → ~10% (both capa and pin-clipping)

2 slabs modified to be tested during the last test beam (February 2013)

- 1 slab with big capa
- 1 slab with pin-clipping

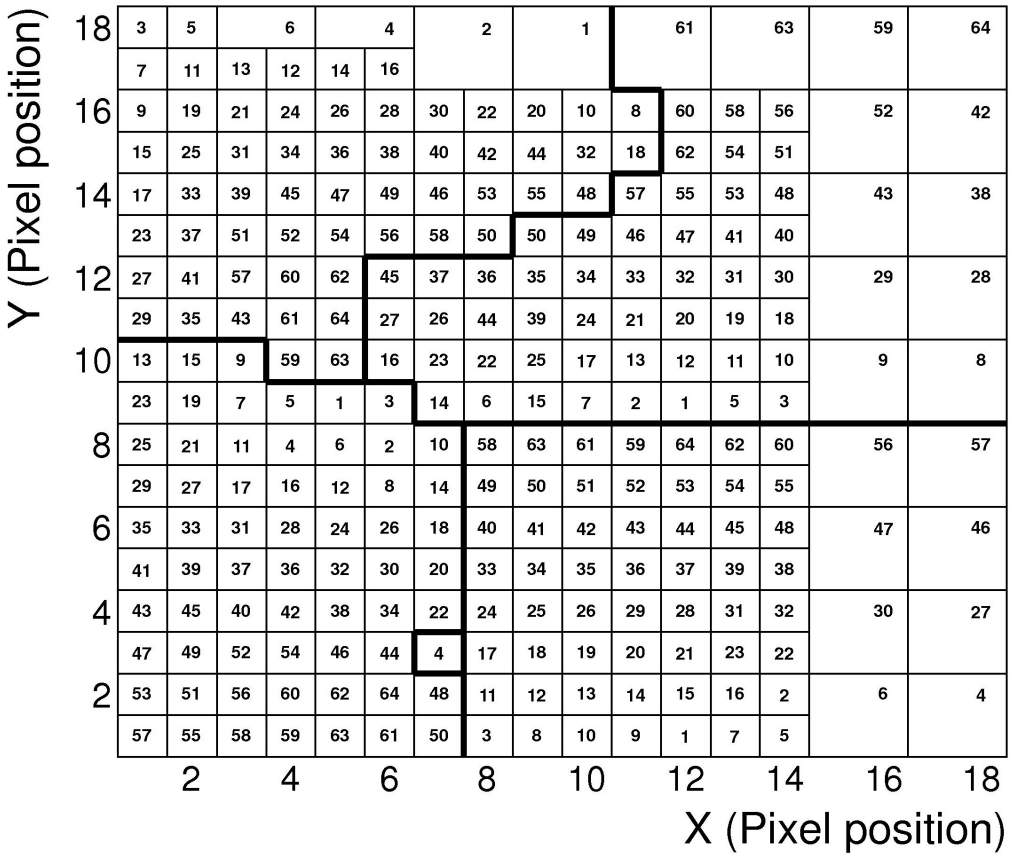
→ significant improvements (see Jérémy's talk)

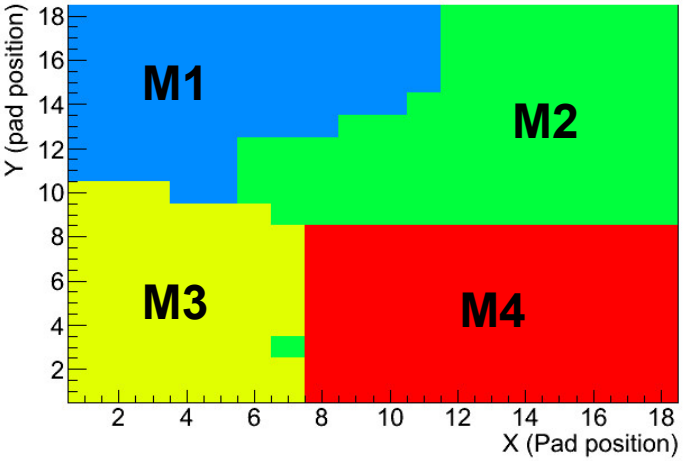
# PCB

PCB is critical → Goal :1 mm thick, 8 layers, 1% flatness , ASICs bounded into
Current: FEV8 Chip in package, 1.4 mm thick

Line density in PCB ➔ routing is crucial

- Noise
- Cross talk (Digital / readout channels → readout channels)



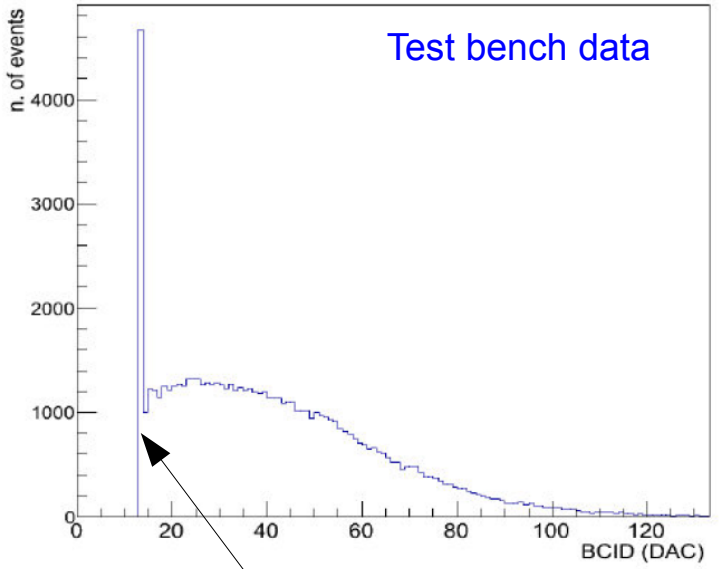
# Switched off channels

Noisy channels + no individual channel adjustement → channels linked to several pixels

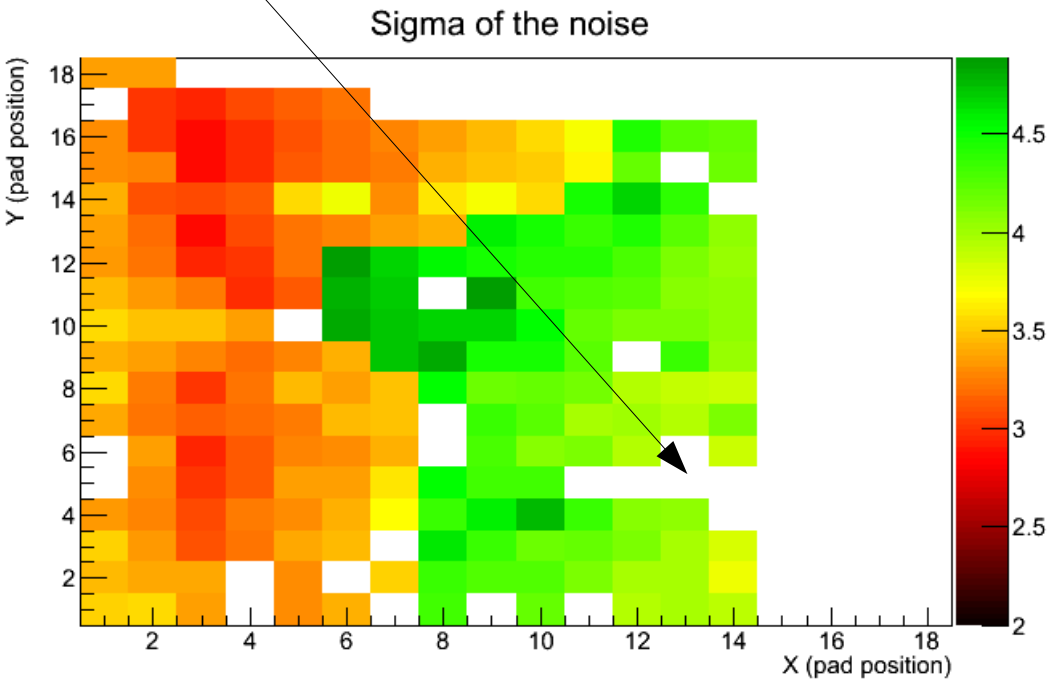
Cross talk with digital lines (valEvt, startAcq, clocks, injection line):

e.g.: ValEvt line close to M4 35-37: signal > 1 MIP

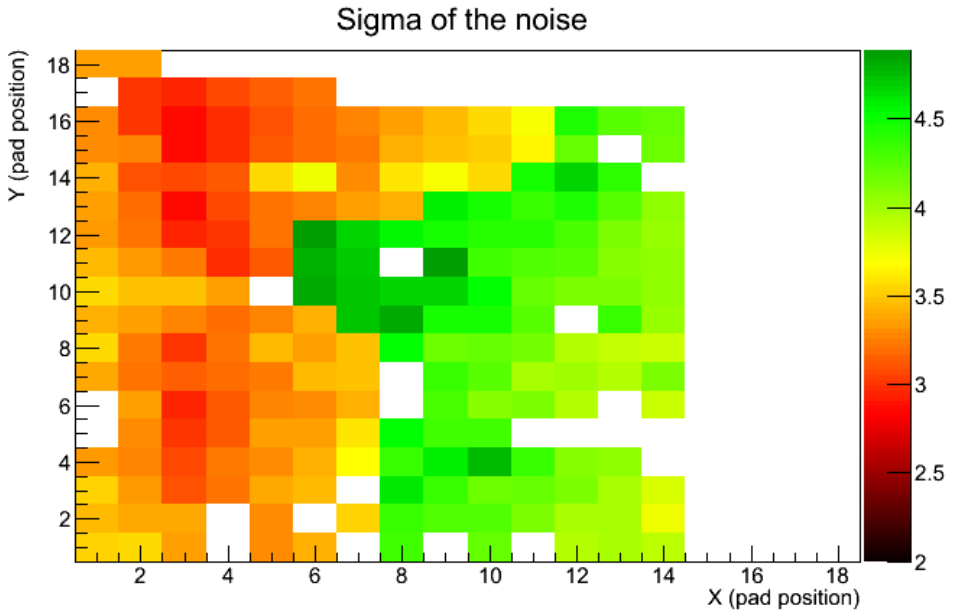
BCID distribution in channel 35 (M4)

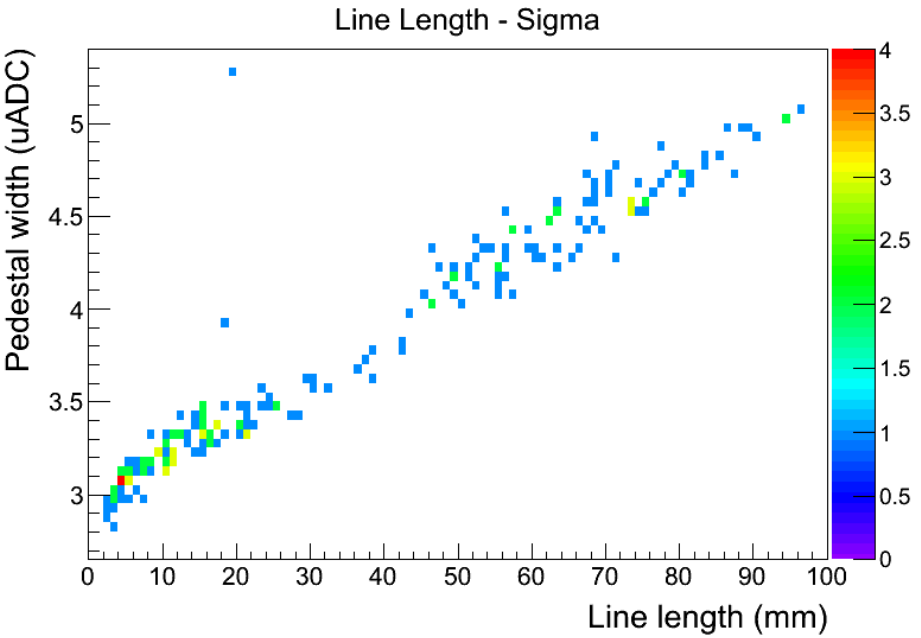



Synchronized with valEvt signal (13 BCID)



# Noise studies




Noise ∝ Line length

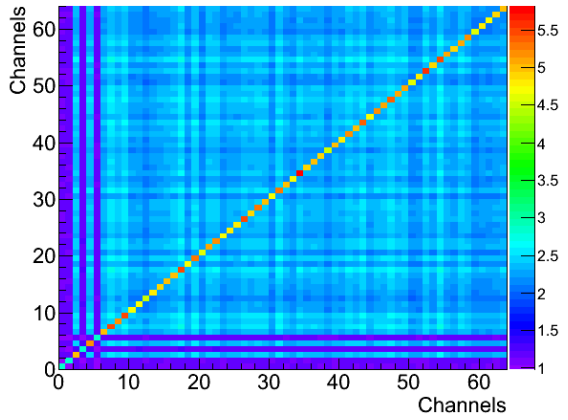
Already improved for the 16 ASIC version of the PCB

# Coherent noise (general behavior)

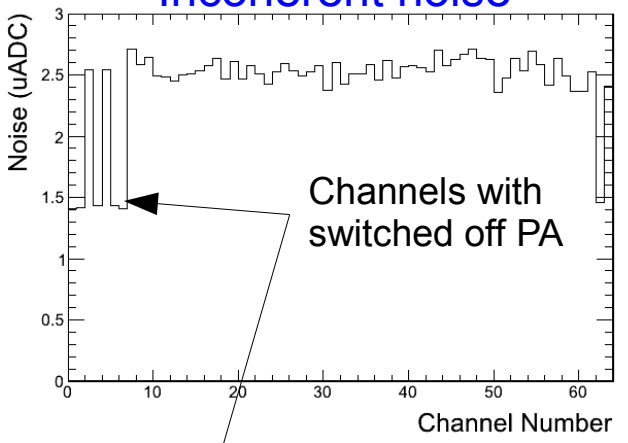
Development of algorithm to identify coherent noise (continuation of Roman studies)

e.g. : chip M1

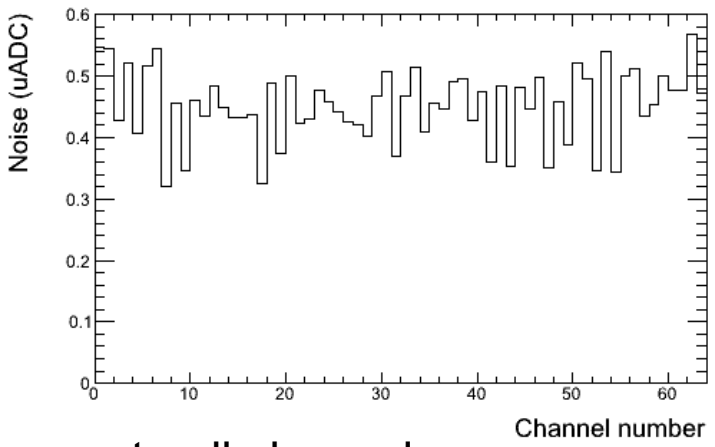
We extract incoherent noise + 2 sources of coherent noise:

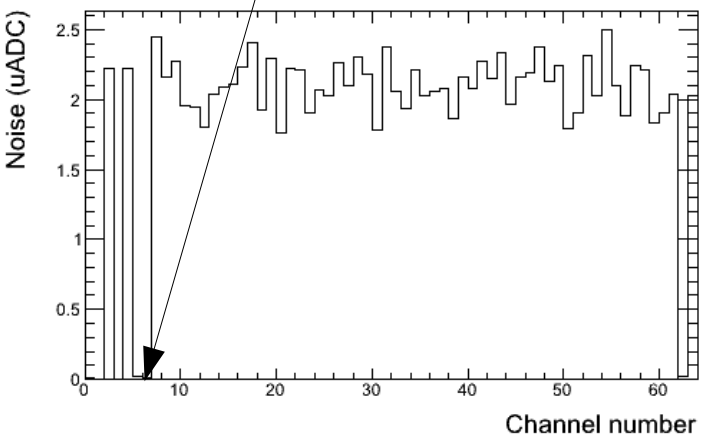



Incoherent noise




Coherent noises




Common to all channels:

- Due to the ramp? (Omega expects ~0.5 ADC)

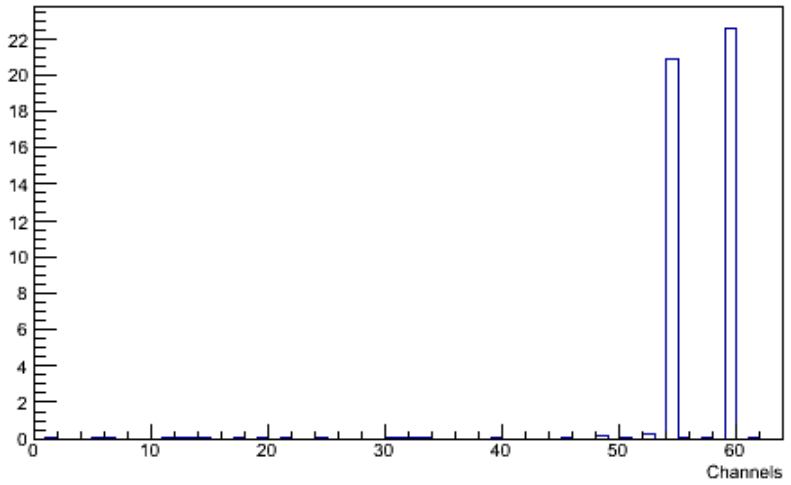
Common to channels with switched on PA:

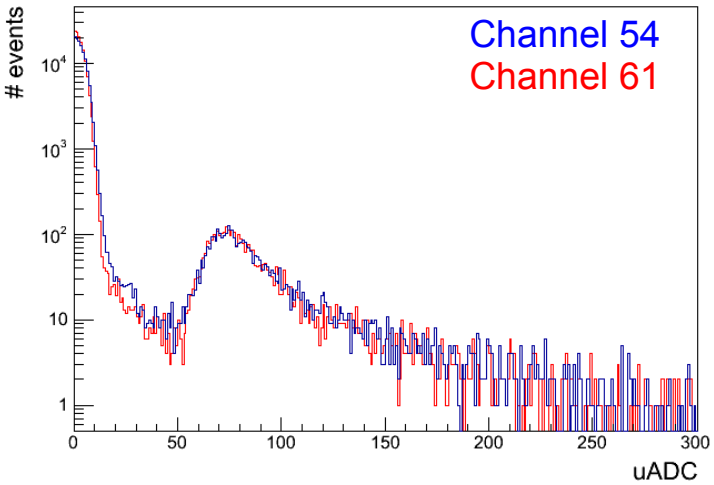
- Due to PA?
- To be clearly identified and reduced (if possible): under discussion with experts (Omega)

# Correlation studies

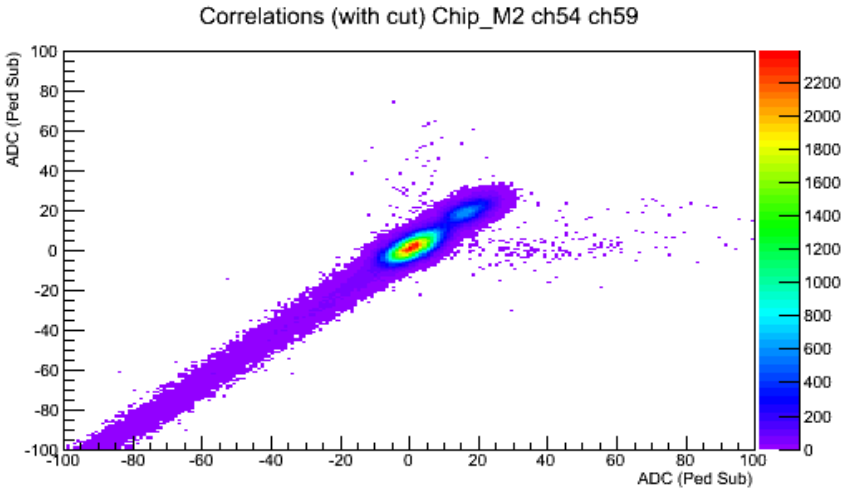
Chip M2 (several layers):

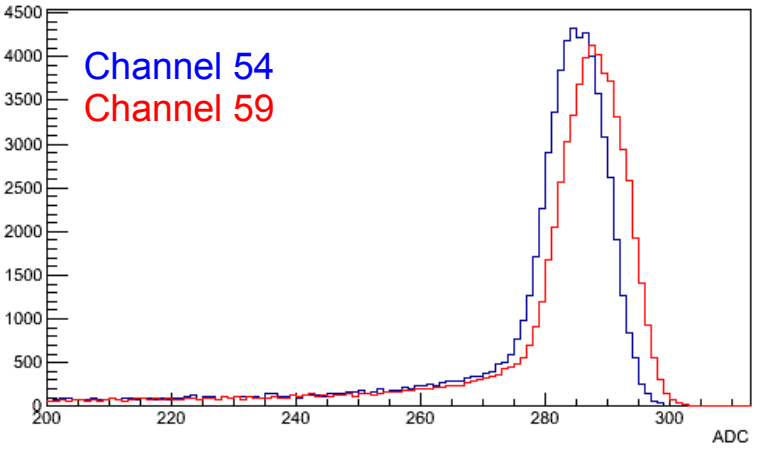
- Another coherent noise source → 2 highly correlated channels
- No clear idea of the source




We don't see an effect on MIP distribution

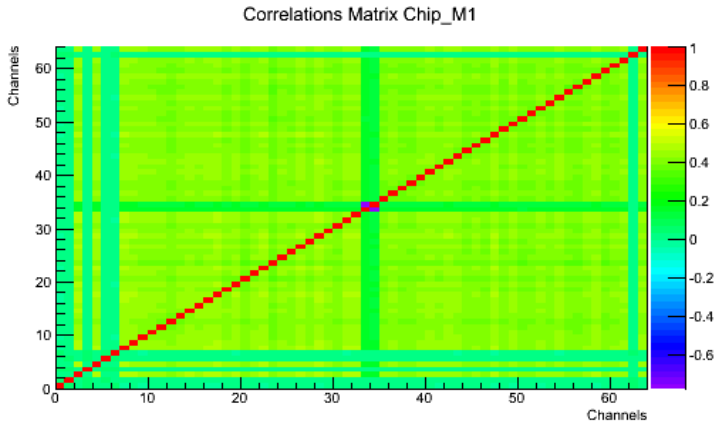


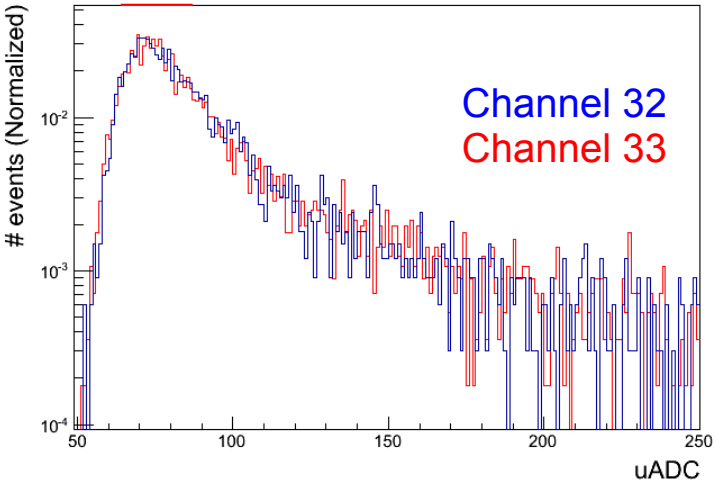



# Correlation studies

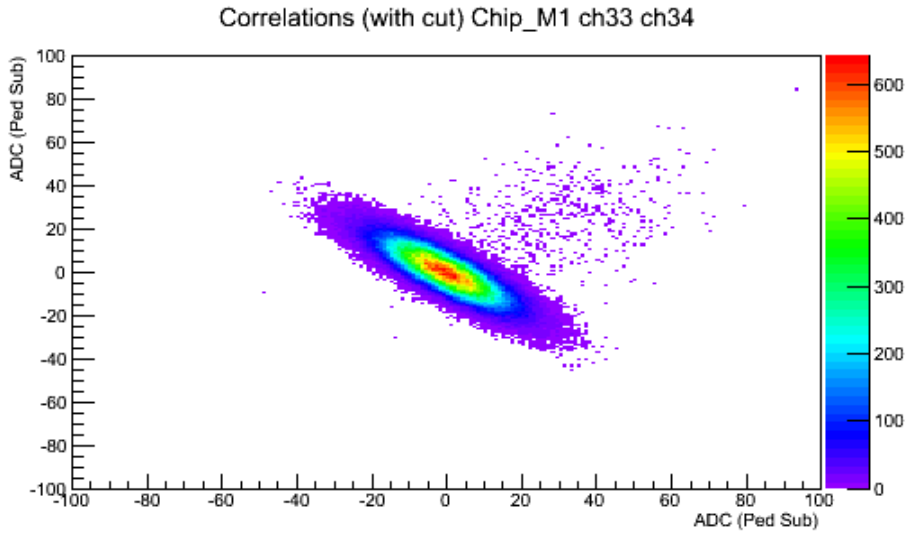
Chip M1 (only in 1 slab):

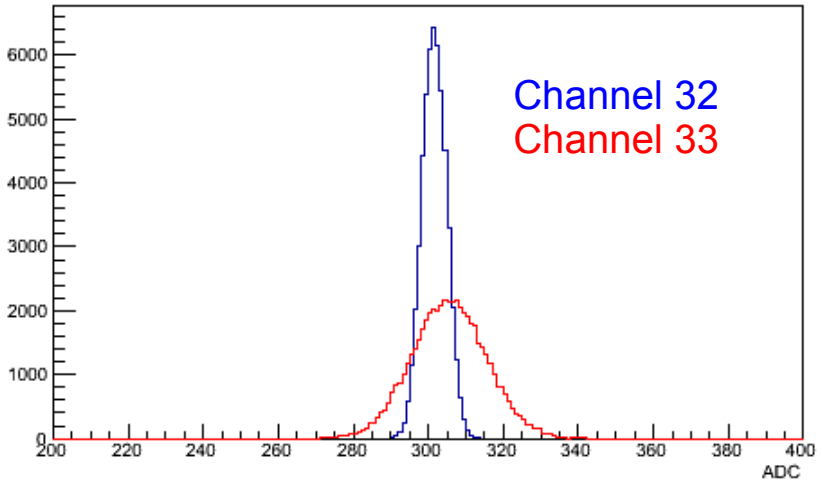
- Another coherent noise source → 2 highly anti-correlated channels
- No clear idea of the source of this behavior



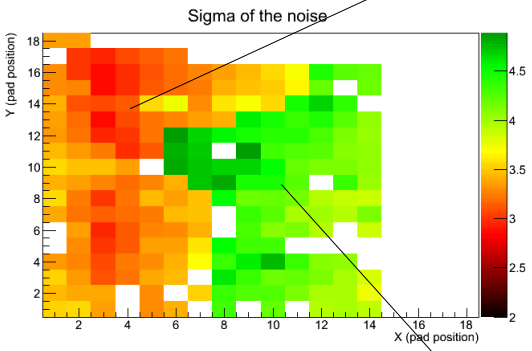

We don't see an effect on MIP distribution.
We should check the S/N ration @ low gain

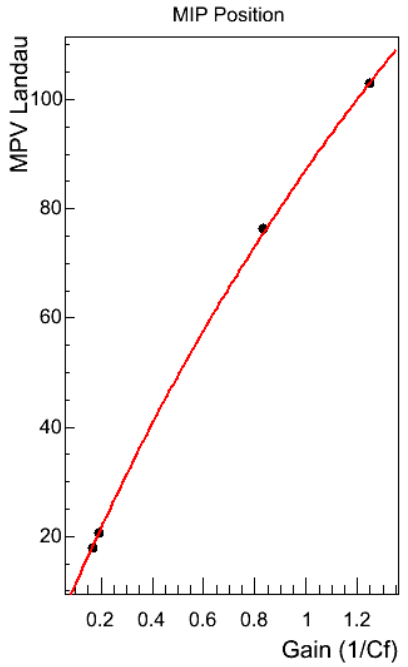


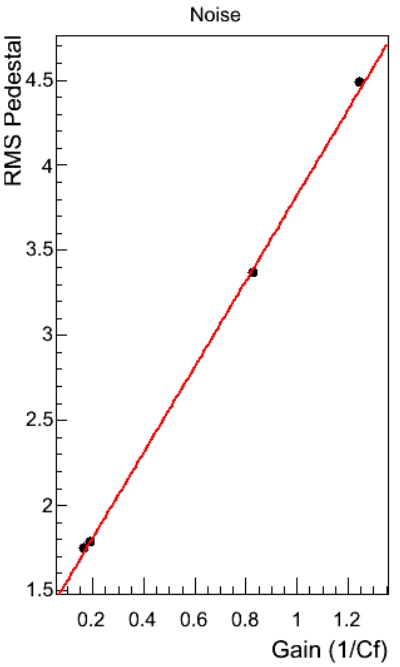



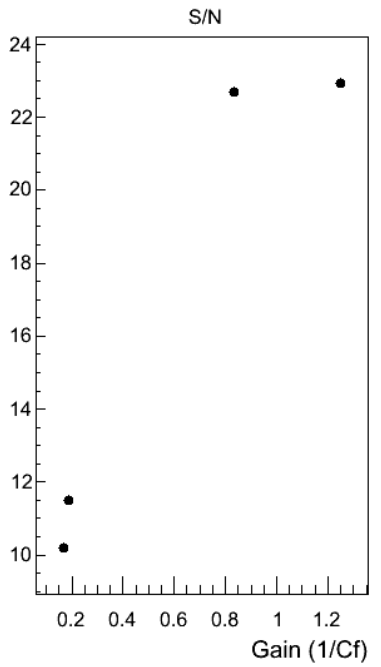
# SKIROC results as a function of the gain

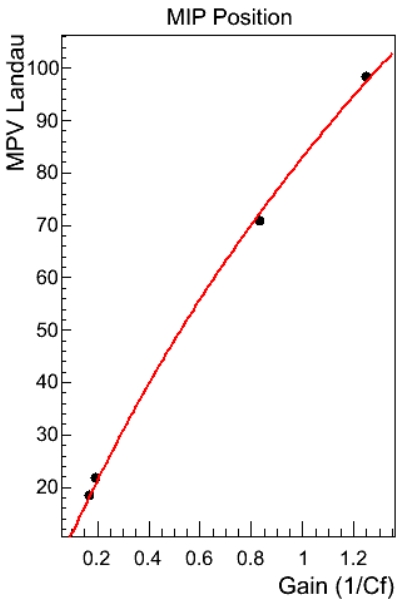
Gain $\propto$ $1/C_f$

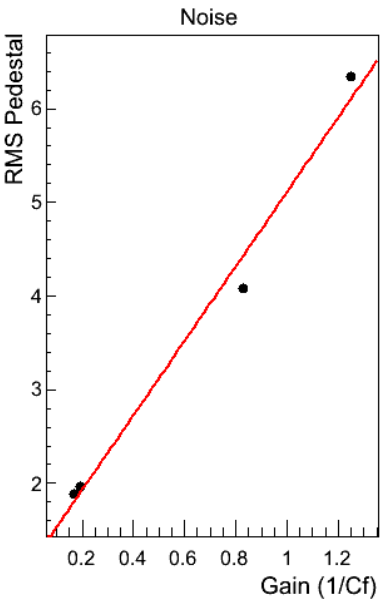


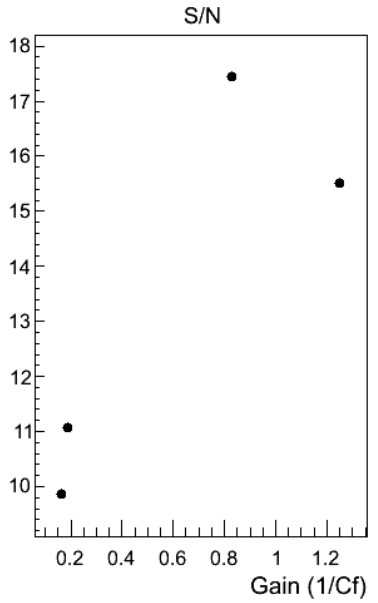



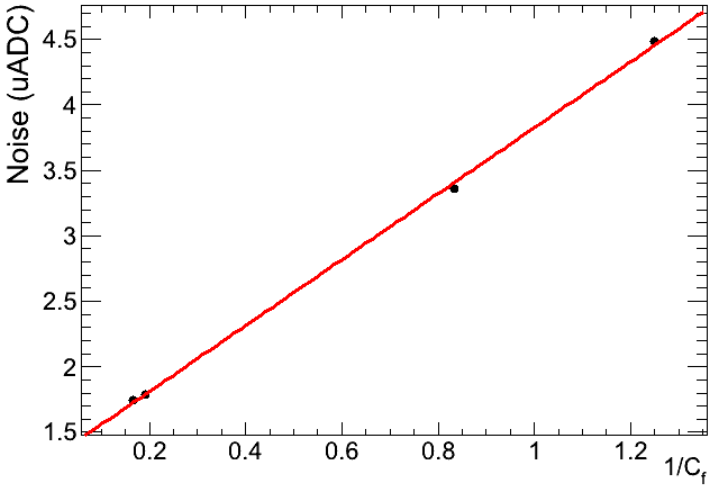



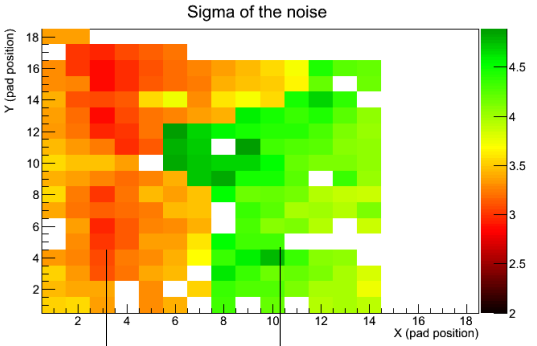



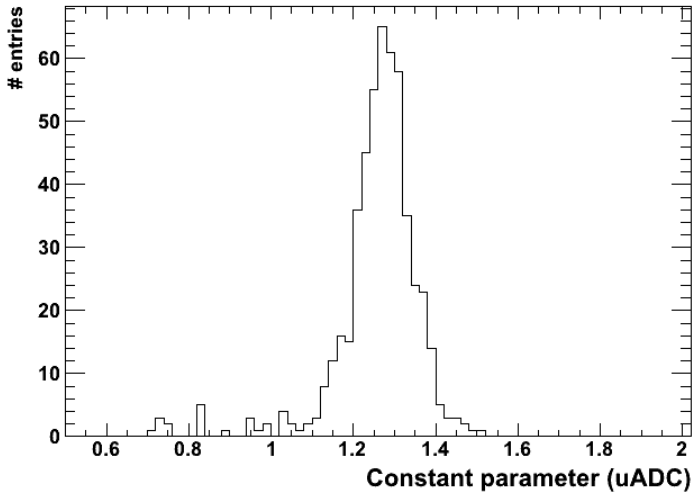

Saturation of the MIP position → bad holdscan calibration?

# Fit of the noise as a function of the gain

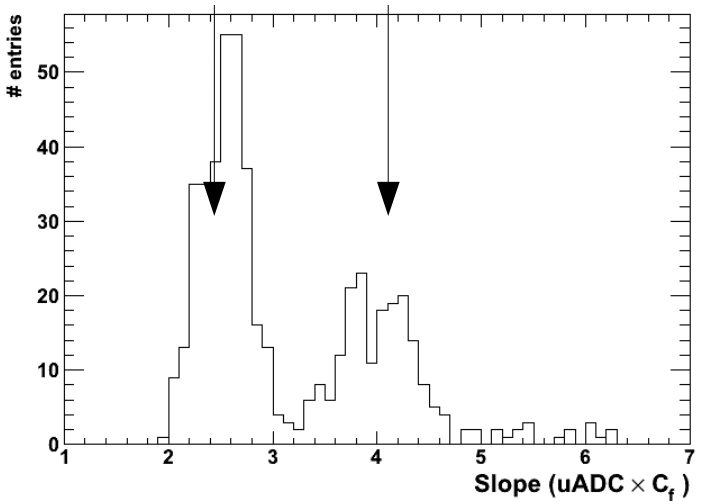



Constant parameter of the linear fit for all channels / ASICs / Slabs

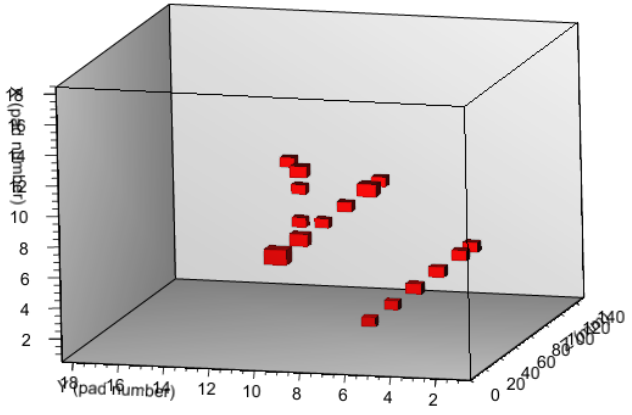



Slope of the linear fit for all channels / ASICs / Slabs

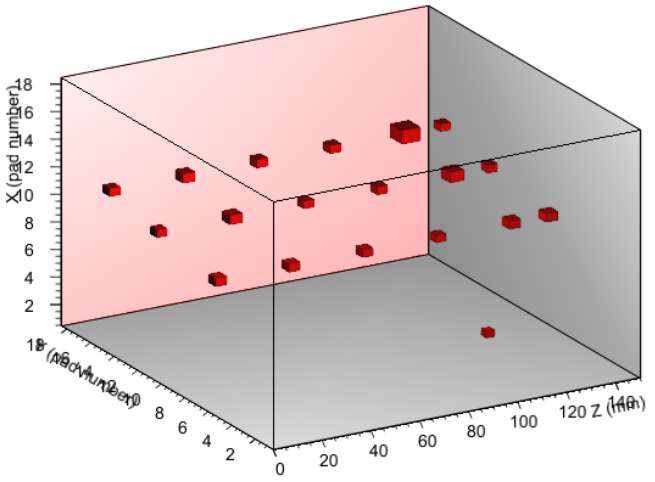


# Event display

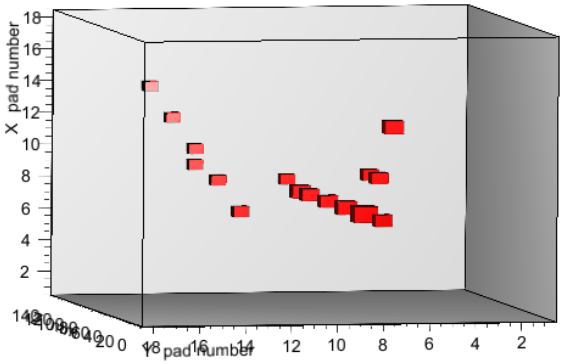
## 2 e- (3 GeV, no tungsten)



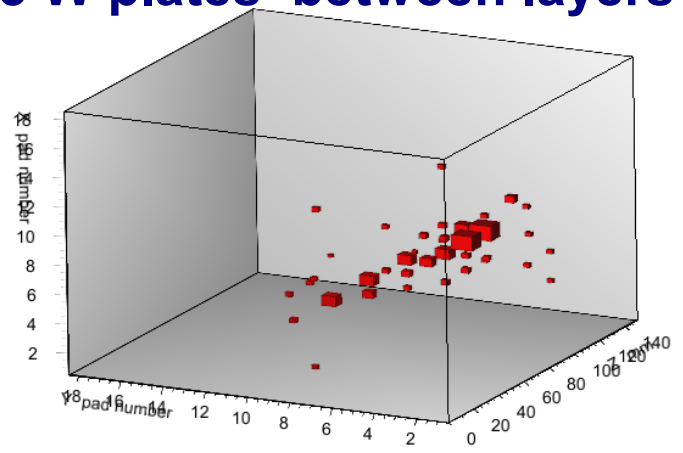
## 3 e- (3 GeV, no tungsten)



## 1 cosmic + 1 e-
## (3 GeV, no tungsten)



## 1 e- (5 GeV)
## 5 W plates between layers



# Summary

2012 test beams have provided useful data.

- Mainly thanks to the Frédéric's work on DAQ software

Major step forward in the understanding of the detector

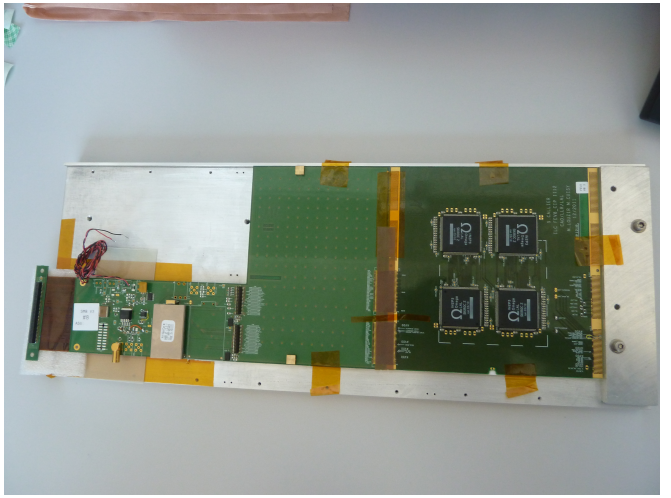
- BCID+1
- Plane events
- Switched off channels due to crosstalk with digital line or readout channels
- Noise structure

**R&D in progress… first test beam shows promising results**

# Back up

# The road to the technological prototype

Intermediate step: { First test in beam / Benchmark to go further



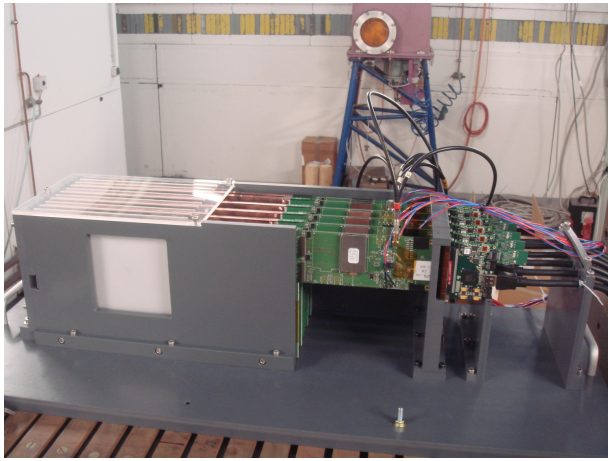
- U structure (single detection layer per slab)

- Si wafer:
  - 9x9 $cm^2$ – Thickness = 320 μm
  - **pixel size: 5x5 $mm^2$** :lateral granularity = 4 x better than physics prototype

- 4 SKIROCs per slab (1⁄4 final design)
  - 4 x 64 channels = 256 channels/slab

DESY : e- (1 - 5 GeV)

- Spring 2012 : 1 layer
- Summer 2012 : 6 layers
- Winter 2013 : 10 layers



# PCB

PCB is critical → Goal :1 mm thick, 8 layers, 1% flatness , ASICs bounded into

FEV COB

- Available since december 2012 (Boards from Exception and Protecno)
- First board for 16 ASICs (btw. Several proposal to assure planarity exist)
- Now equipped with 8 SKIROC ASICs (Boncing by CERN) → Needs testing
- However, bonding was not straightfoward, thin bonding pads can be improved