Silicon-Tungsten ECAL, tests and plans

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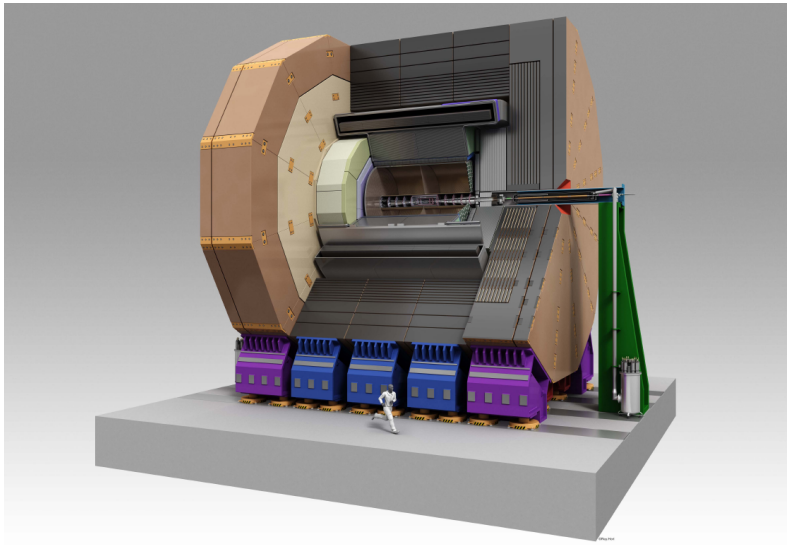
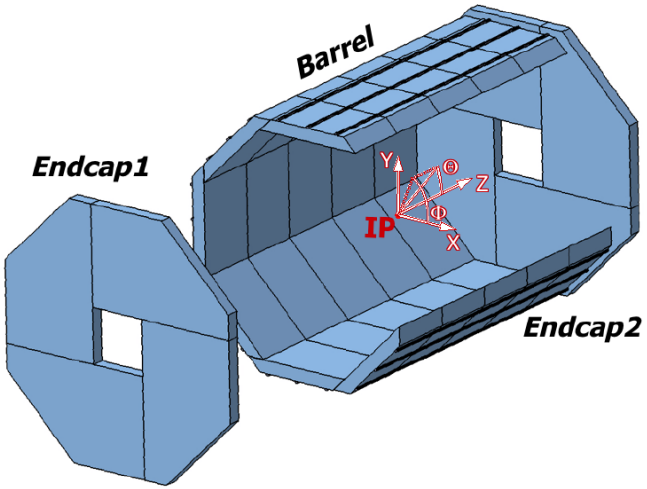
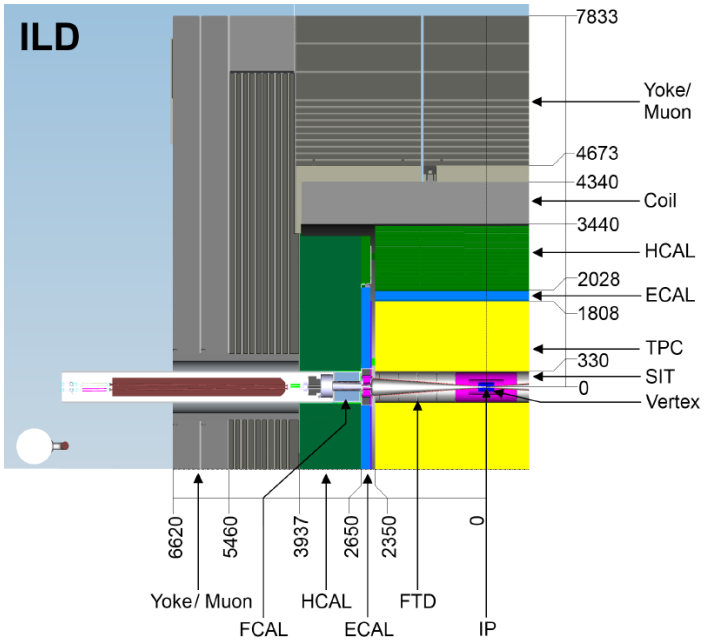
Outline

Topic

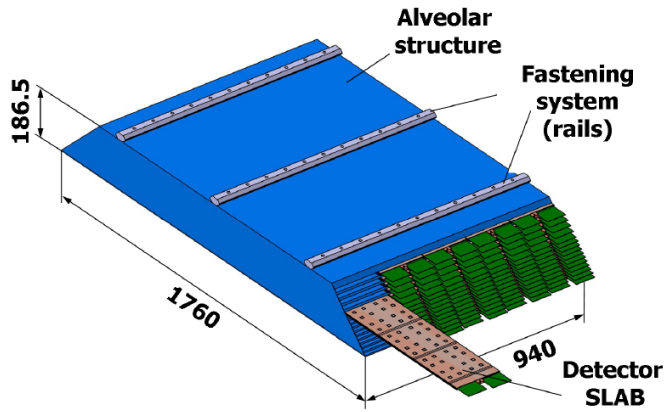
Overall view



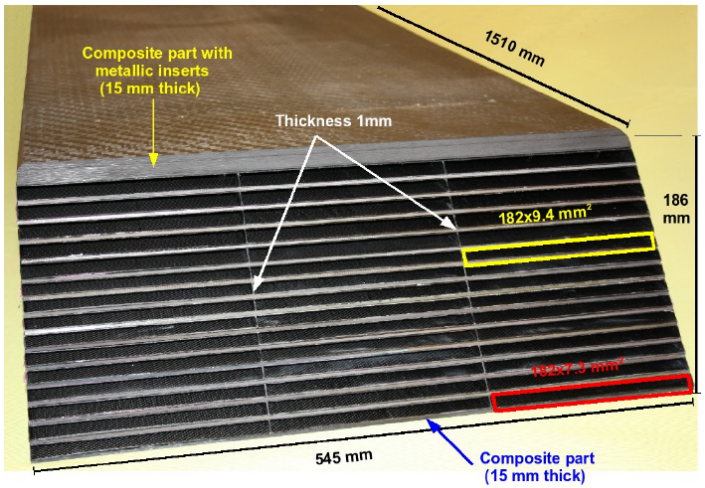




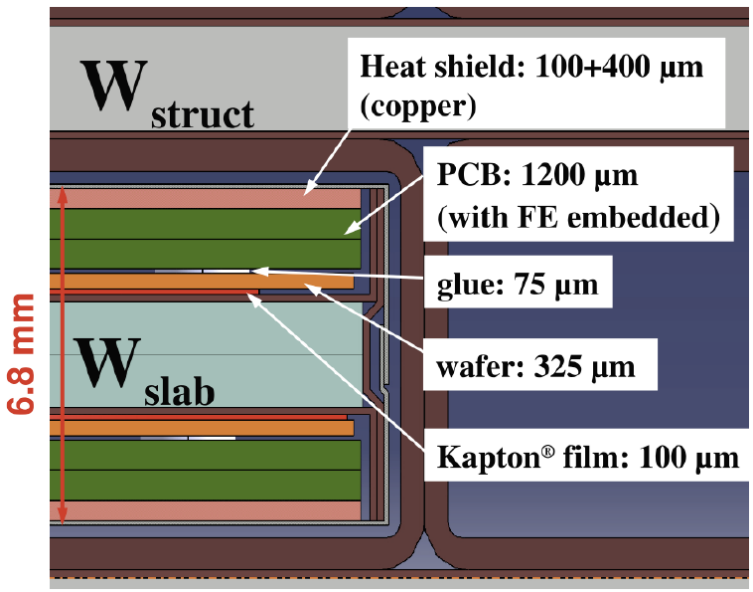
R $\sim$1.8 m (?), thickness $\sim$20 cm
For 30 layers:
$\sim$2600 m^2 Si, $\sim 10^8$ channels, $\sim$130 t W
Modular design, barrel = 8x5 modules, no projective cracks.



Zoomed view



Prototype: 3/5 of one module.

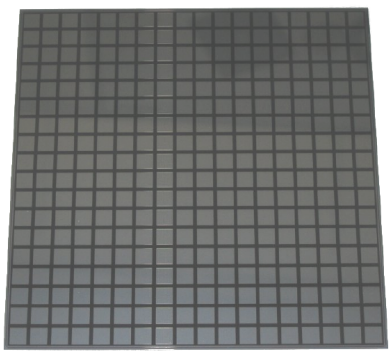


Carbon-fibre support contains every second W plate.

2 PCBs of embedded front end electronics with glued 16x16 sensors are on both sides of other W plates.

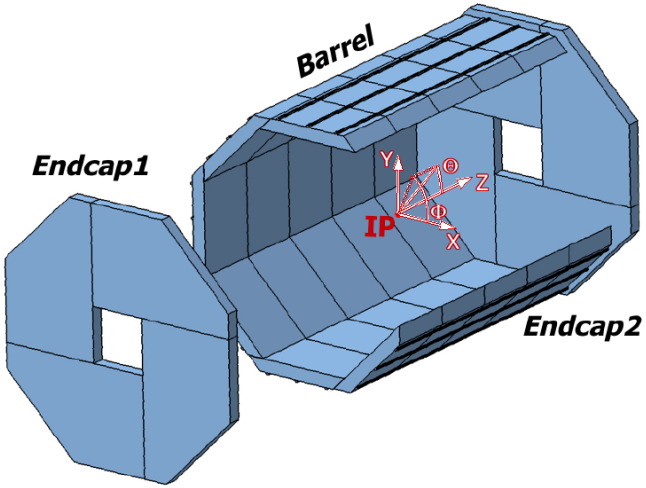
1 barrel module = 5 x 15 slabs
1 slab = 8. . . 13 x Active Sensor Units,
1 ASU = 4 x Si sensors = 1024 chan.

HV, LV, signal cables, water cooling run in 3 cm ECAL - HCAL gap, exit between barrel - endcap.

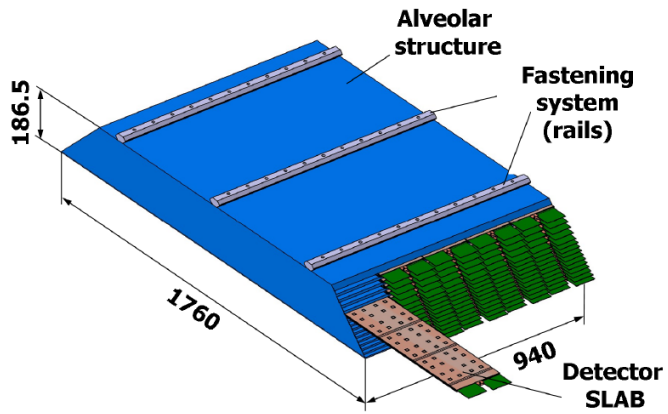


Hamamatsu Si sensor

Possible changes



For 30 layers: $\sim$2600 m^2 Si, $\sim 10^8$ channels, $\sim$130 t W

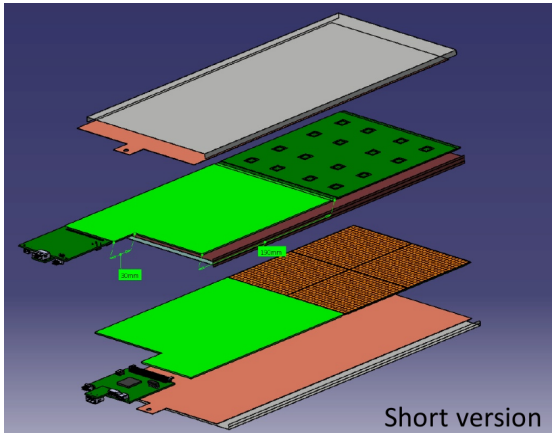


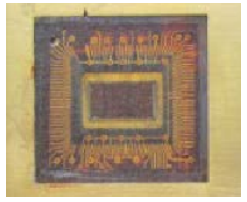
- R = 1.8 m - can be reduced? Compensation by higher B field and granularity in HCAL (RPC, micromegas) and ECAL? Big impact on full ILD cost.
- Endcaps will also contain endcap "rings" close to beam pipe. No detailed design yet, high e^+e^- backgrounds from beam-strahlung ($\lesssim$ 170 hits/chip/spill)
- 30 layers $\rightarrow$ 20?
- ECAL thickness:
  $\rightarrow$ 19 cm for naked die chips inside 1.2 mm PCB (difficult),
  $\rightarrow$ $\sim$23 cm for BGA packaging. For 20 layers: $\sim$19 cm.
  Cu 0.5 mm thermal drain in barrel: can be thinner (slab end: ΔT=2.2°C)?

Thickness of PCB + embedded electronics

Two options:

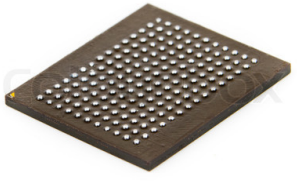
- ”extreme” design (difficult):
  - naked die chips in PCB hollows, bonding connection
  - PCB with 8 layers, 1% flatness
  - only 1 mm thick (slab 7 mm)

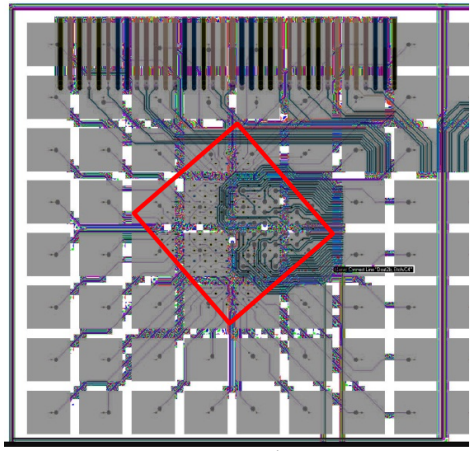




- conservative design (currently preferred, next step in R&D):
  - BGA chip packaging
  - 2.5 mm thick (slab 10 mm)

$\rightarrow$ 2-3 times less length of chip-cell traces w.r.t. current prototype

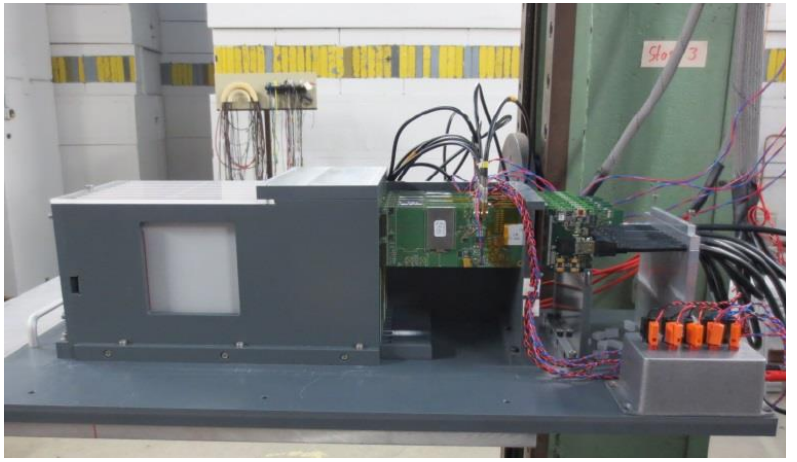




Current technological prototype

10 (2 failed) single layer slabs in TB Feb'13
1 slab = 1/4 ASU = 1 Si sensor = 256 chan.
Embedded electronics, modular design, close to final. Still, relaxed constraints on thickness.

Next steps: reduce thickness (with BGA) and increase area



Long slab prototyping is under way.
N x (1/4) ASUs are connected by Kapton cables. Long transmission lines (1.5 - 2.5 m).

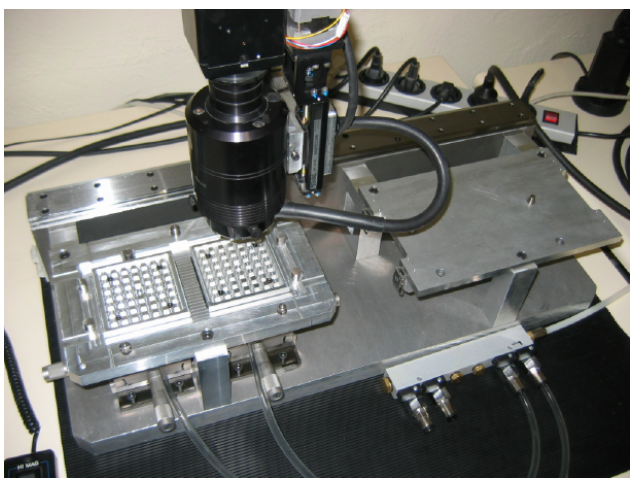
ILD barrel slab = 8 x 4 x (make thinner) $\rightarrow$

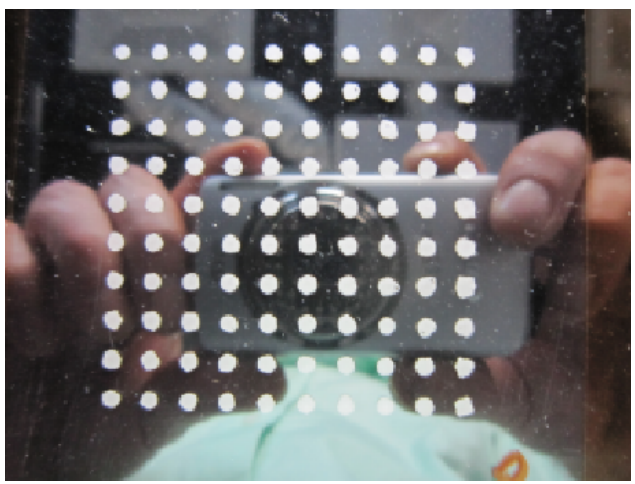
Si sensor gluing robot, here in LPNHE

Si is glued with conductive epoxy to PCB. $\sim 10^8$ glue dots in ILD ECAL.

Epotek 4110 epoxy
glue dot deposit time 0.5 sec
polymerisation 12 hours
resistance <80 $m\Omega$

LPNHE robot will be shown today at 17:00-18:00.

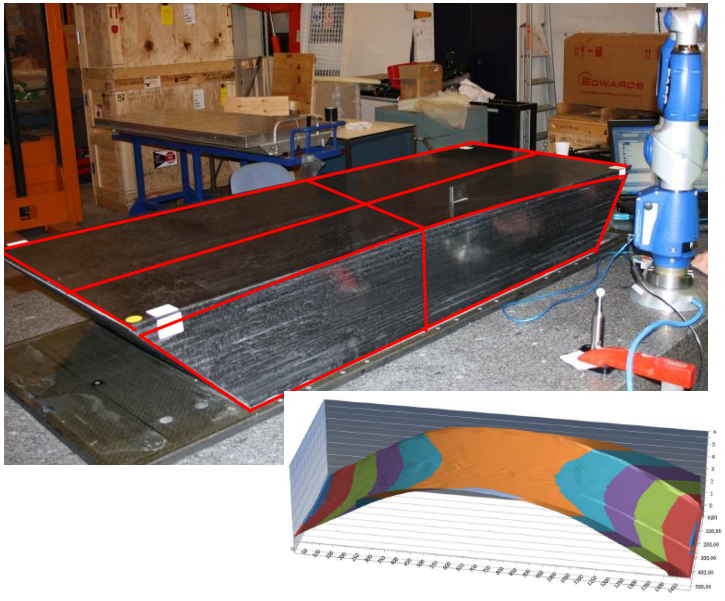




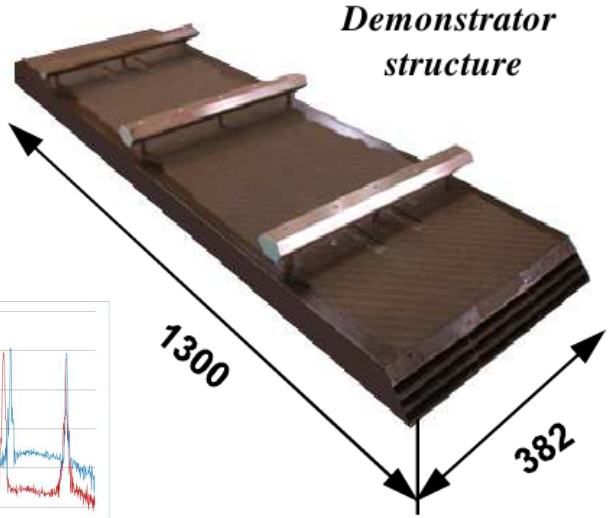
Mechanical structures

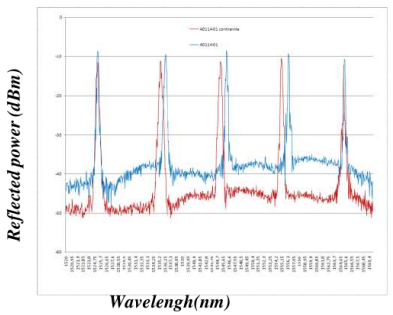
Prototype: 3/5 of one module, $\sim$ 600 kg.
Separately built layers “cooked” together.
Simulated mechanically & thermally.

	Exp.,mm	Measured
Height	552.78	552.65 ± 0.05
Width	205.3	$205^{+5.28}_{-0}$

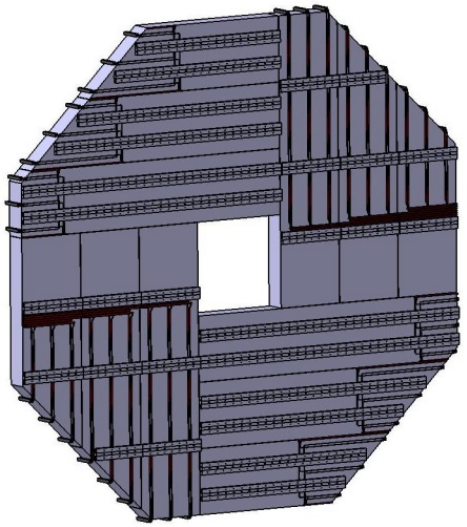


Another prototype: 60 kg alveolar structure with 3 slots with molded Bragg grating fibers.
Plan: precisely measure deformations under stress by measuring frequency shift of light reflected by fiber.

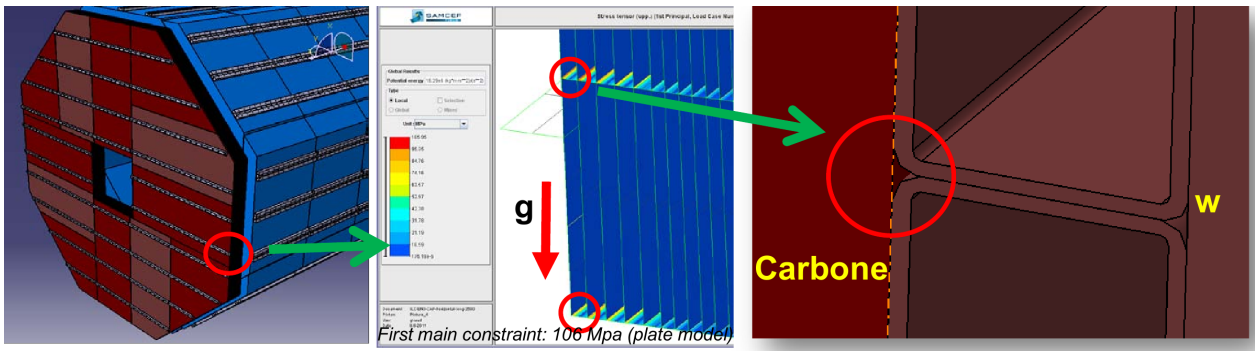




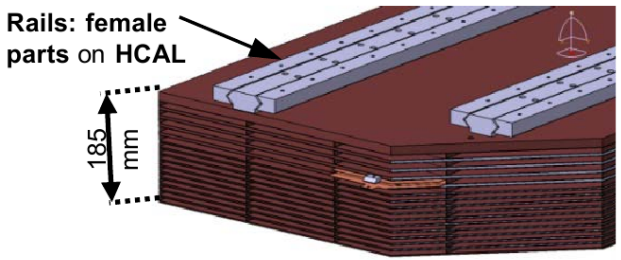
Endcaps and rails



Endcap: W lies on thin walls of carbon-fiber structure. Lot's of simulations and tests.



ECAL hangs on rails attached to HCAL. 3D design & tests of 30 mm thick double row rails, optimization of positioning.

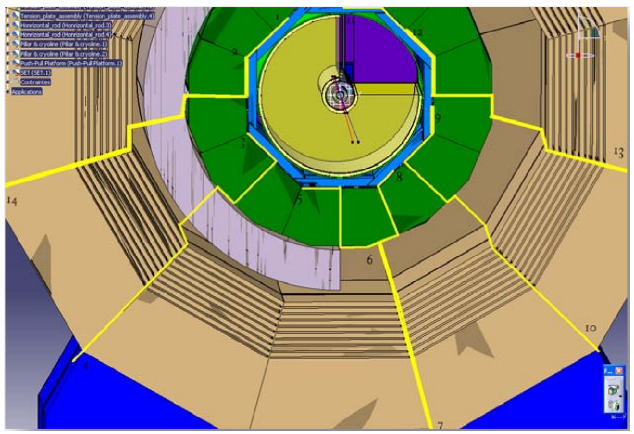


Power pulsing and cooling

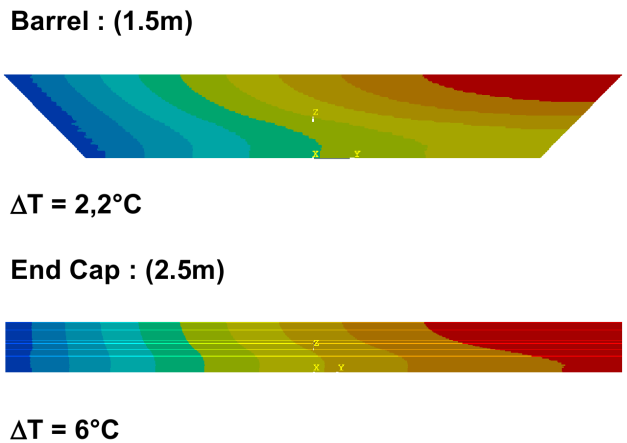
With "power pulsing" (OFF between ILC bunch trains, duty cycle 0.5%): 25 μW / channel $\rightarrow$ 2.5 kW in total within structure (neglecting power dissipated during ON-OFF transition)

First tested in DESY in Feb'13, DAQ performance and interconnections under alternating Lorenz force: Ok.

Heat evacuated: from inside by 0.5 mm (?) copper plane, at module edge with DIFs in ECAL-HCAL gap - by 12-14 mm water pipes; in total: 3-30 kW. Electronics temperature 20-40°C.



Pipes: ΔH = 8 m, ΔP = 0.8 bar, validation tests in fall 2013



Thermal flux simulation

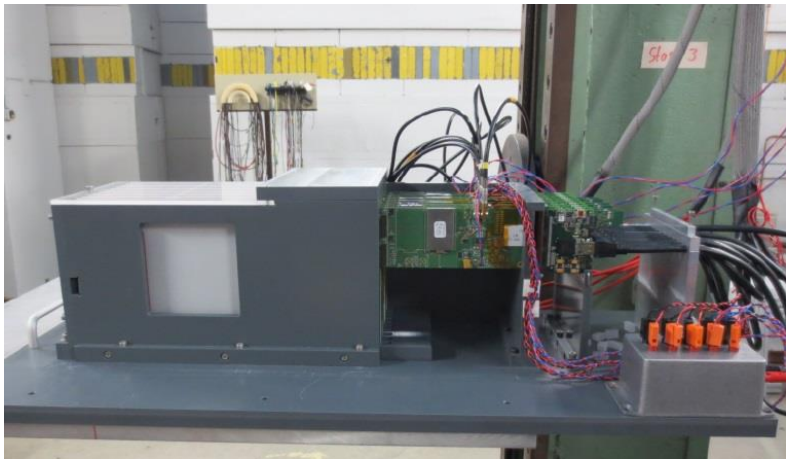
Edge cooling prototype

Topic

Technological prototype

TB Feb'13 achievments

- new DAQ software
- allows 2 LDAs (old soft: 1) + new algorithms (automatic masking / threshold adjustment);
- new DIF firmware, slab modifications
- allow power pulsing



Observed problems

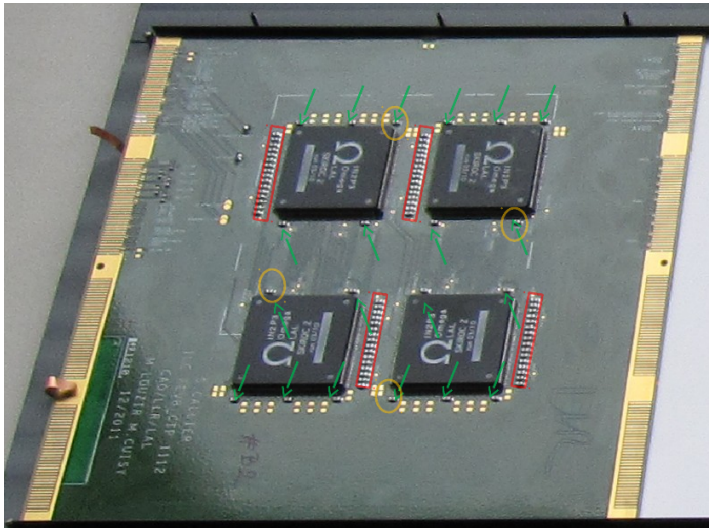
- many fake triggers
  Trigger in bunch BX can be followed by retriggerings in BX+1,+2...+14.
  Plane events with many (up to 100%) hits = avalanche of retriggers
  $\rightarrow$ high trigger thresholds ($\sim$1 MIP), noisy data, dead time after filling up SKIROC memory
- difficulties in DAQ configuration
  $\rightarrow$ need of debugging tools, verification after configuration

Improvements in technological prototype

Retriggerings and plane events are clearly caused by noise in SKIROC power lines. About 1/10 of analog power noise is propagated to SKIROC input.

Two improvements:

- decoupling capacitors (of two types to cover large range of frequencies) - all 8 slabs in LLR modified, big improvement
  (capacitors on photo: orange - add, green - change, red - remove for power pulsing)



- bug discovered: one analog power line was connected to digital
  $\rightarrow$ fixed in one slab (SKIROC "pin clipping"), also helps

Two new slabs are in production. Both improvements will be implemented (plus resistors for individual adjustment of thresholds per channel).

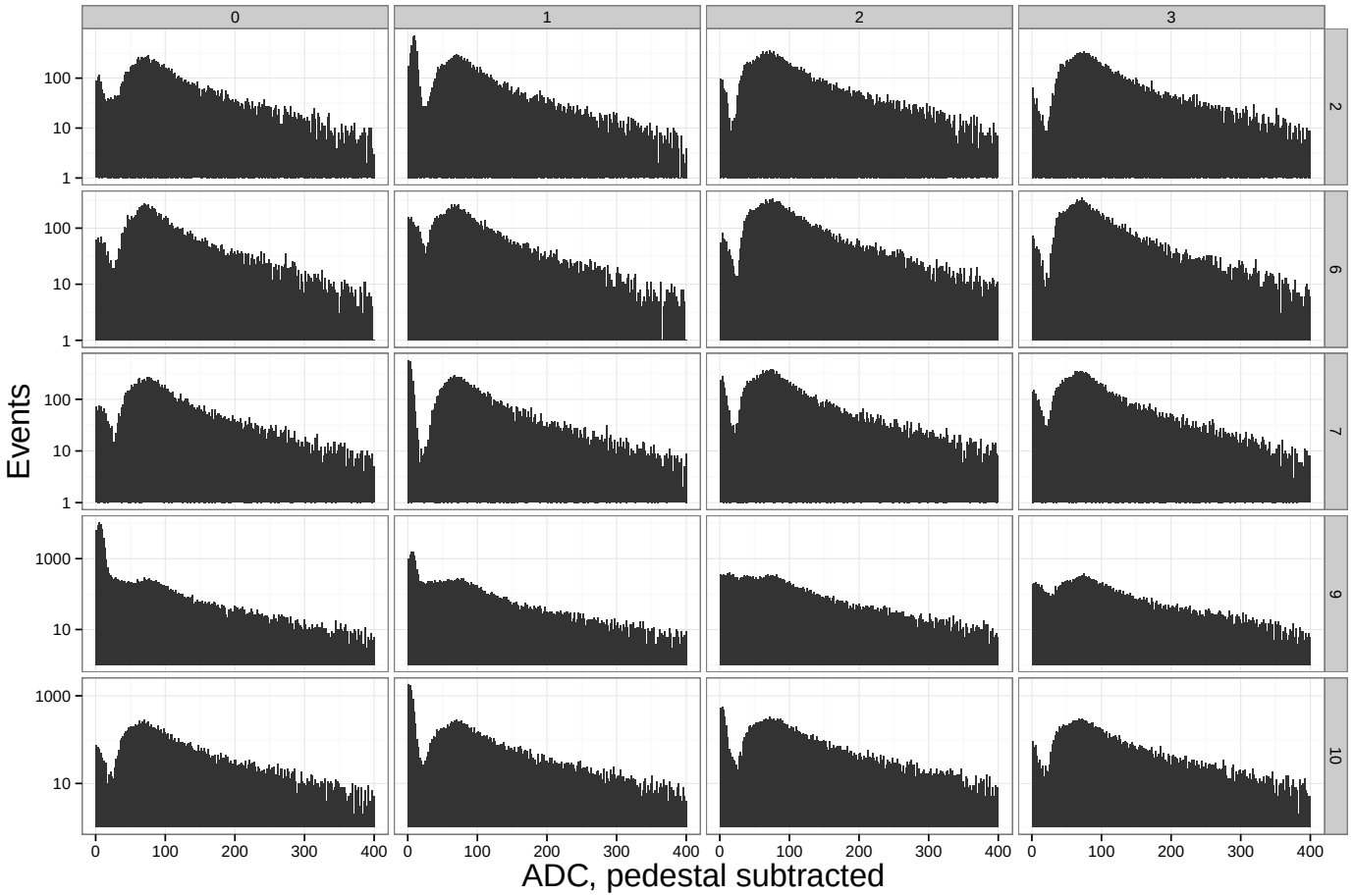
Long term: Jean-Baptiste Cizel (following Remi's advice) studies a modification for SKIROC3 to suppress sensitivity to power noise by 10.

Cosmic muons (May runs in LLR)

Low rate, requires duty cycle close to 100%. In the past, power line noise filled up SKIROC memory before first muon arrived$\rightarrow$ no cosmic signals.

4 slabs with decoupling C and one without (#9) but "pin clipped" (worse).

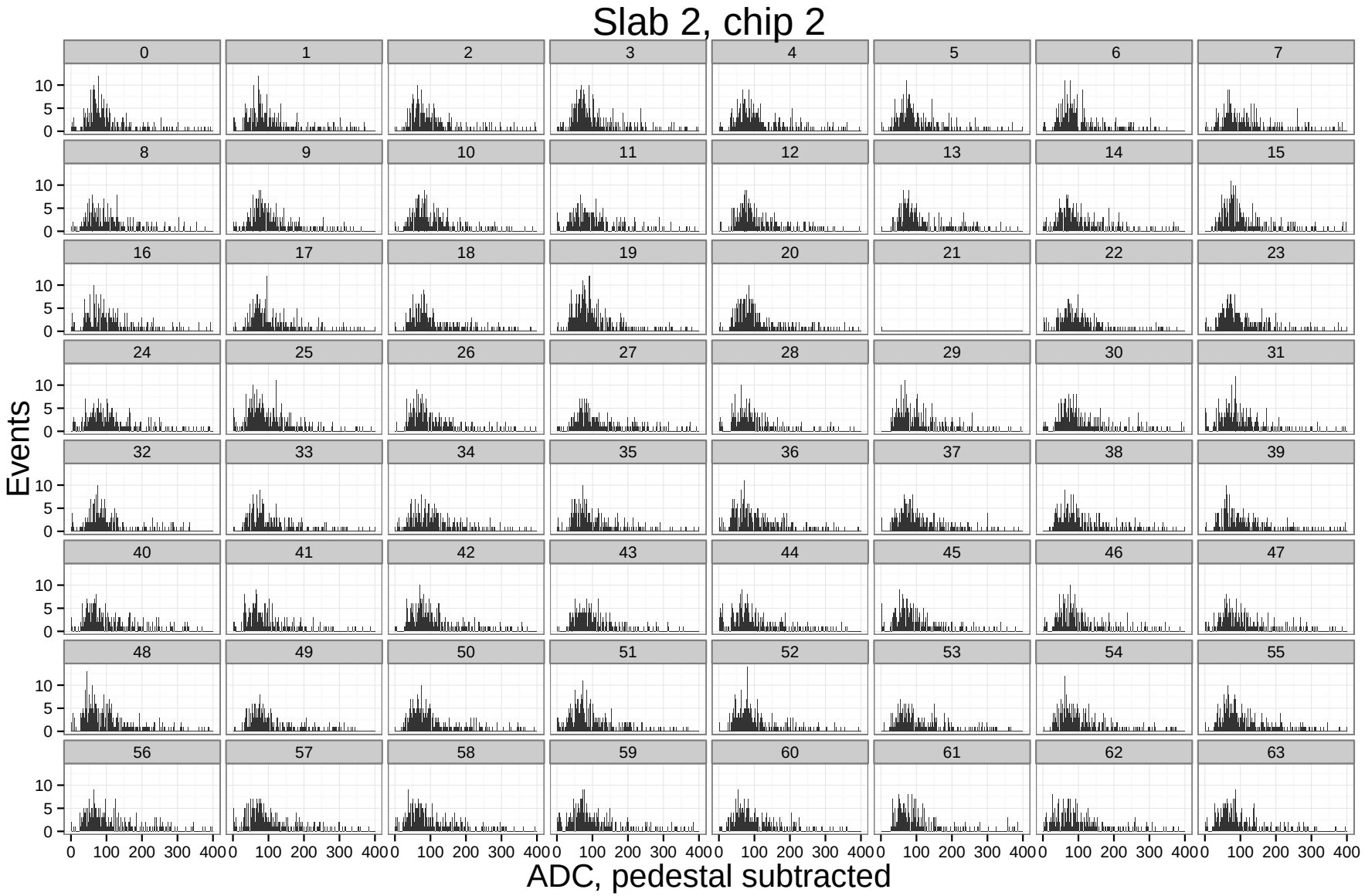
Threshold $\sim$0.5$\times$MIP = 35 ADC (1.2 pF gain). Sum over channels for 4 chips X 5 slabs



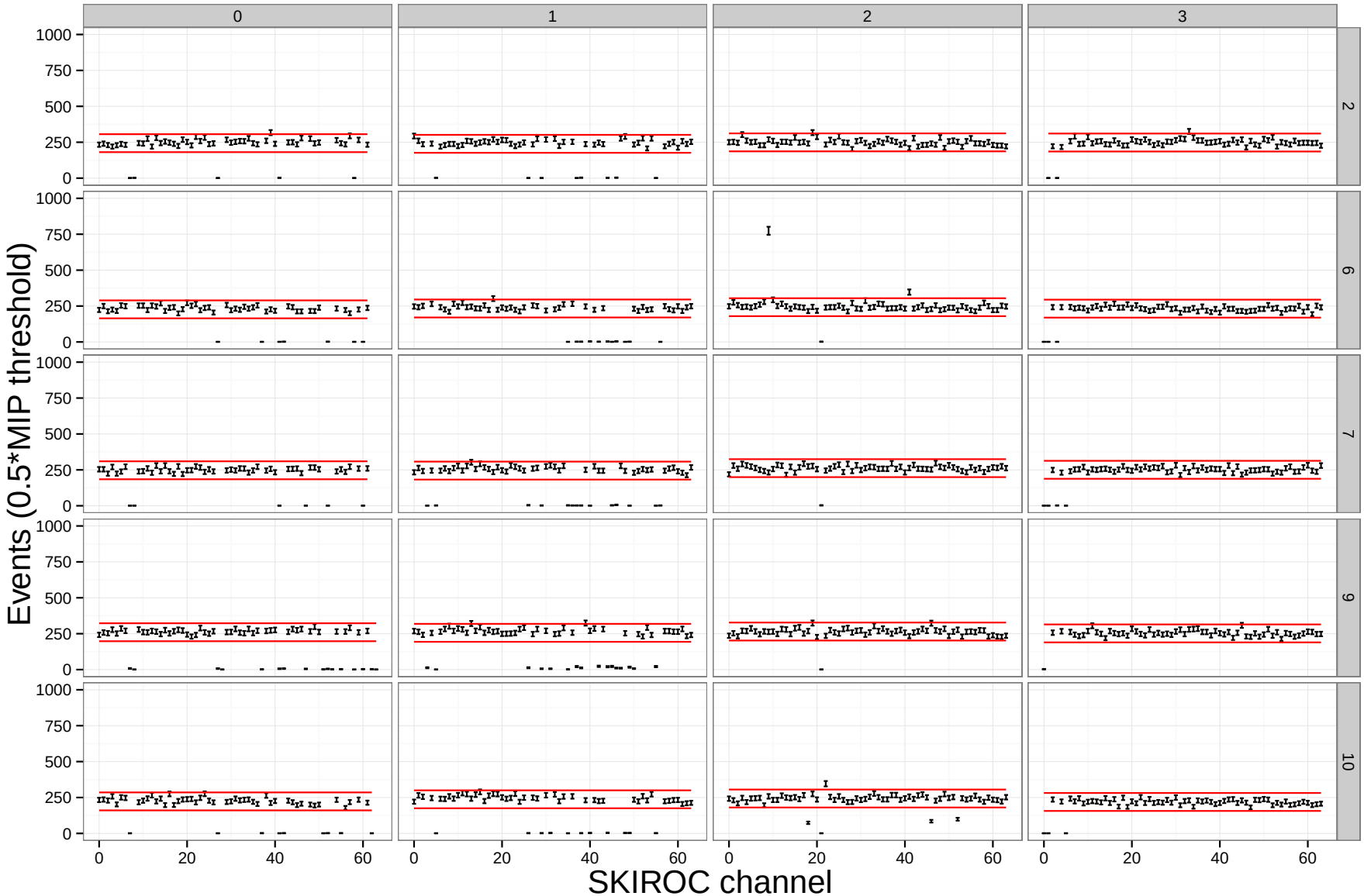
Channels connected to 2 or 4 cells are masked plus $\sim$5% of channels, probably picking up digital signals

Muons (cont.)

In one week enough statistics to calibrate channels individually (50 K muons per slab).



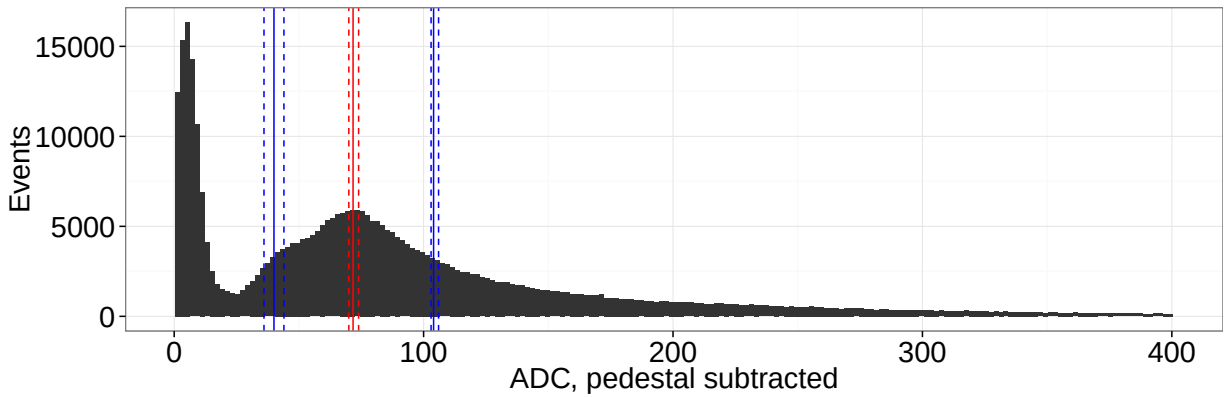
About 250 muons per cell above 0.5×MIP



Exclude channels with number of events N outside $\pm 4\sqrt{<N>}$ band

Muons, most probable signal

For simplicity, take truncated mean over 55% of lower data in ADC>40 range (red line = mean over band within blue lines). Fit to Landau distribution convolved with resolution is more precise, but sometimes may fail to converge (with >1000 channels). Also note effect of “S-curve” trigger efficiency at the left tail.

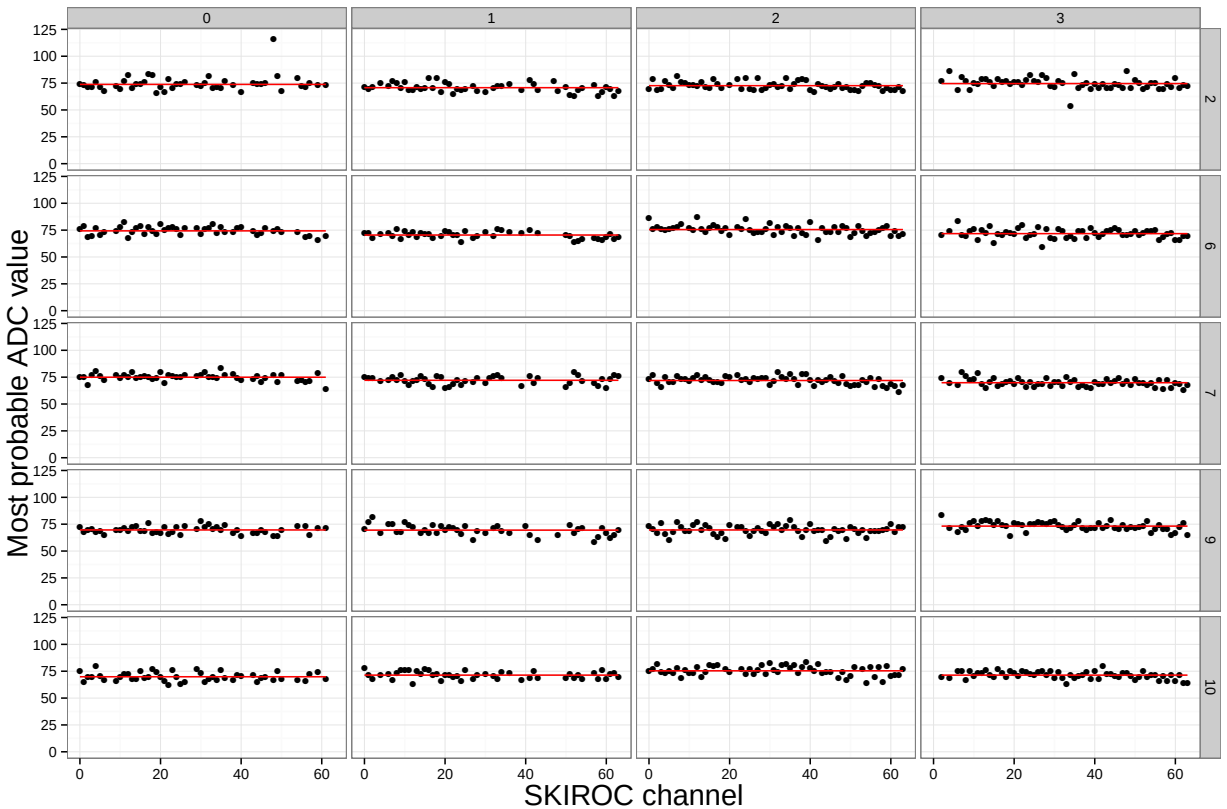


55% truncation is chosen to get the most probable value (MPV) at the right position.
Ideally, the lower threshold ADC>40 should cut a fixed fraction of the lower signal, then truncated mean = MPV. If position is fixed at 40, the fraction varies and there is a bias. ADC>40 cuts more for lower gain channels, effectively increasing truncated mean. The effect for 10% lower gain is equivalent to setting 10% higher threshold (right blue dashed lines on picture) for average gain. Truncated mean is then found to be shifted by 2.7%. Squeezing this picture by 10% lowers MPV by 10% (as assumed), sets threshold back to 40, but lowers truncated mean only by 7.3%. In the following, the bias of truncated mean is thus compensated by enhancing its variations by 1/0.73. The picture above is assumed to be one channel spectrum, ie. we neglected a smearing caused by summing up many channels with slightly different gains.
"S-curve" trigger efficiency is difficult to measure. If it is the same for all channels, for lower gains the left tail is more suppressed and the truncated mean is shifted to the right (again "compensation"). Our estimation of MPV spread is thus a little "optimistic".

Muons, most probable signal

In %	spread	stat. error	above stat.	physical prototype
All	6.1	∼5.1	∼3.3	∼5
Within chip	5.5	∼5.1	∼2.1	
Between chips	2.9	∼0.7	∼2.8	

Stat. error estimation: randomly assign slabs/chips/channels to events and repeat procedure. Not calibrated channels - 15.6% (1.1% without reasonable MIP, 14.5% masked channels, out of which 9.4% with multiple cells)



1.1% of channels with number of events N outside $\pm 4\sqrt{<N>}$ band or with MPV above 100.

Calibration and quality control for mass production

Si signal depends only on depletion region thickness $\rightarrow$ no dependence on external factors like temperature has been observed in physical prototype. Robustness and stability over years at % level (variations due to cable length change etc.)

Calibration spread $\sim$ 5%.

Mass production: possibly, one calibration only. Muon beam and cosmics. More steps for sensor / front end electronics validation to detect failures early, before final assembly.

ASIC front end chip linearity range: 1...1500 MIPs. A few % non-linearity at lower end due to shaper timing dependence on signal amplitude. Can be calibrated with electrical charge injection.

DAQ electronics: GigaDCC

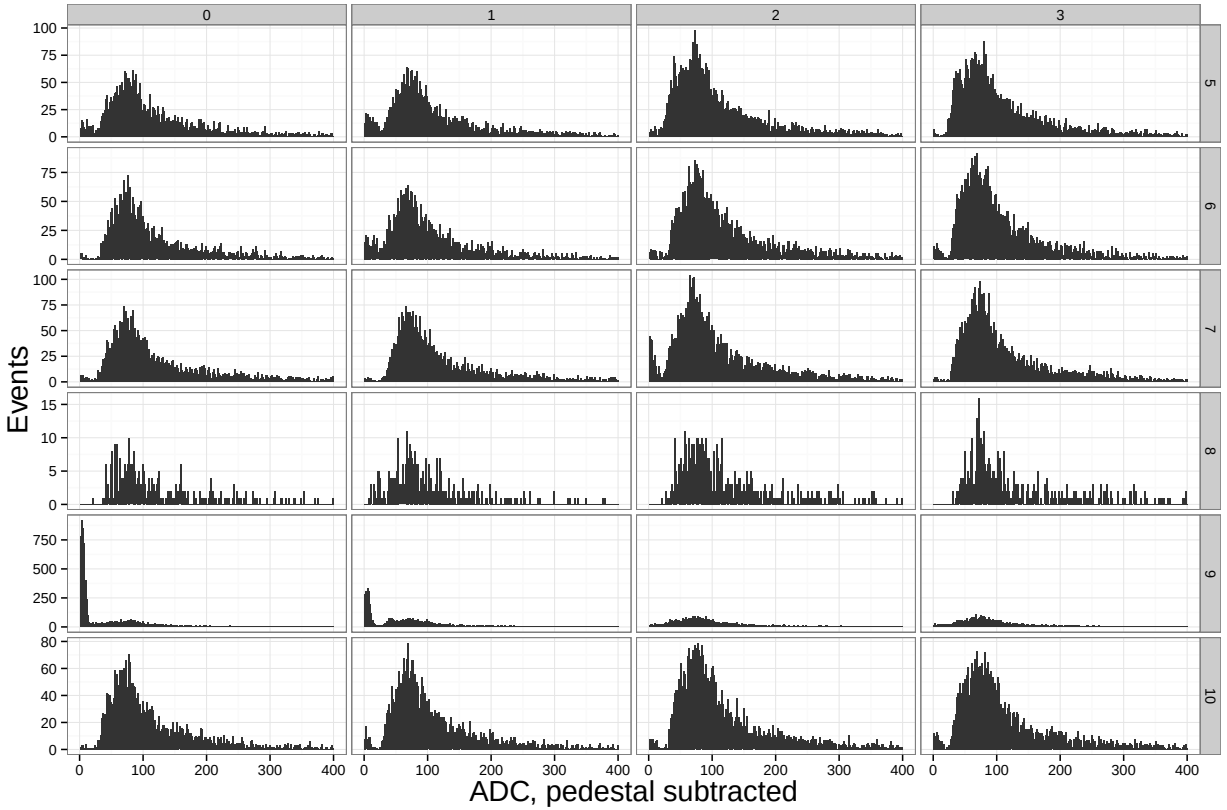
Link Data Agregator (LDA):

- difficult to maintain firmware (Xilinx licence is needed for Ethernet interface, current version is obsolete; understanidng of packet management requires reverse engineering)
- not sufficiently reliable (grounding, shielding, connections)

Gigabit Data Concentrator Card (GDCC) will replace LDA. Same software, reuse of some hardware parts.

DAQ electronics: GDCC (cont.)

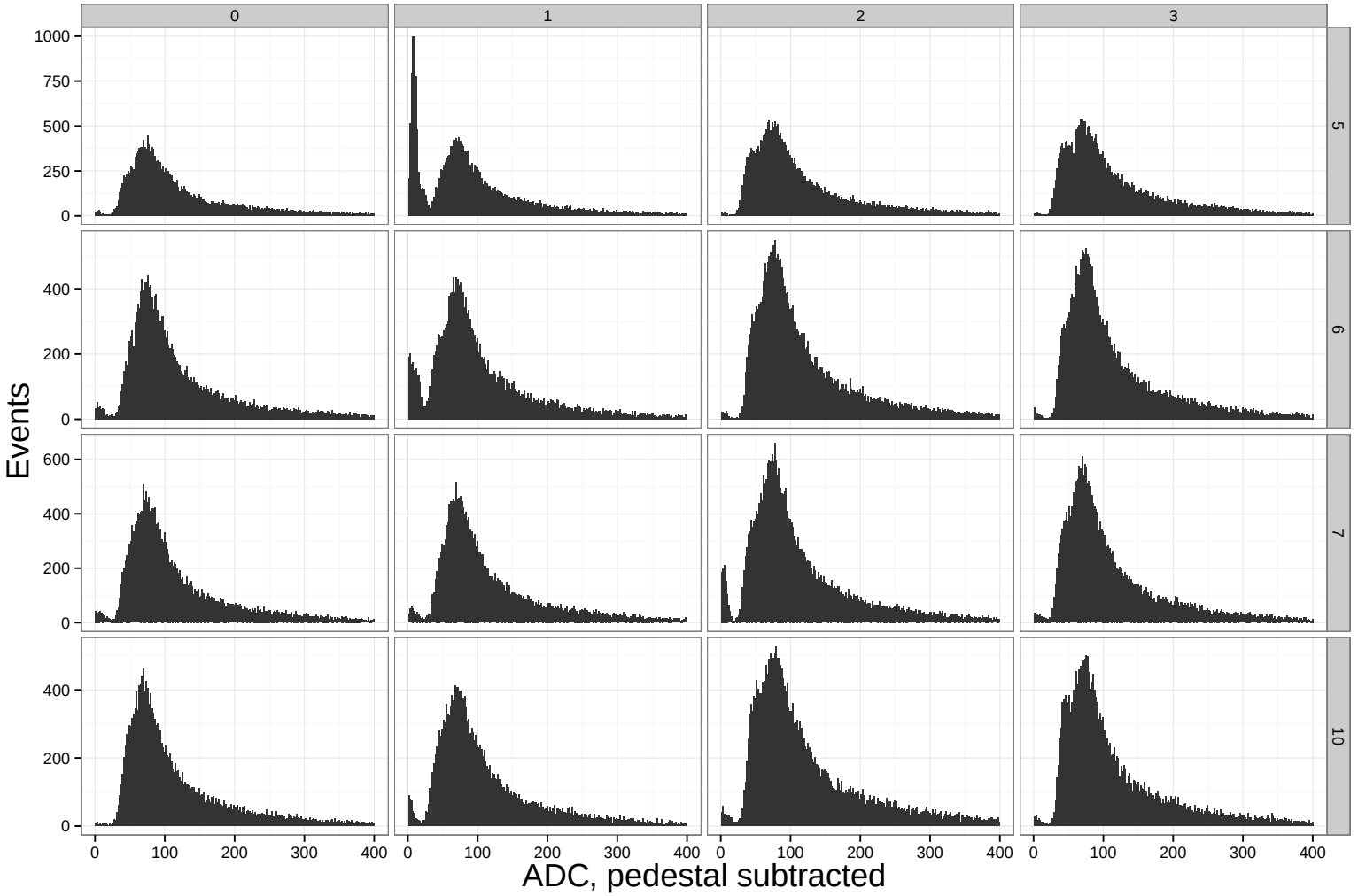
First iteration of tests has been performed in February, a few bugs resolved.
Main source of packet losses (1-2%, bug in LDA) is discovered and understood.
Second iteration in May. First run with all 6 GDCC channels (cosmics)



Slab 9 had no decoupling C, but "pin clipped" (more noise). Slab 8 was sending data only in the first part of the run.

DAQ electronics: GDCC (cont.)

Run with spill rate 50 Hz (!)



Plan: test GDCC in TB Jul'13, decision on production in September.

Topic

DESY beam test in Jul'13

Schedule

July 1-3: machine days

morning July 4 - 8:00 July 15: SiW, ScW beam tests, electrons 1-5 GeV

Preliminary ("maximal") SiW program

end of June: 1 week calibration with cosmics

July 3: installation

With DESY beam (about 1 week):

- Calibration without W
  - SKIROC trigger delay scan
  - find max spill rate (+duty cycle for at least 15 events / spill)
  - LDA/GDCC synchronization
  - choose trigger thresholds / masks
  - position scan $\times$ SKIROC gain scan
- Showers with 10 layers, 4.2mm W = 12 X_0
  - energy scan
  - same in continuous (not power-pulsed) mode
  - SKIROC gain scan (eg. for two points: 1.2, 6pF)
- Software improvement
- GDCC tests (if Ok, always run with one GDCC)
- Combined run with ScW (w/o synchronization?)

DESY beam test in Jul'13 (cont.)

To be done:

- decoupling capacitors for two slabs in LAL (8 in LLR are modified)
- 2 new slabs with all decoupling caps, "pin clipping", increased range of threshold adjustment per channel. 12 slabs in total (10 slots in mechanical structure, 2 spares), 2 LDAs. Possibly: one new PC in rack.
- one tested GDCC
- mechanics: 2.1, 4.2 or 6.3 mm of W in any slot (by June 20)
- reporting for ANR project

Topic

Status and plans

- Scalable modular ECAL design with high level of industrialization
- Currently, 10 prototyping slabs, 2.5K channels $\rightarrow 10^8$ in ILD.
- Slabs should be made thinner with BGA SKIROC + new PCB, longer (x16 in barrel) and wider (x2).
- Automated gluing of Si sensors, $\sim 10^8$ glue dots
- Si sensor improvement (guard ring) and industrialization
- Development and improvement of DAQ electronics (SKIROC2$\rightarrow$ 3, DIF, CCC, LDA$\rightarrow$ GDCC, software)
- Power pulsing looks Ok
- Cooling: can 0.5 mm Cu thermal drain be thinner in barrel? (Taking into account extra power dissipation during ON-OFF power pulsing transition).
  Tests of water loop, heat exchanger.
- Carbon-fiber+W structure. 3/5 of barrel module constructed, precisely measured and well simulated. Plan: validation with Bragg grating fibers. Simulation and tests of carbon-fiber thin walls in endcaps, ECAL rails.

Status and plans (cont.)

- Retriggerings and plane events are due to noise in SKIROC power lines. Decoupling capacitors help a lot.
  Bug fix in next PCB (connection to analog power instead of digital for one power line).
  Jean-Baptiste's modification in SKIROC3 to suppress sensitivity to power noise by $\sim$10.
- With decoupling capacitors: cosmic data are taken routinely. Trigger threshold at $\sim$0.5 MIP. Still, 4-5% of channels connected to one cell should be masked.
- GDCC can take data with all 6 channels and can run at 50 Hz spill frequency. No problems observed (sometimes difficult to configure).

TB Jul'13

- Two new slabs, modification of mechanical structure (1,2,3$\times$2.1 mm W).
- Plan: calibration and showers, continuous and power pulsed modes, different energies, gains. Test GDCC, combined run with ScW.