Test results of an scintillator ecal layer with embedded electronics

Technological prototype of ScEcal

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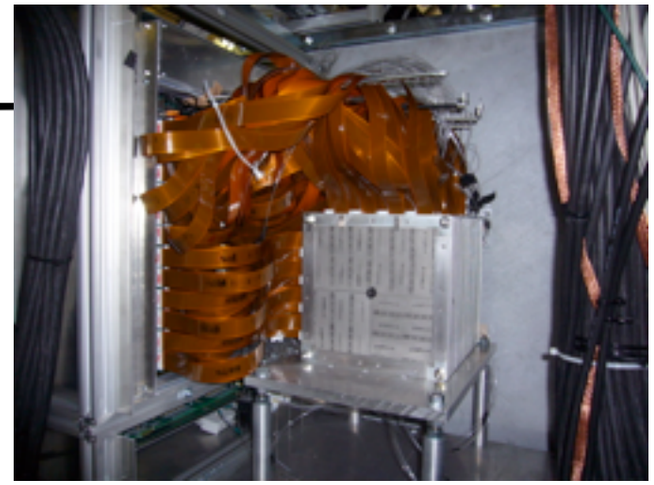
for ScECAL - CALICE-Asia

ECAL meeting @ Paris June/2013

Technological prototype

- From physics prototype to the real calorimeter

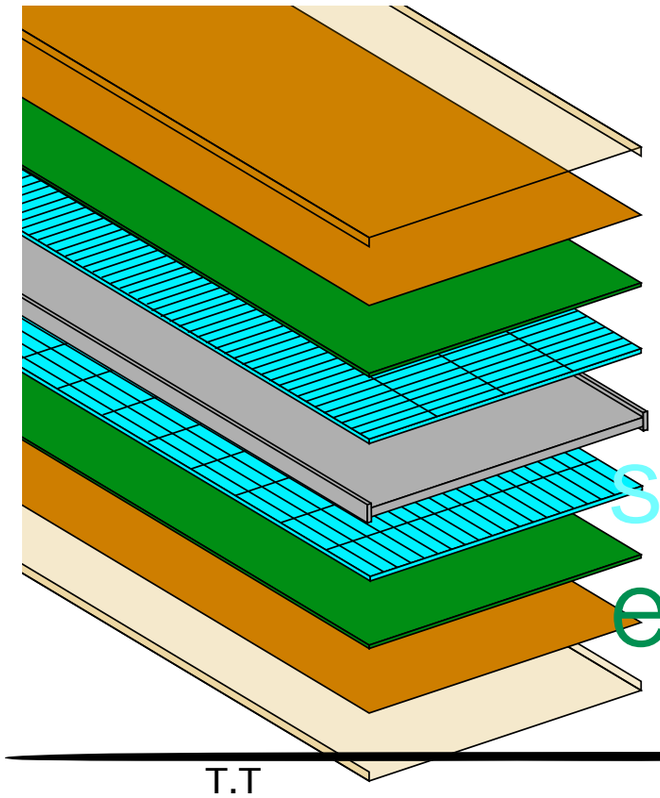


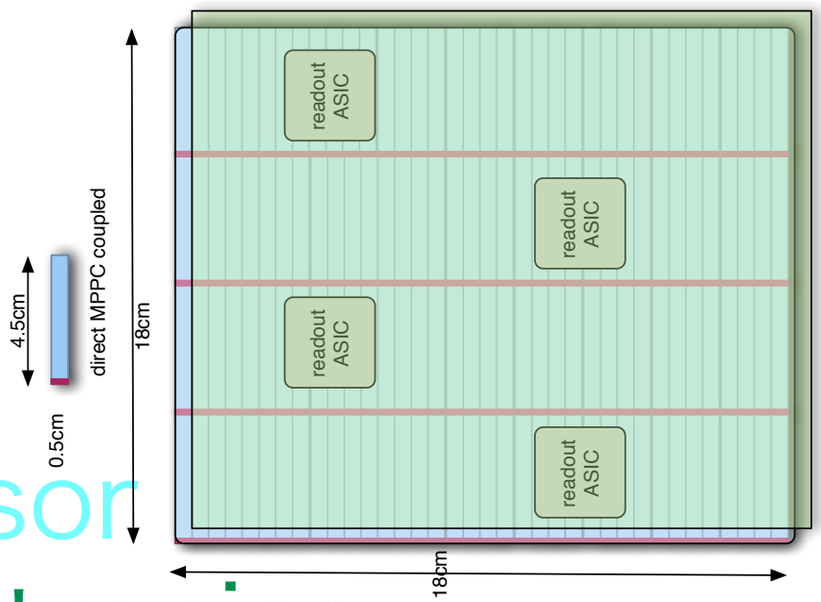
- physics prototype TestBeam2009@FNAL

- Technological prototype

sensor layer **with**

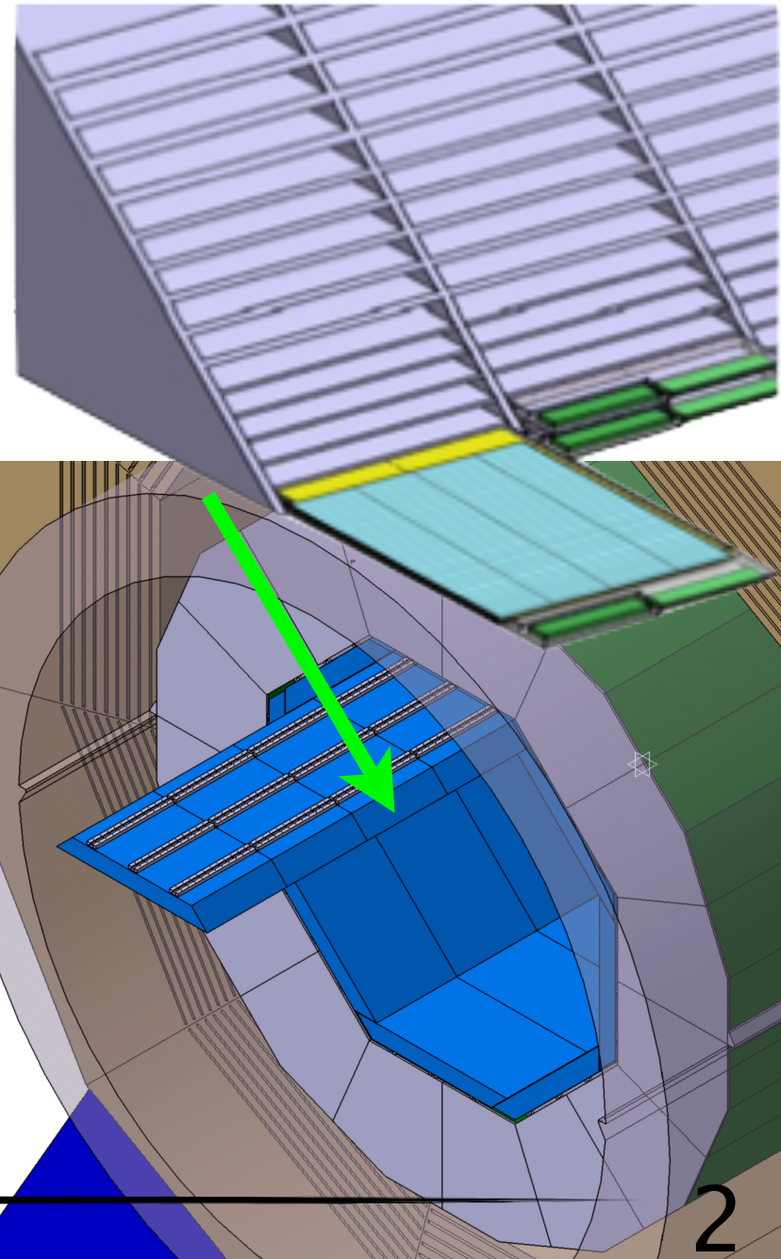
embedded electronics





sensor

electronics

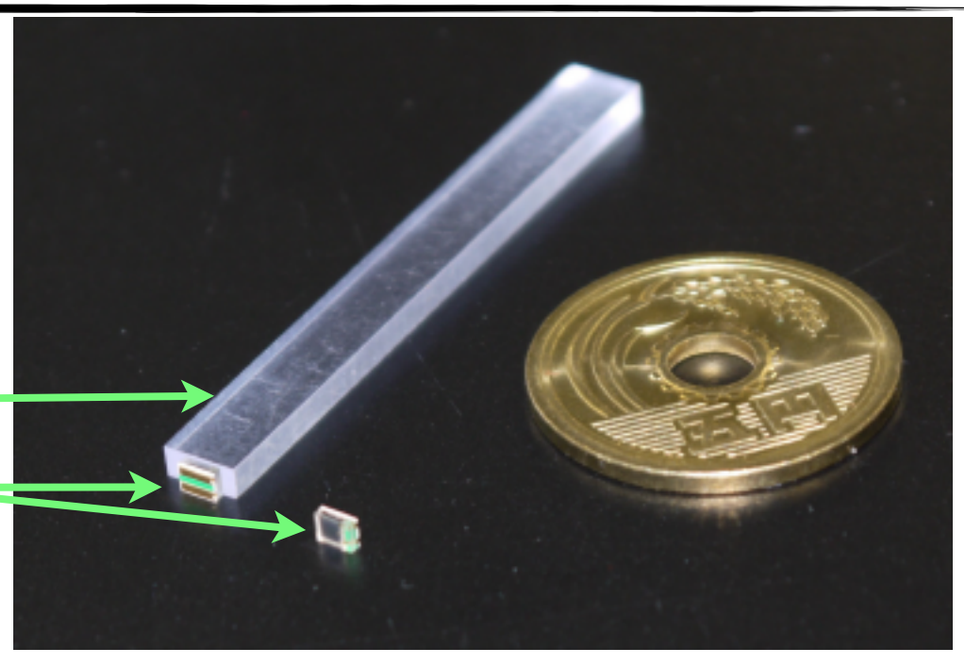


scintillator ECAL Technological prototype : scecal

- sensor = scintillator strip and photo-sensor (MPPC)

scintillator : 2 x 5 x 45 mm^3

MPPC : 1 x 1 mm2 1600pix.
direct coupling without any glue



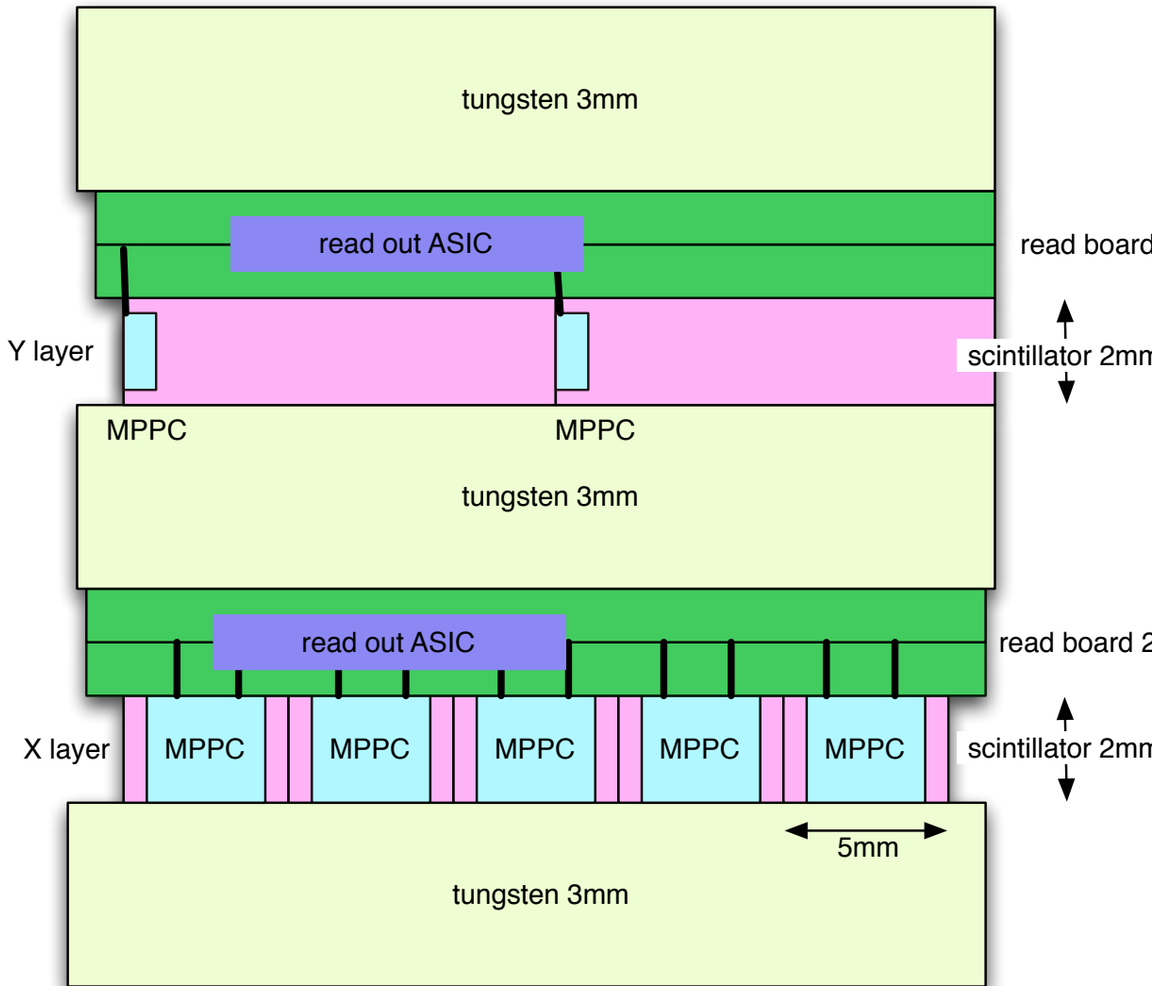
side view of scecal

- embedded electronics = EBU : ECAL Base Unit

ASIC=SPIROC2b

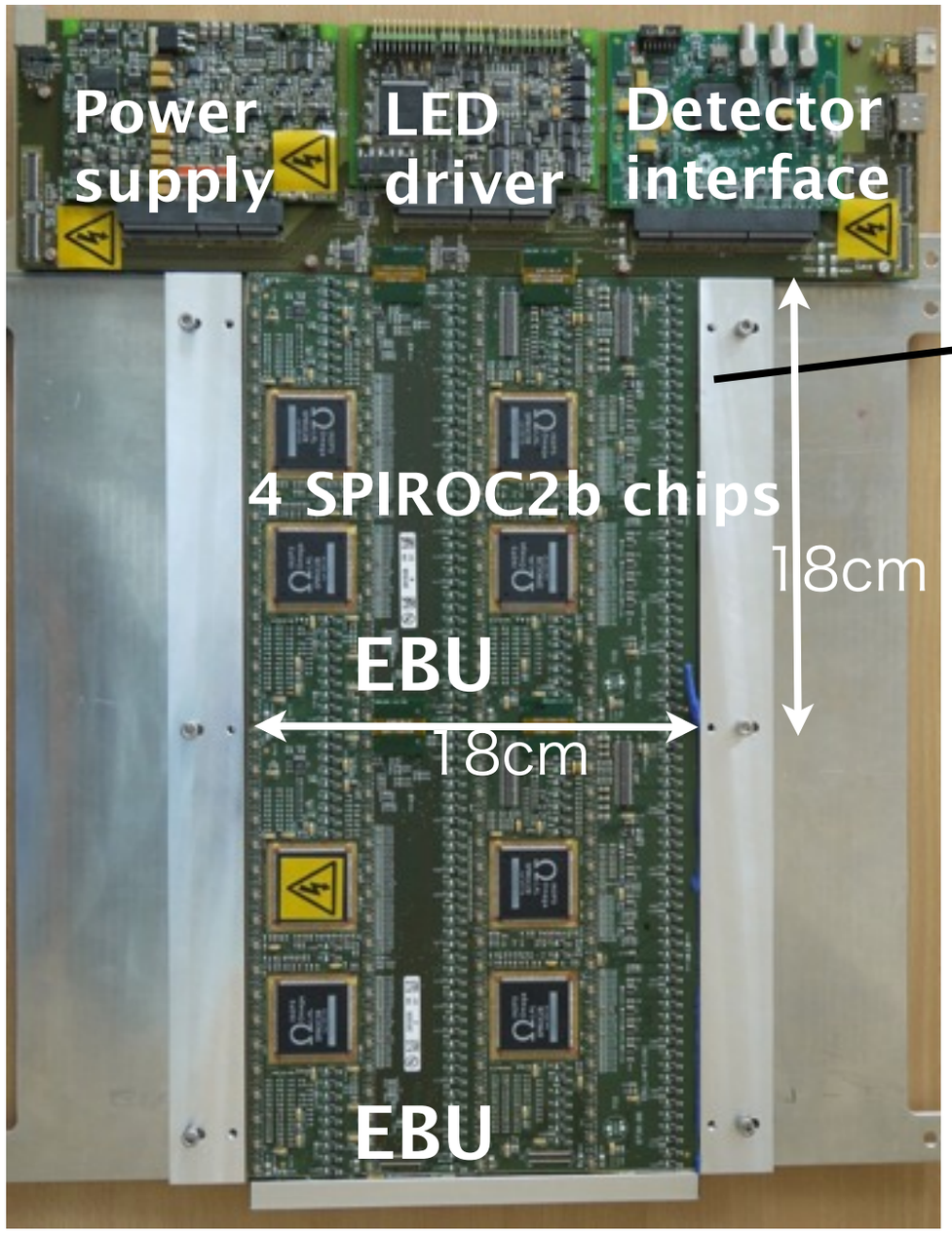
Bias supply
amp. ADC/ TDC
Readout I/F

calibration via LED

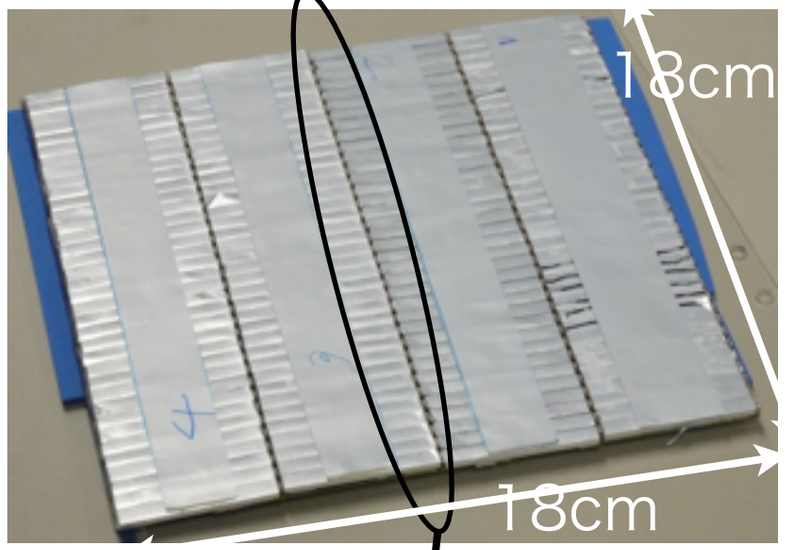


actual ScEcal technological prototype

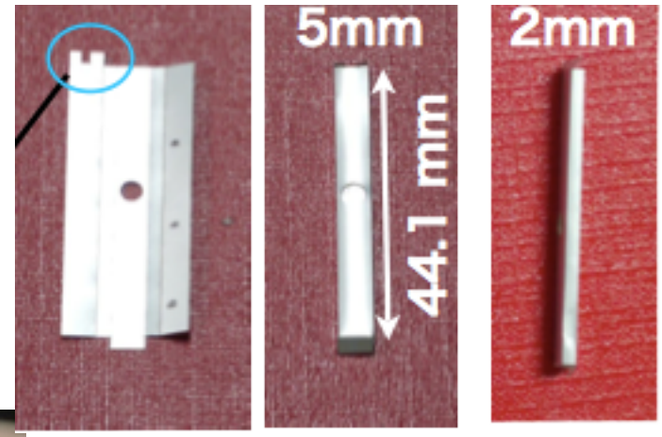
- 4 SPIROCs on a EBU control 144 = 4 x 36 channels.
- board is developed by DESY ~ AHCAL
- detector interface board (DIF)

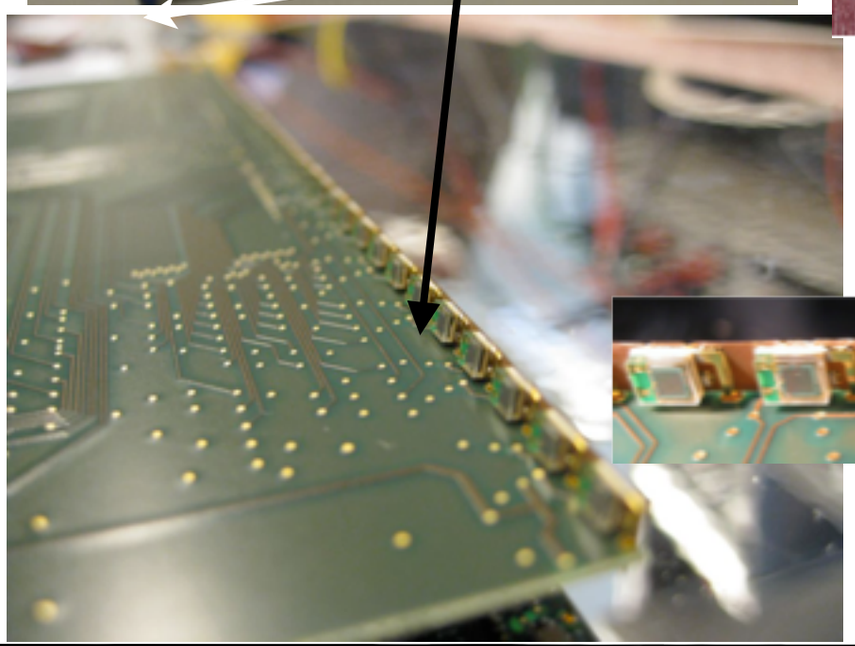


-back side of EBU

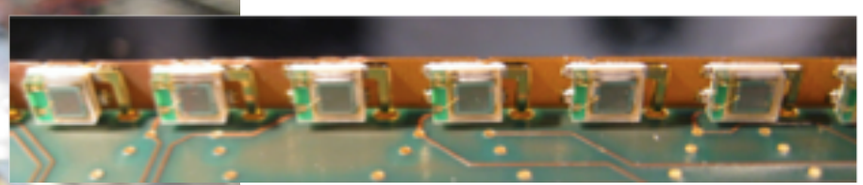


- a scintillator covered by reflector film



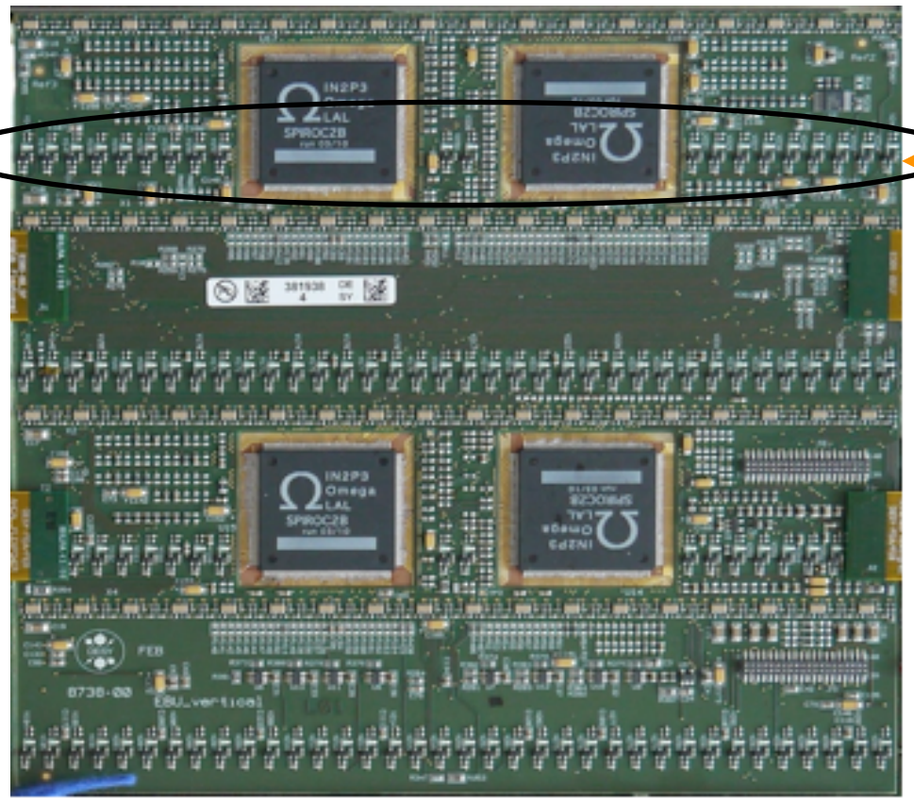


- MPPC ladder

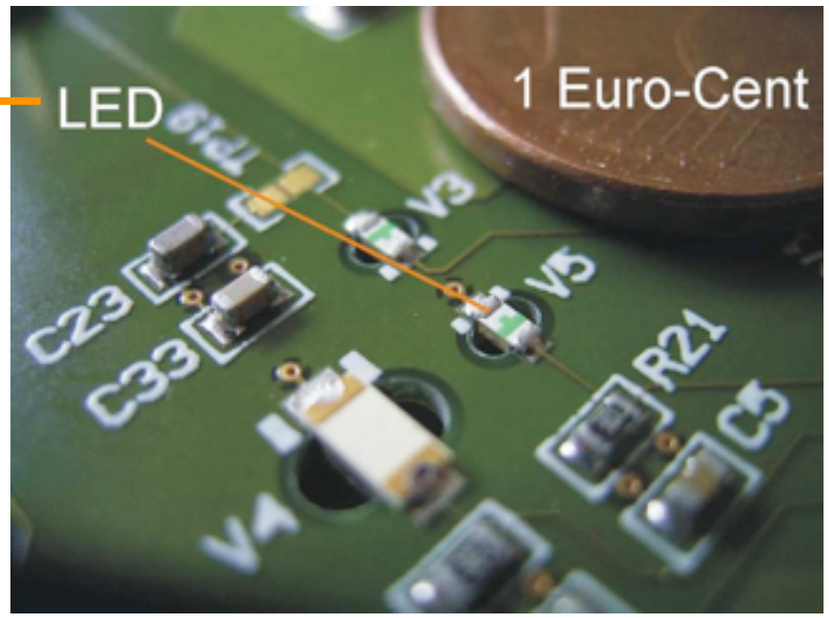


LED calibration and gain monitoring system

a EBU



an LED & its hole to a scintillator

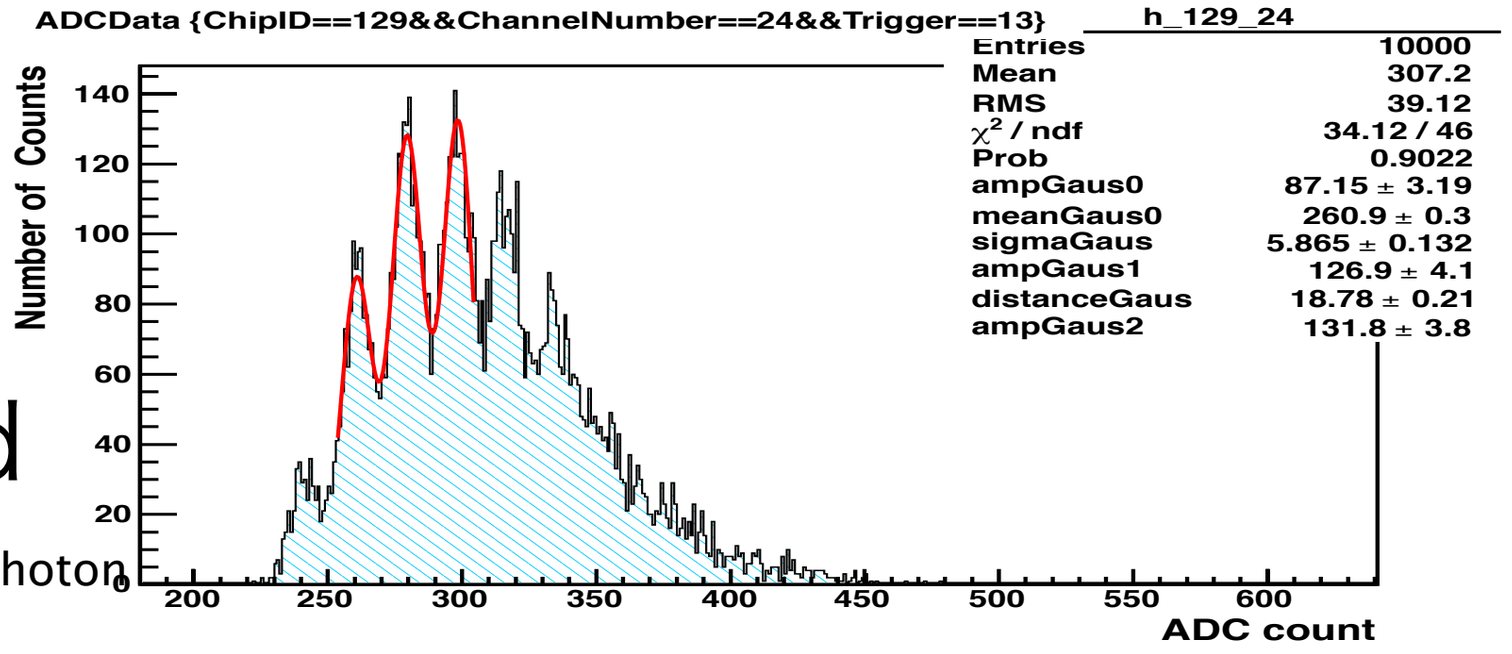


- EBU has LEDs for each channel except on chips or connector

Photo electron peaks are measured by LED lights

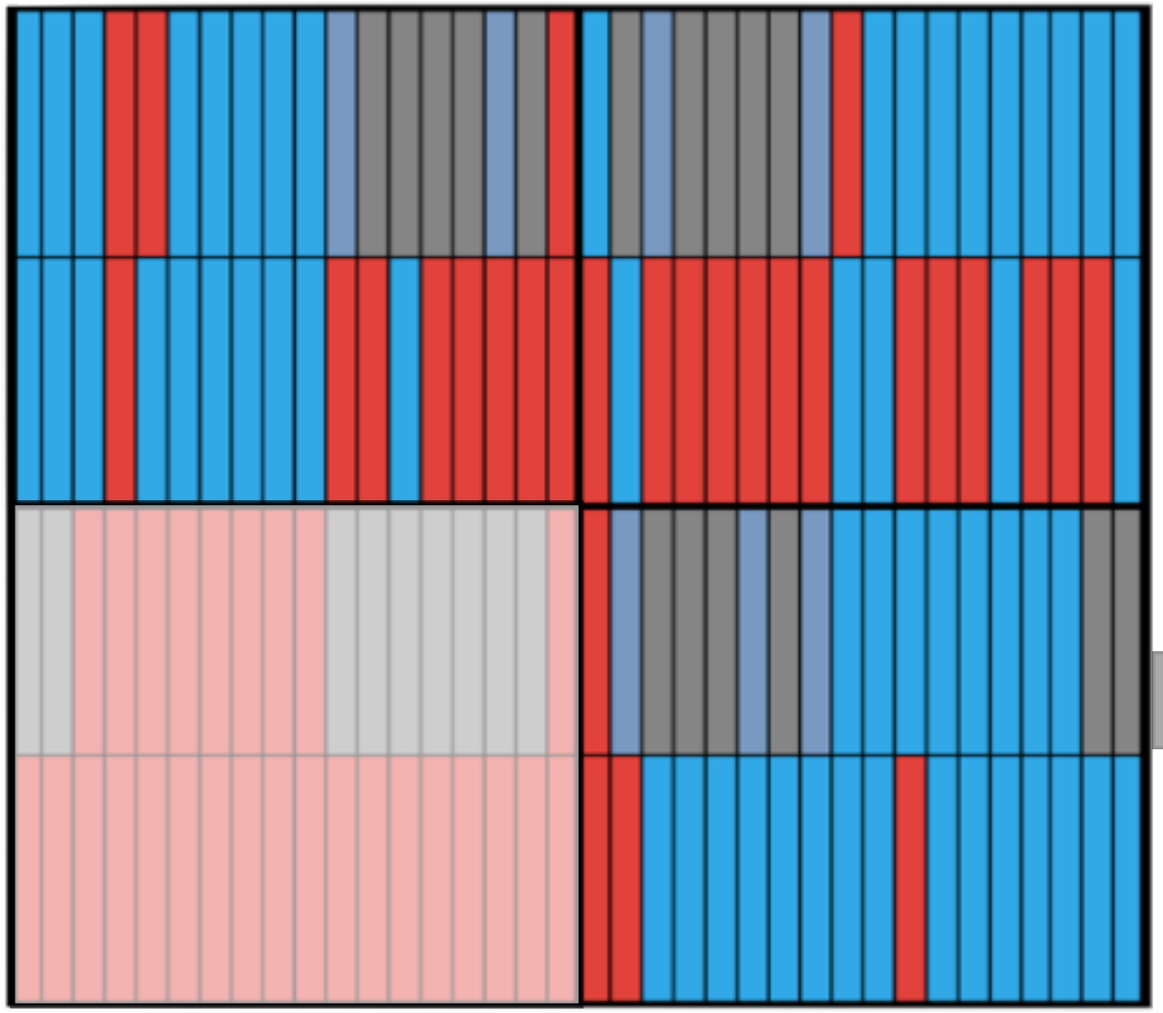
gain monitored

- ADC distribution to measure #photon



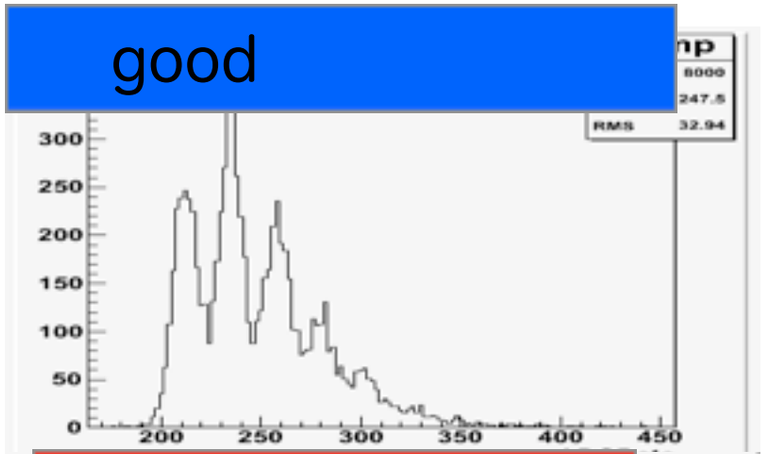
results of LED gain monitoring system

chip 129 chip 130

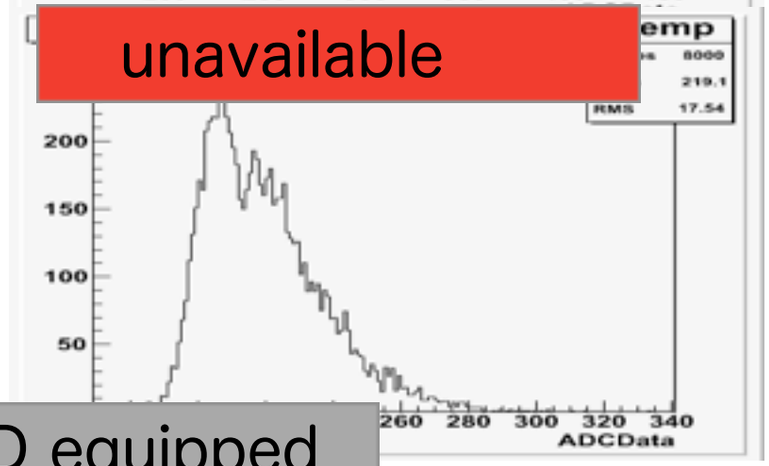


chip 132 chip 131

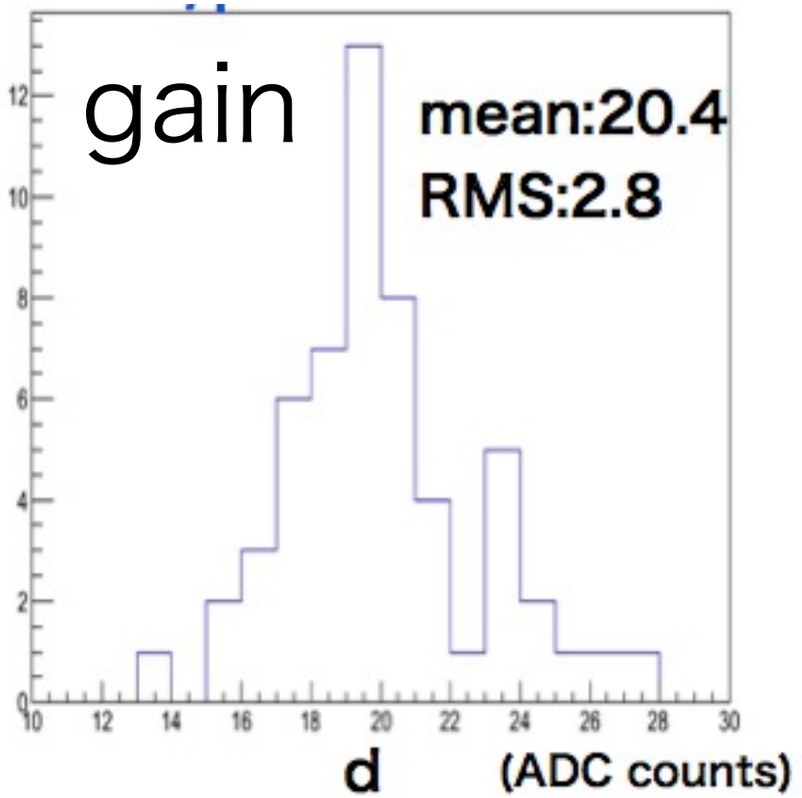
good



unavailable



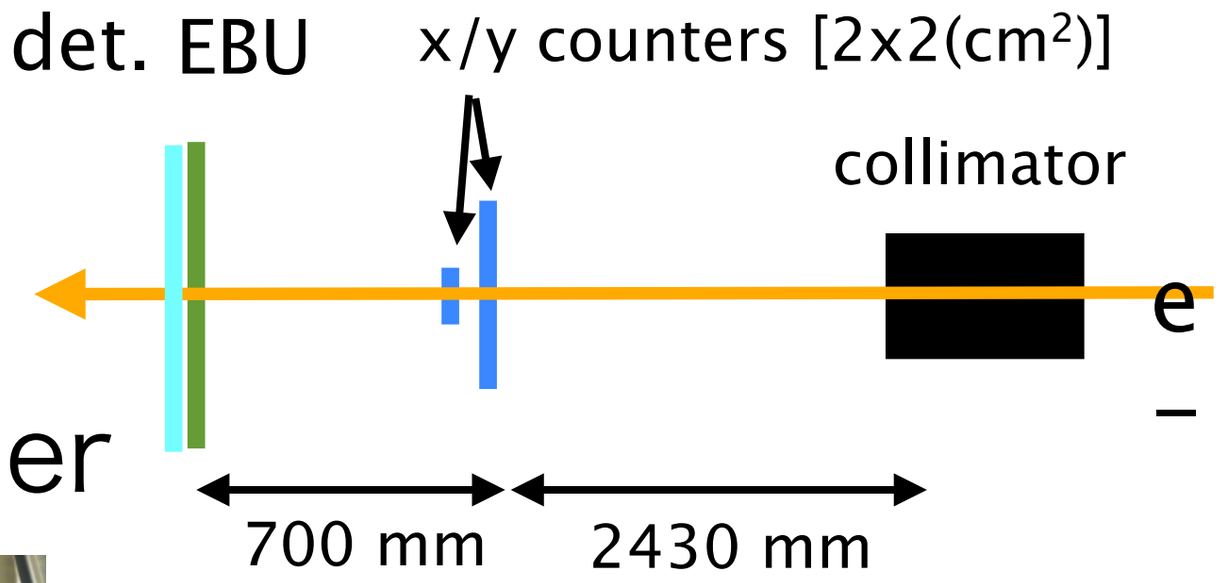
no LED equipped

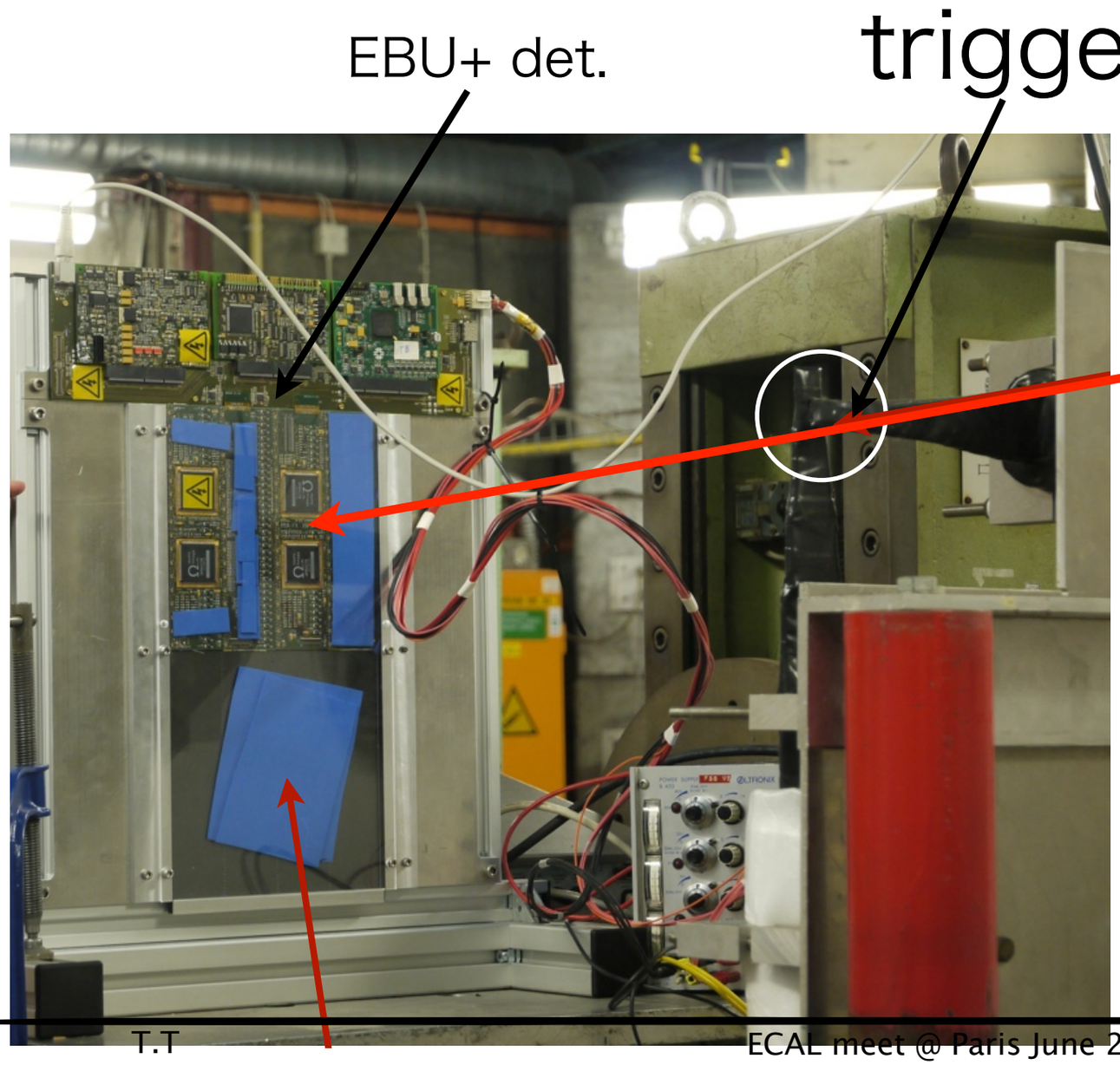


- (#good channels)/(144-32) = 50%.
  56
- There is no channel
  on ASIC132 measured correctly.

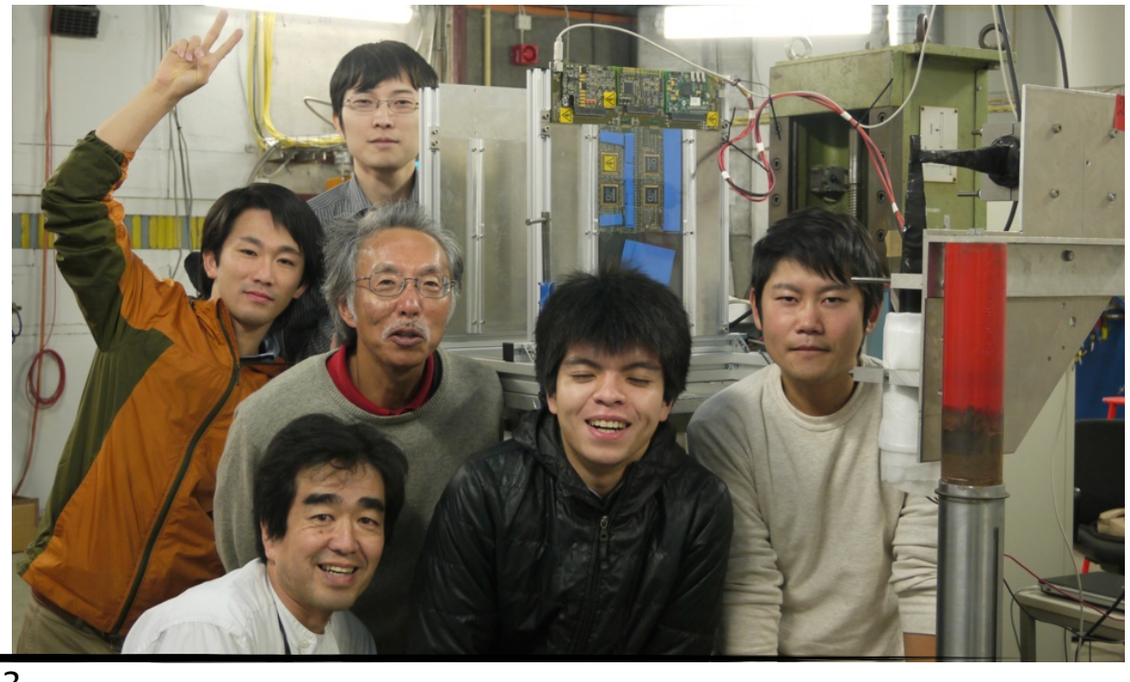
Beam test at DESY Oct-2012

- response to MIPS are measured at DEST st, 26





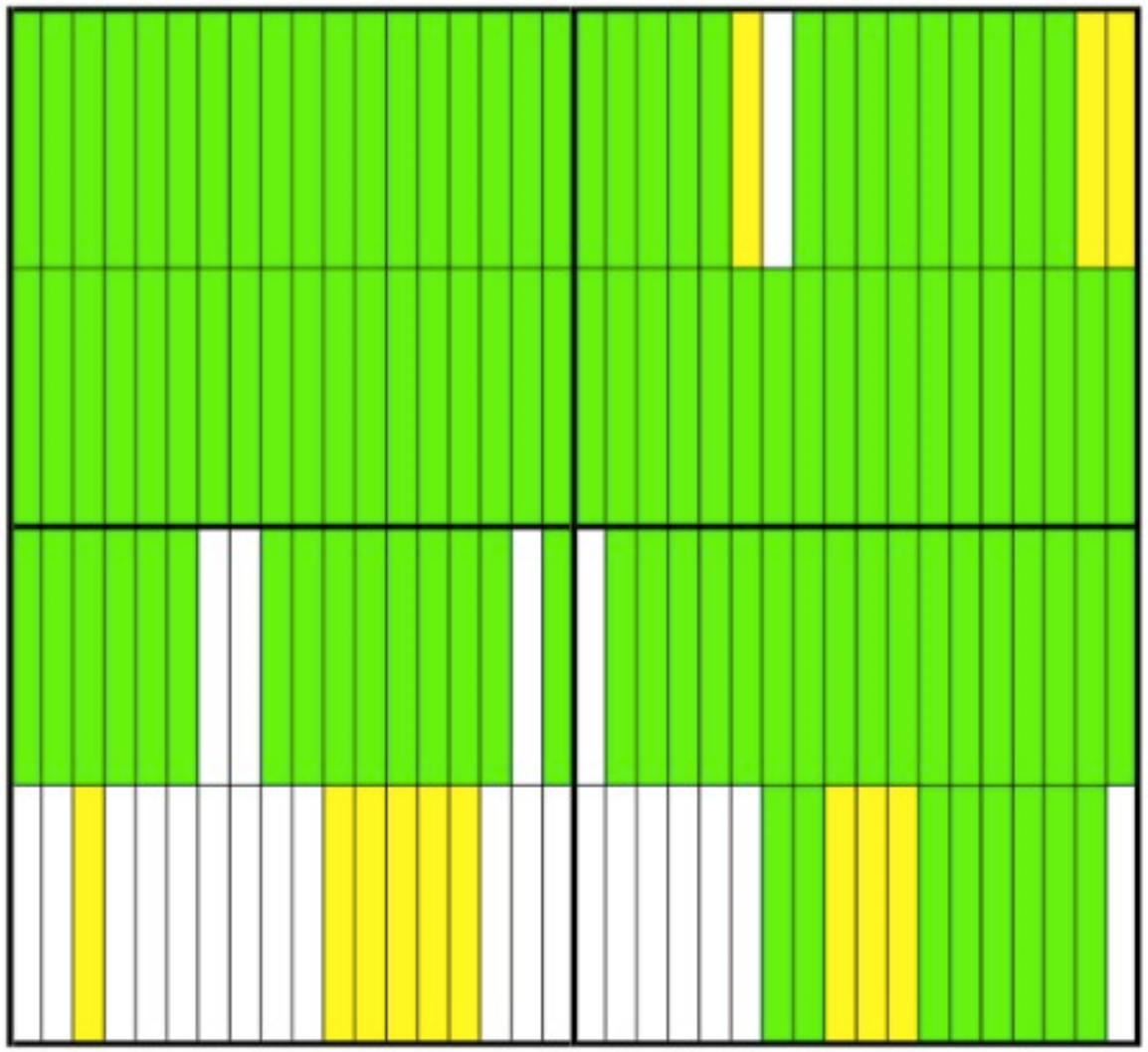
10/Oct/2012



Response to 3GeV electron events

electrons at the center positions

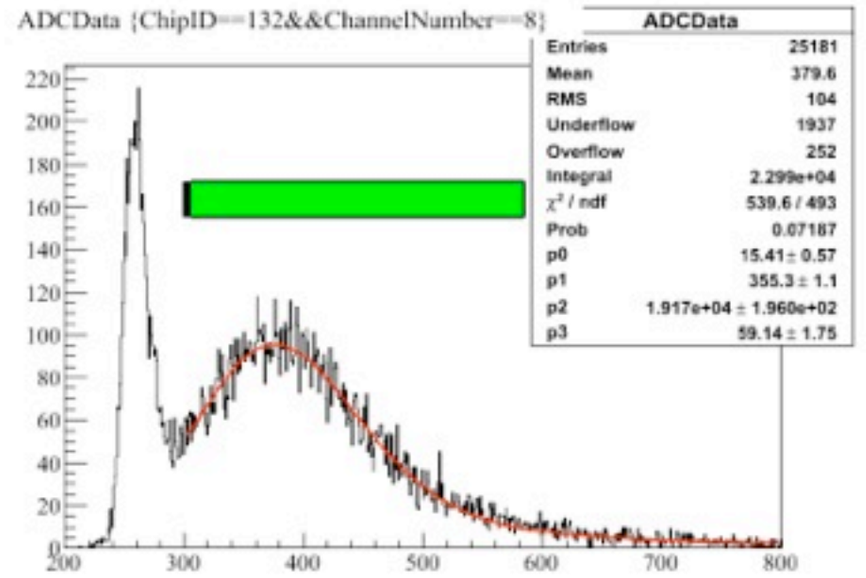
chip 129 chip 130

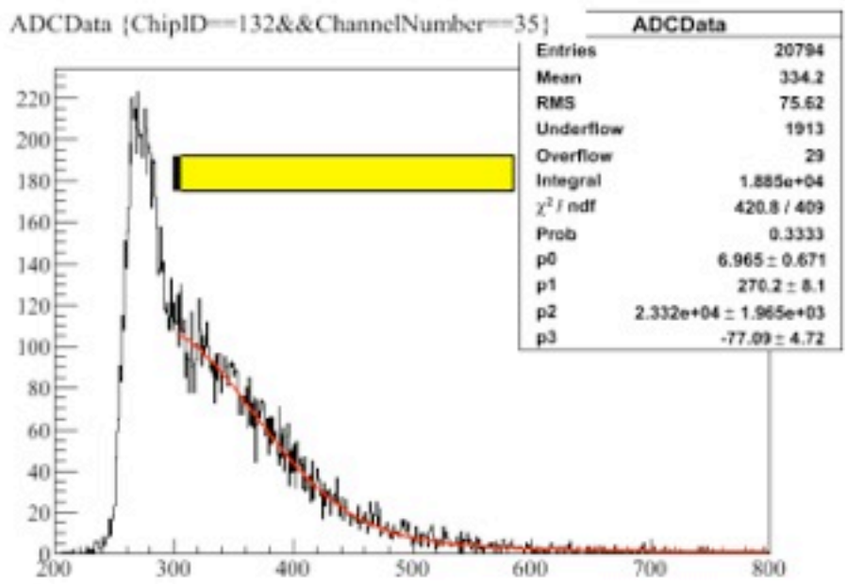


chip 132 chip 131

- 75% channels have succeeded to have good MIP distribution

ADC histogram

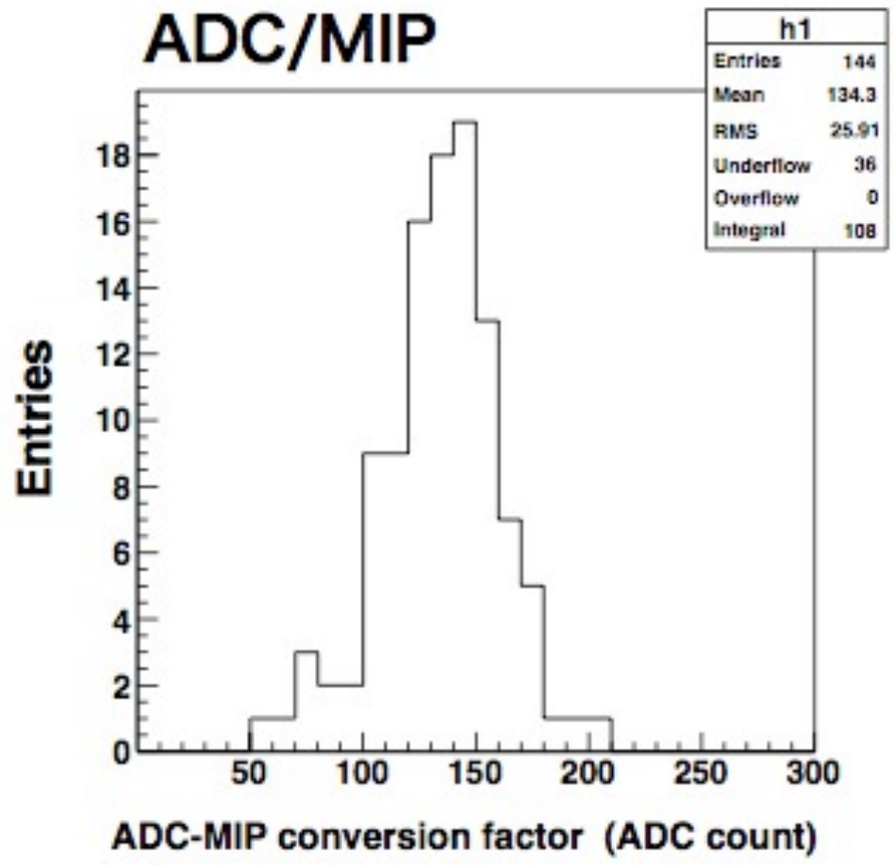


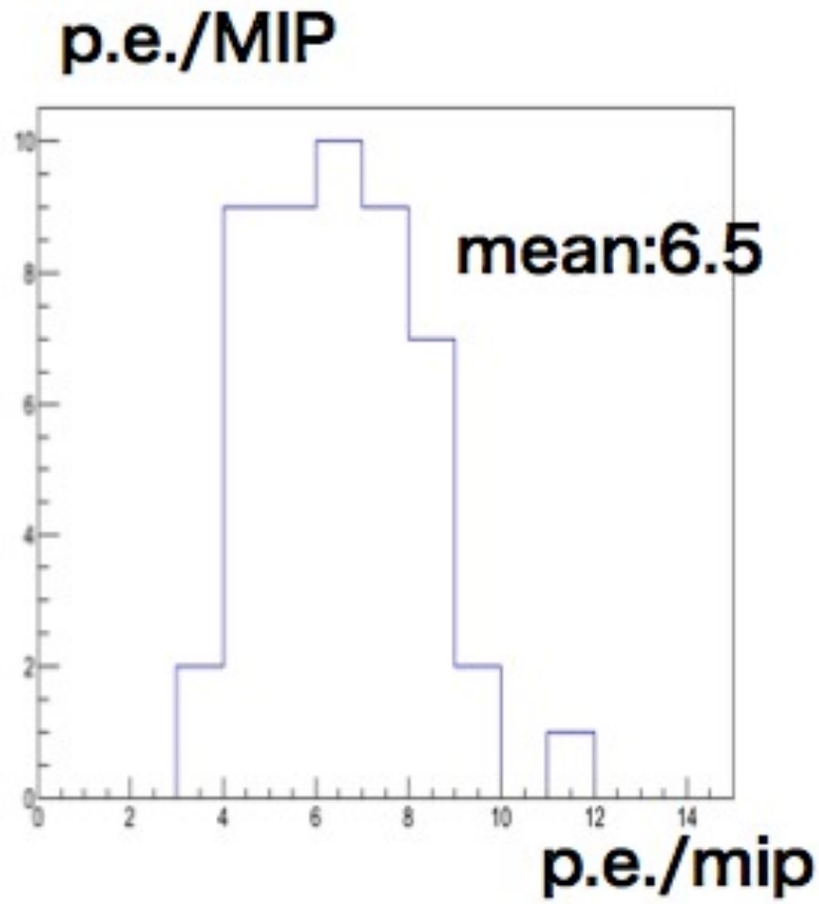


: no signal or large noise

results of beam data 2012

ADC/MIP and #photo-electrons/MIP





- 108 channels out of total 144 ch. (75%).

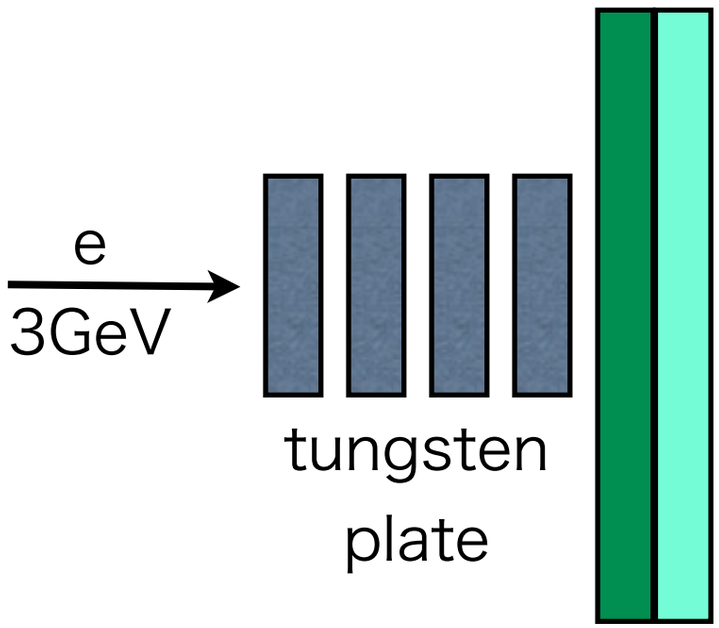
- RMS/Means = 19.3%
  (This is the similar to the case of FNAL physics prototype).

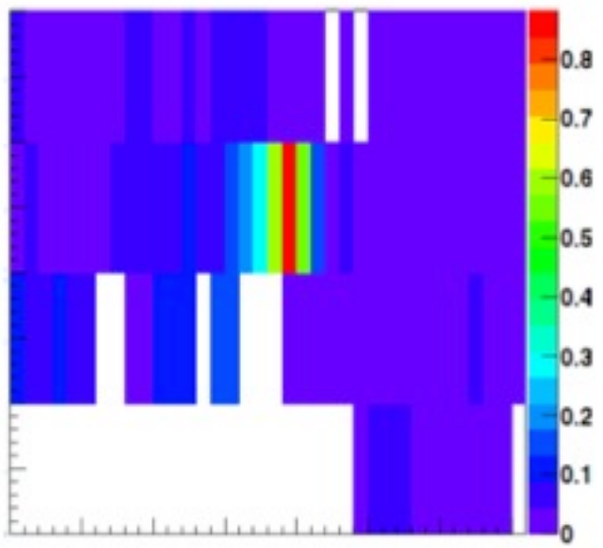
- mean = 6.5 is near the requirement,
  we need to increase gains for lower response channels (2-5 p.e.)

  - seven photo-electron is required for the real calorimeter
    to remove thermal noise and keep response for bhabha events

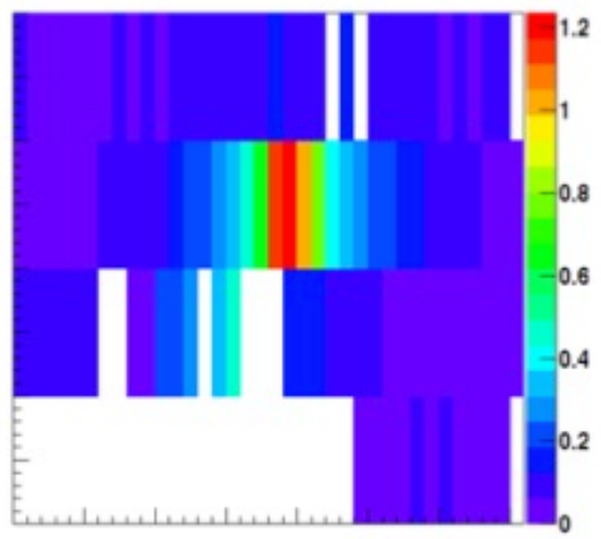
Shower events

- Putting absorber plates in front of EBU, we measure the spread of shower.



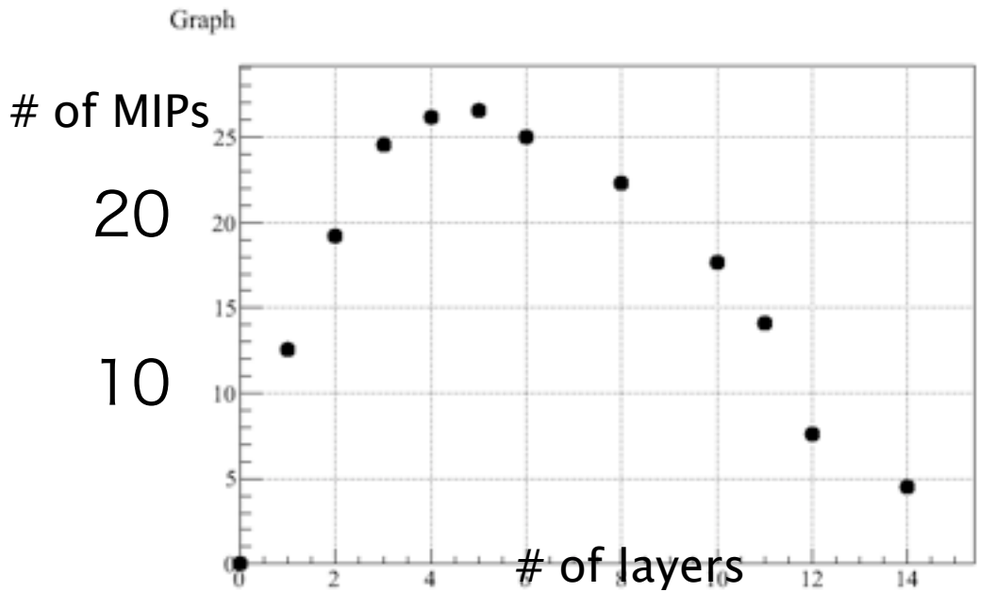


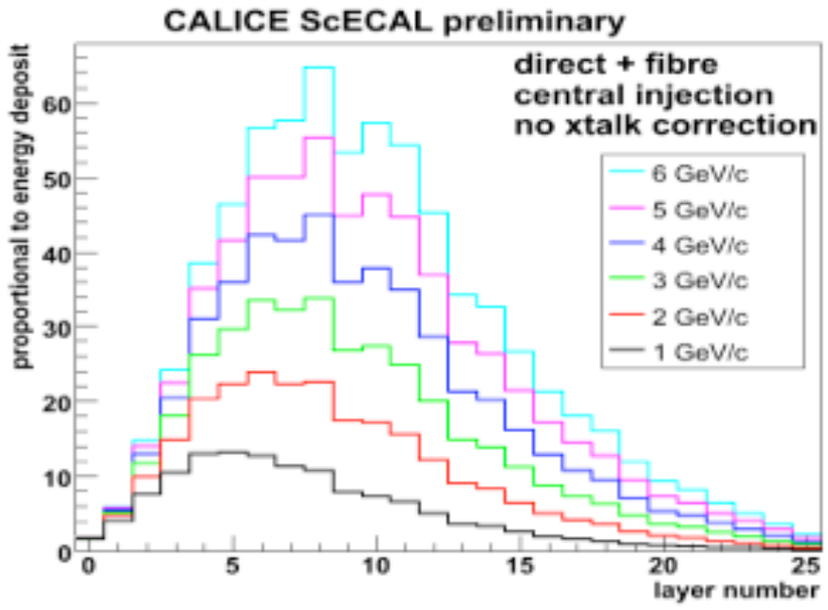
3 GeV e^- w/ 0.7 X_0 absorber.



3 GeV e^- w/ 6.4 X_0 absorber.

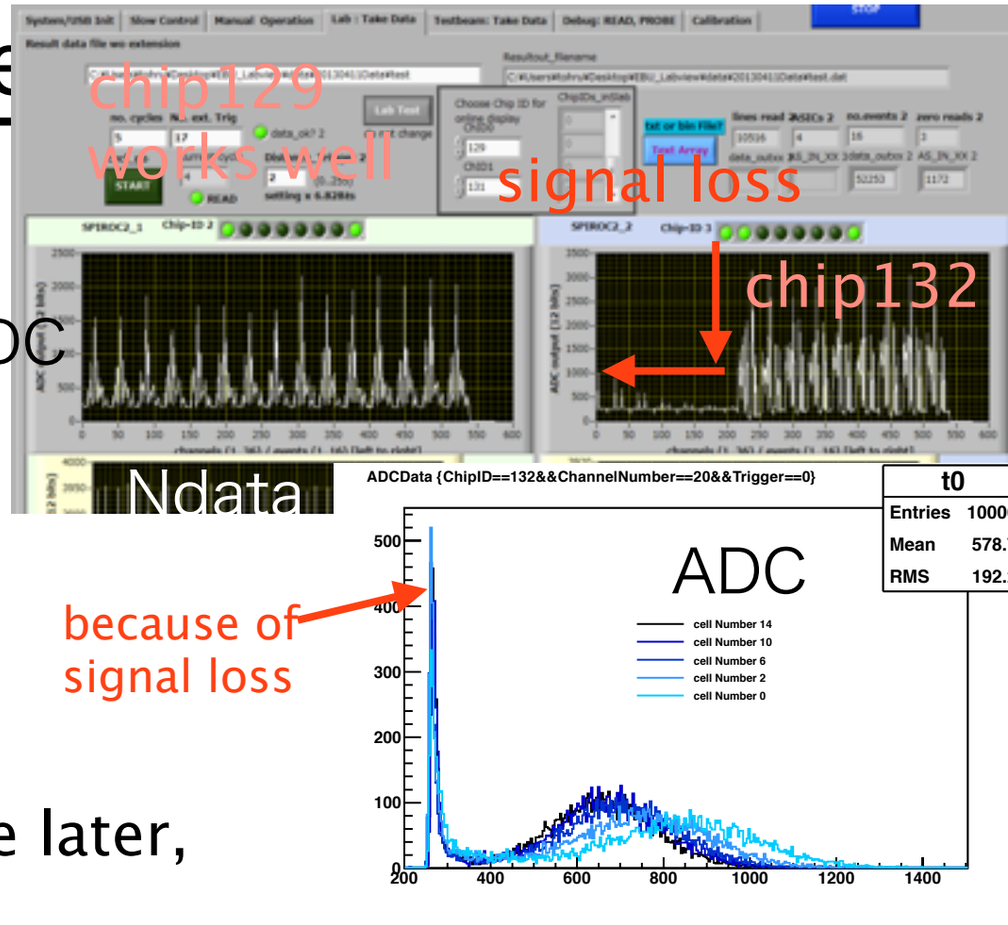
- longitudinal shower profile comparing with the result of physics prototype
  - EBU + scintillator layer
  - with physics prototype in 2009





at Shinshu , retested the LED mode

- When we use LED mode, for many channels on chip131 and 132 (at DESY only chip 132), signal loss sometimes happen.
  Once after it happens, Signal loss is kept in the whole of the cycle



- changing a trigger timing-delay value to become later, they work well.(lower picture)

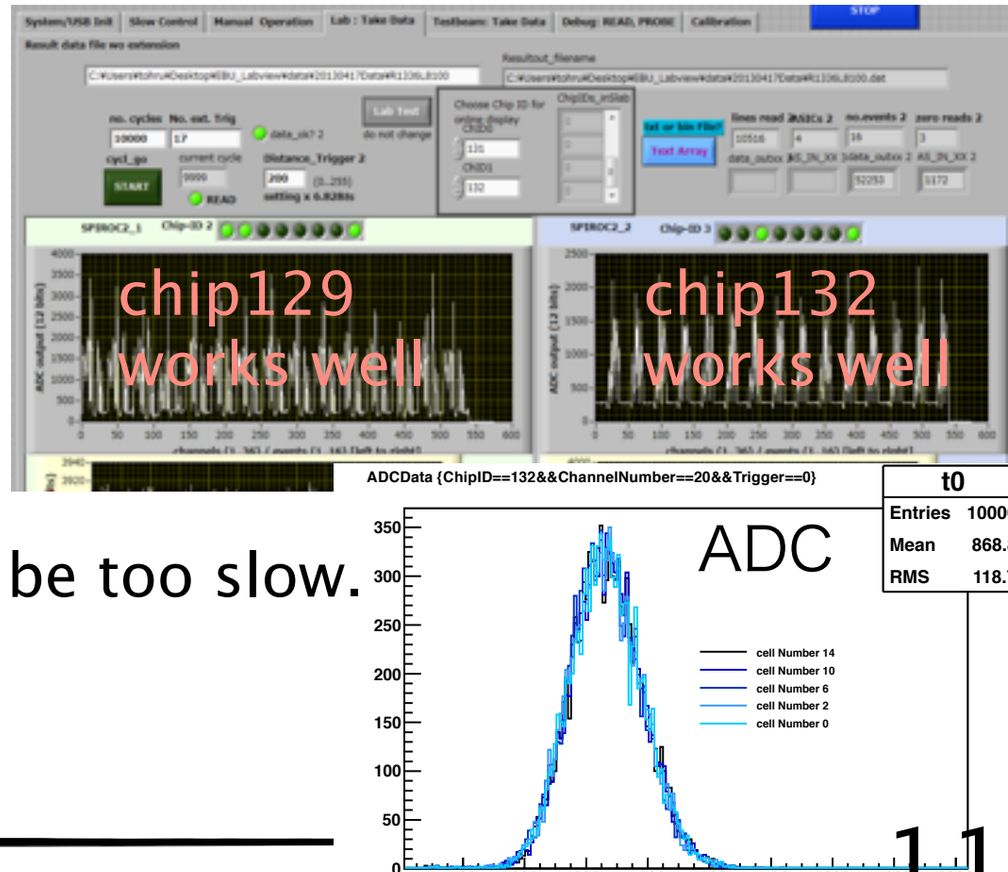
- the reasons due to LED frequency dependence

  A. the MPPC bias voltage might decrease when the LED frequency is too high .

  B. the LED bias voltage might drop

  C. the SPIROC channel-wise input DACs might be too slow.

at low frequency LED mode

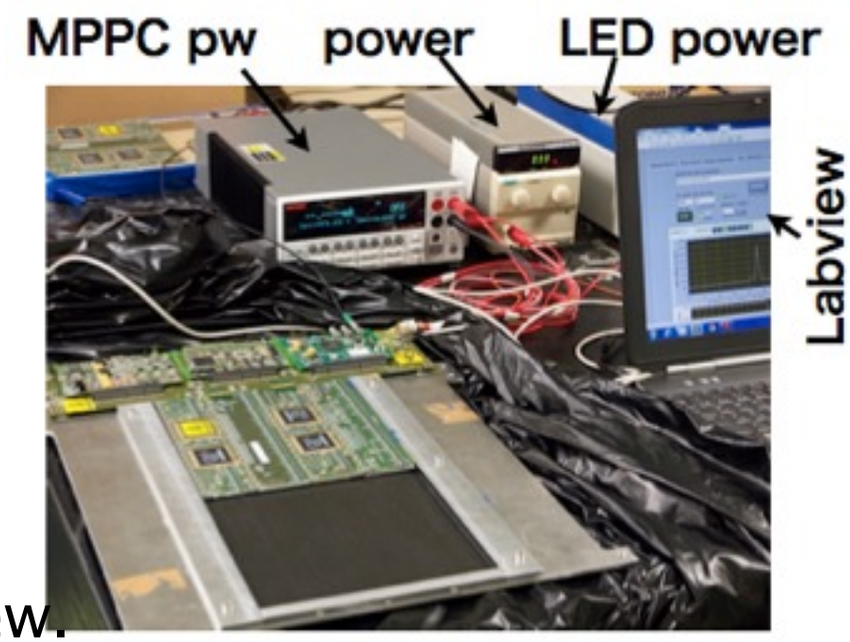


at Shinshu　Bad channels at beam were investigated

- For a few unseparated channels against MIP signal, we rise MPPC's bias voltage. they work well.

due to lower gains

- we could not do pre-experiment well to measure break down voltage of MPPCs.
  due to this, we set the wrong DAC value to the Labview.

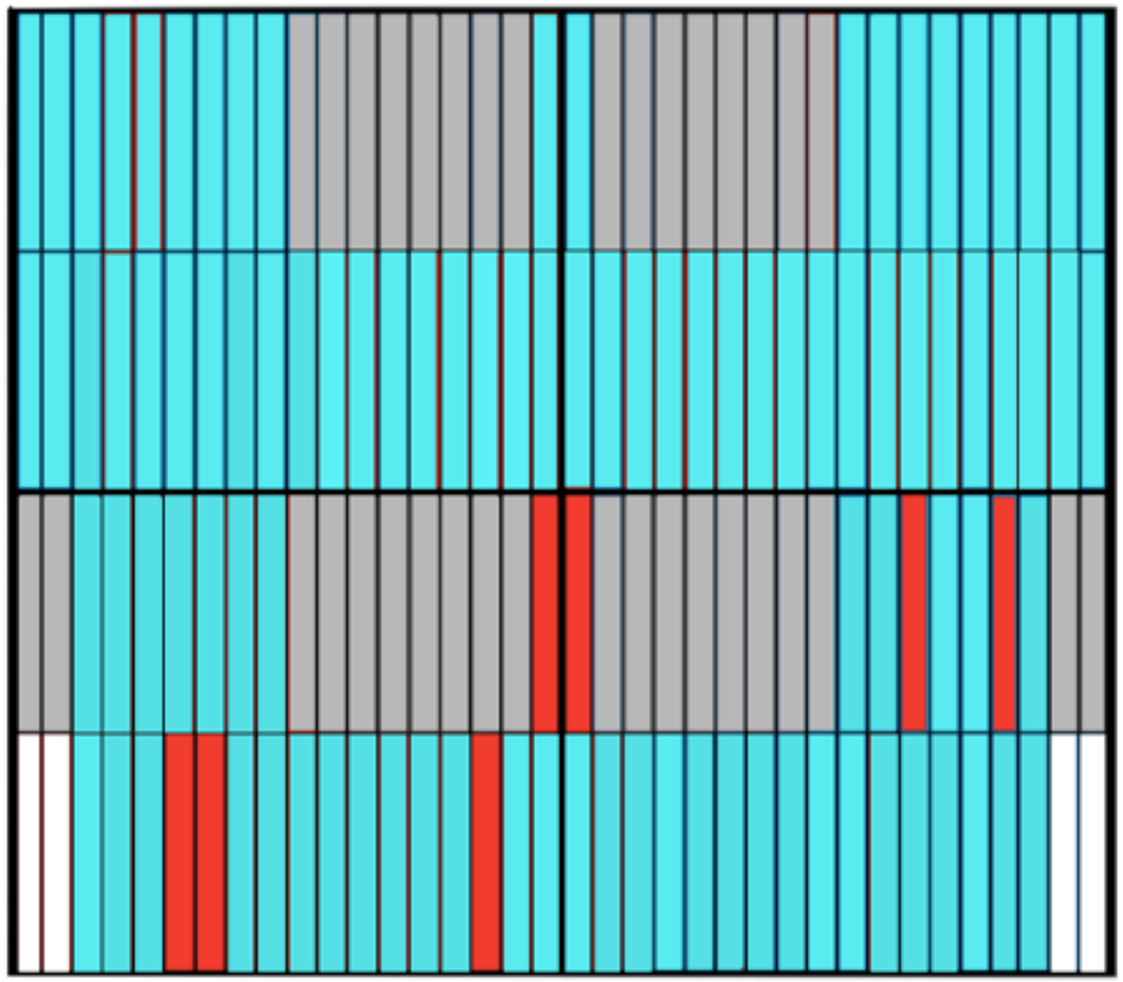


- we took out two lanes of scintillators and removed the reflector in front of MPPC, then they work well.

construction fail

- when we fixed a scintillator layer by hands, a scintillator layer cought a reflector film.

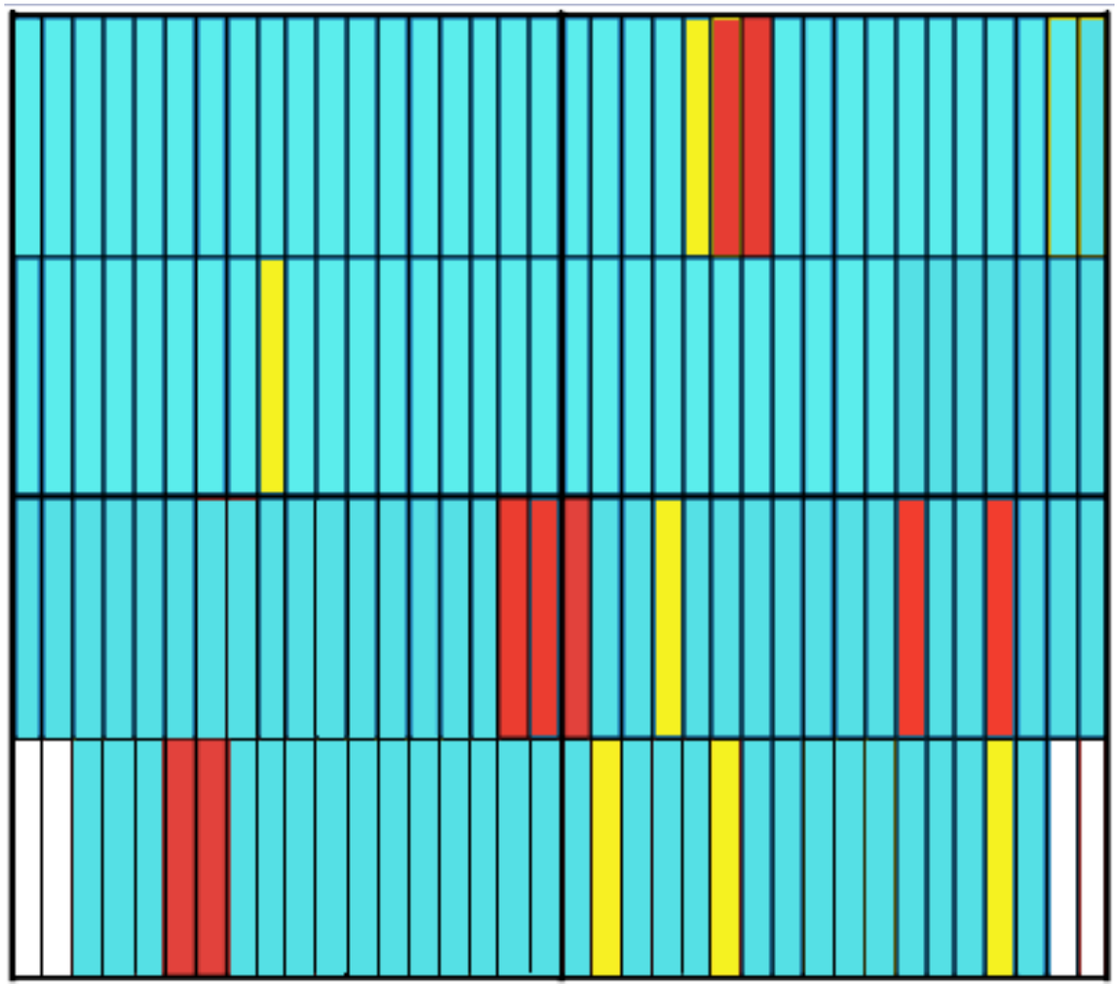
LED calibration results



- LED calibration result
97ch/108ch ~90% success

source test results Sr90

- bias voltage ΔV = +2.5 from break down



still lower biasing at
- MIP calibration result with Sr90 RI source : 125/144~87%

Recovered at Shinshu 2013

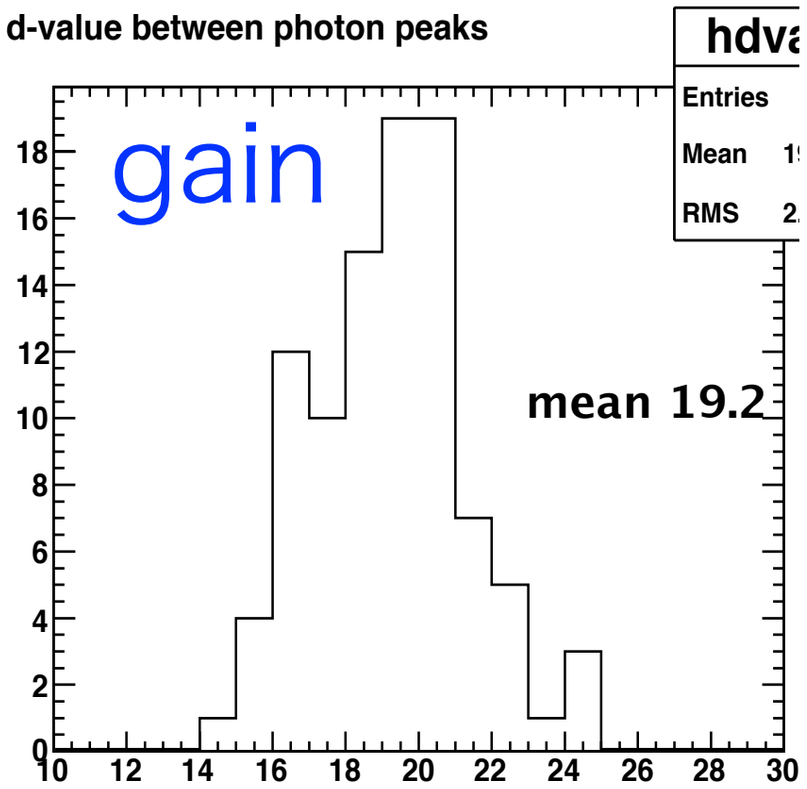
- result with LED and Sr90 RI source (not include some dead channels)

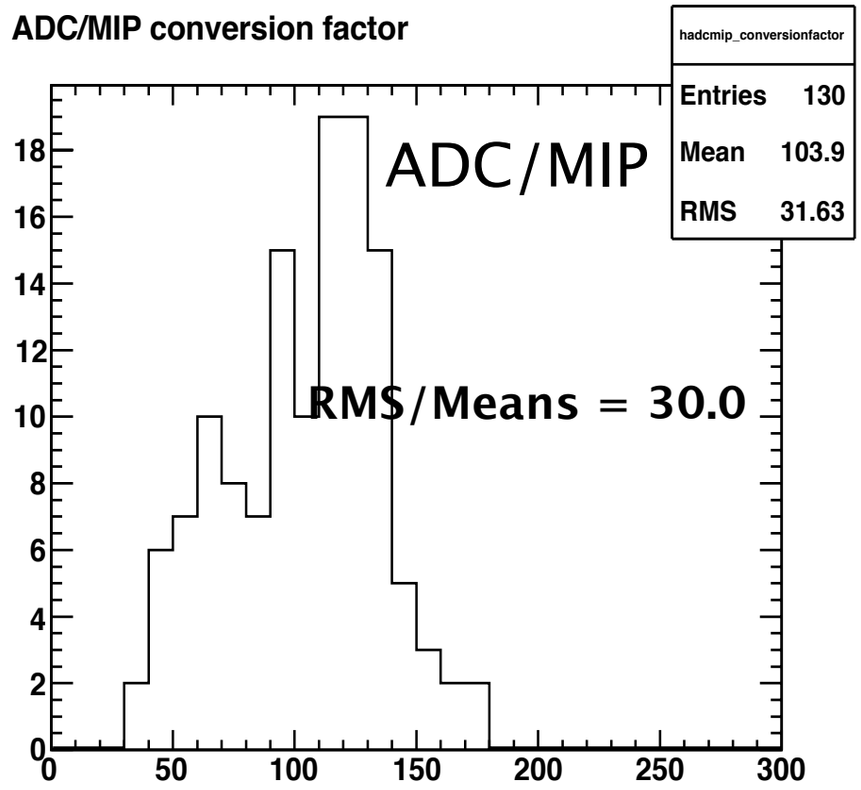
- gains are reasonable

LED: BT to Shinshu

Nch: 56 to 130

mean : 20.4 to 19.2





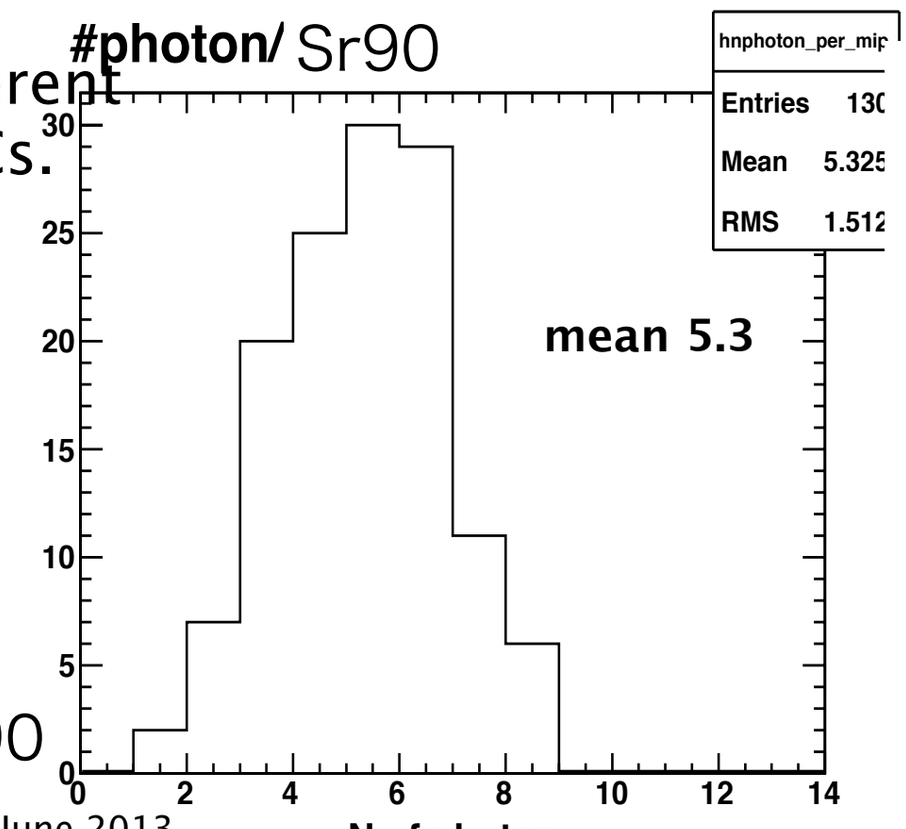
#photon for MPV is not different between control area of ASICs.

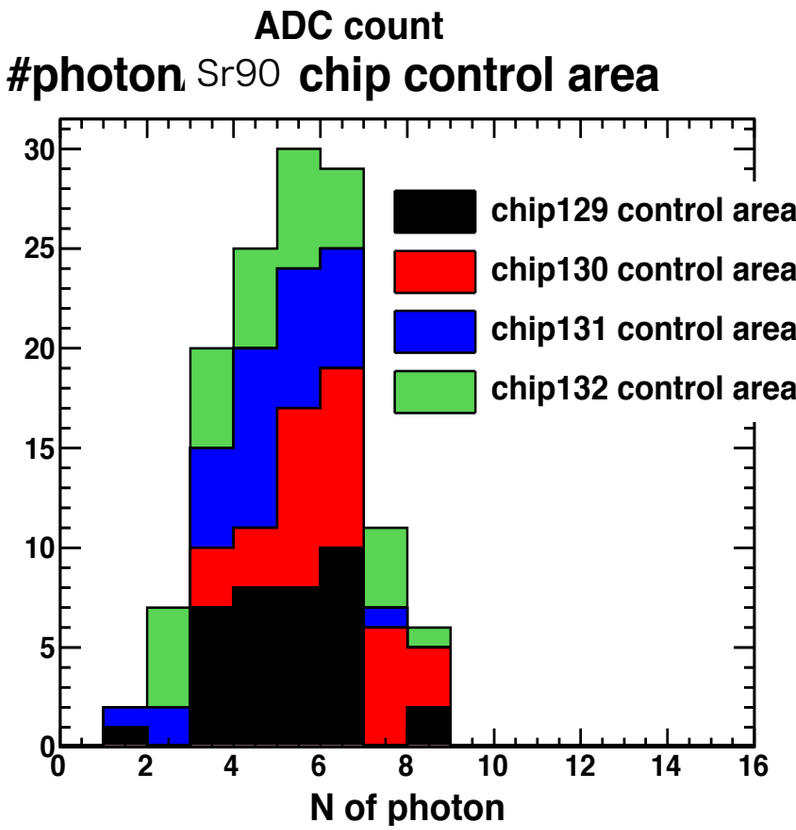
MIP: BT to Shinshu

Nch: 108 to 130

mean : 6.5 to 5.3

may be due to source Sr90





Summary until now

- We have tested a technological prototype layer
  144 channel using electron beam at DESY Oct 2012.

- We have measured the MIP peaks in the energy deposit at around 6.5 p.e.
  for 75% of channels.

- From TB, we have leant much, and investigated some problems
  we have solved some of those problems at shinshu university

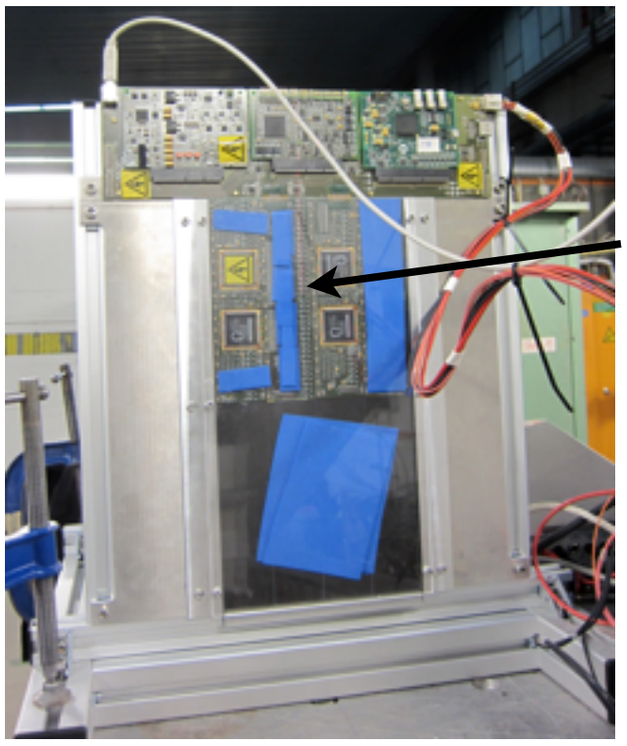
- we could measure d-value on LED mode with 97 channels
  in 108 equipped LED channels. -> 90%

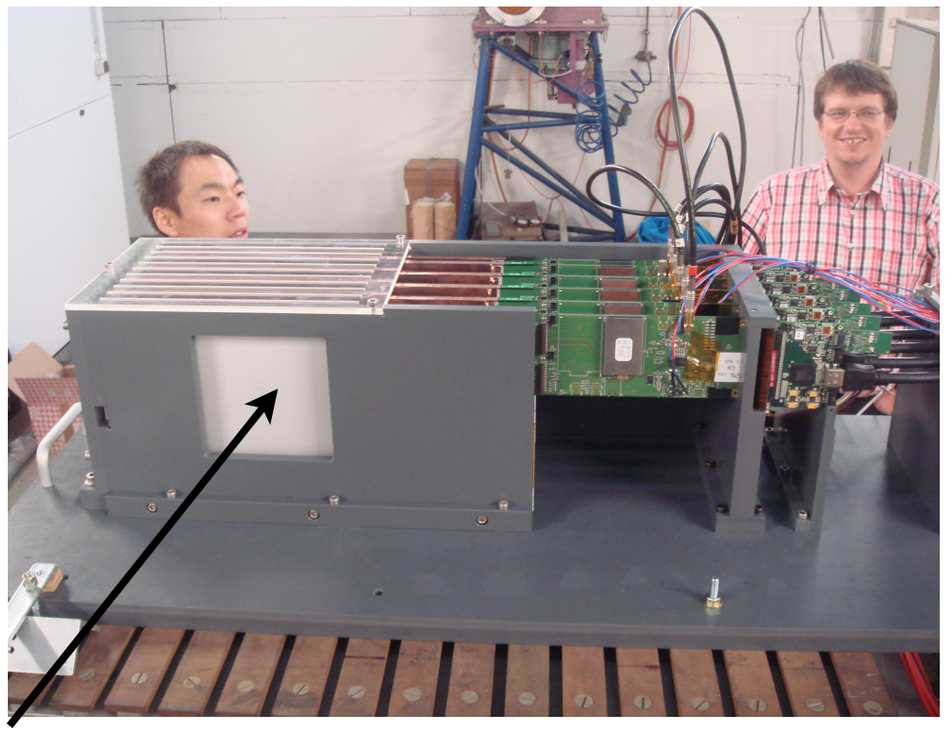
- we could measure MPV on TestBeam mode with 125 channels
  out of 144 channels with Sr90 RI source. -> 87%
  and the result is MPV of around 5.3 p.e.

plan for the July beam test

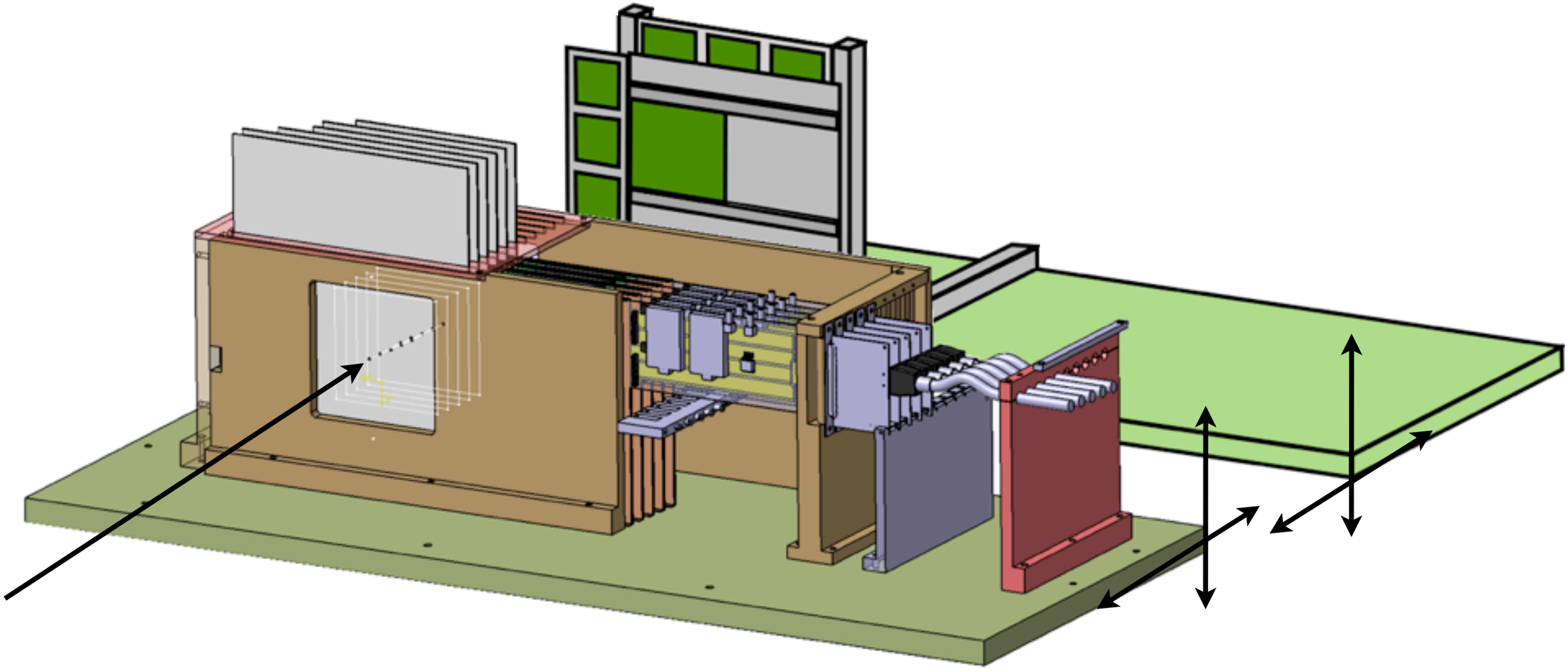
- Next test beam is scheduled at beginning of July, we will test the hybrid ECAL with SiECAL group.
- The purpose is
  - synchronized between Sc layers (not trivial)

    Two layers (x and/or y type) ScECAL prototype
    - the power pulsing mode
    - the TDC data
  - combined with Si-W-ECAL prototype (Hybrid ECAL) (if possible)





setup at DESY st. ??



on the moving stage

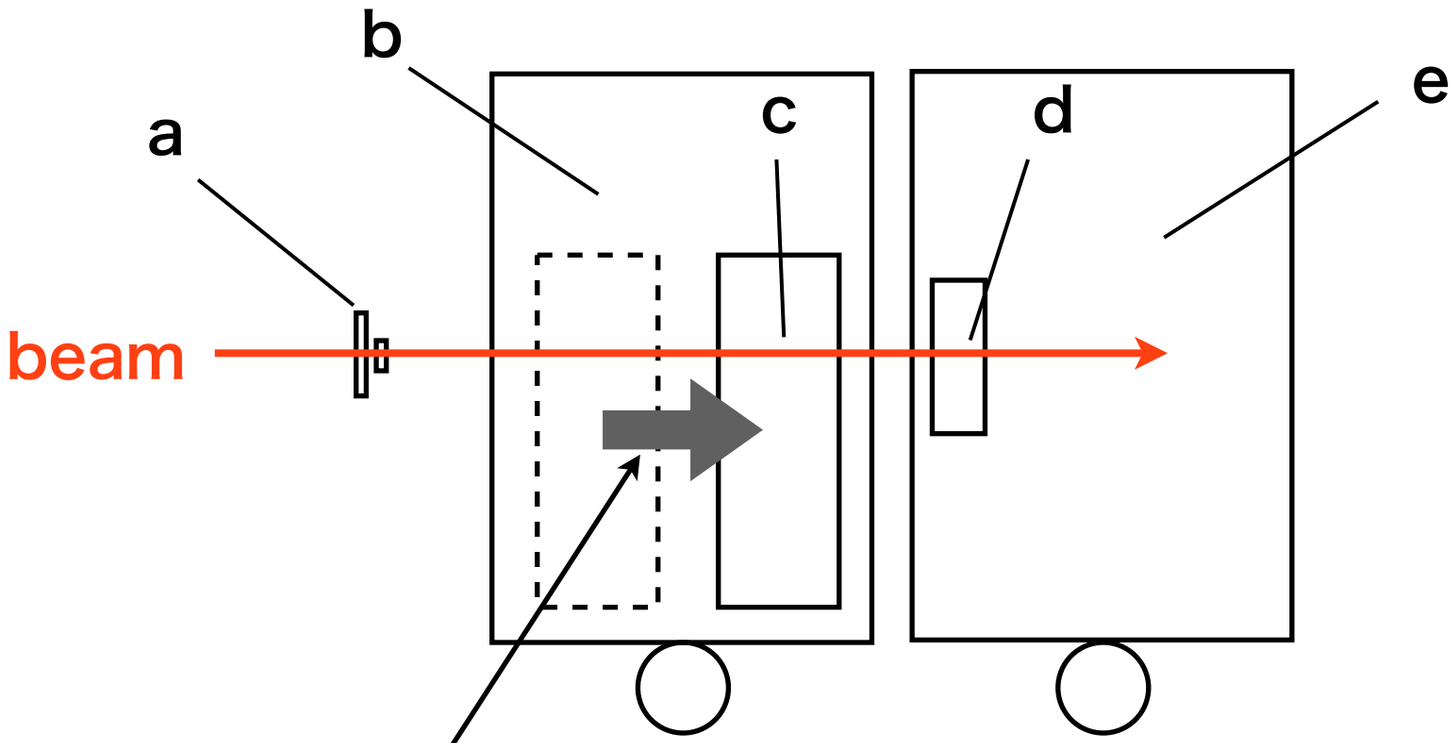
possible schedule

Mon.	day		
6	24-30	Scintillator assembly on EBUs and lab-test	
7	1	Set up with Si-prototype	
	2		
	3		
	4	Optimization; data taking rates, DAQ/ MIP runs	
	5	Physics runs; energy scan, position scan	
	6		
	7		
	8	Si-prototype, spare days	Sc-prototype MIP position scan
	9		
	10	Si-prototype dismounting	Sc-prototype Power pulse, TDC runs
	11		
	12		Sc-prototype, spare days
	13		
	14		Sc-prototype dismounting

Members from Asia

- Shinshu University
  - T. Ogawa, ?, K. Kotera,
- Kyushu University
  - Y.Sudo,
- Tokyo University
- Kyungpook University
  - ?

Sc-layers behind the Si-prototype



a. x-y counters
b. stage (1)
c. Si-prototype
d. Sc-prototype
e. stage (2)

- Can Si be put downstream side on stage (1)?
- It is better if we can use some signals from Si prototype instead of x-y counters.
-