SKIROC 2 Measurements

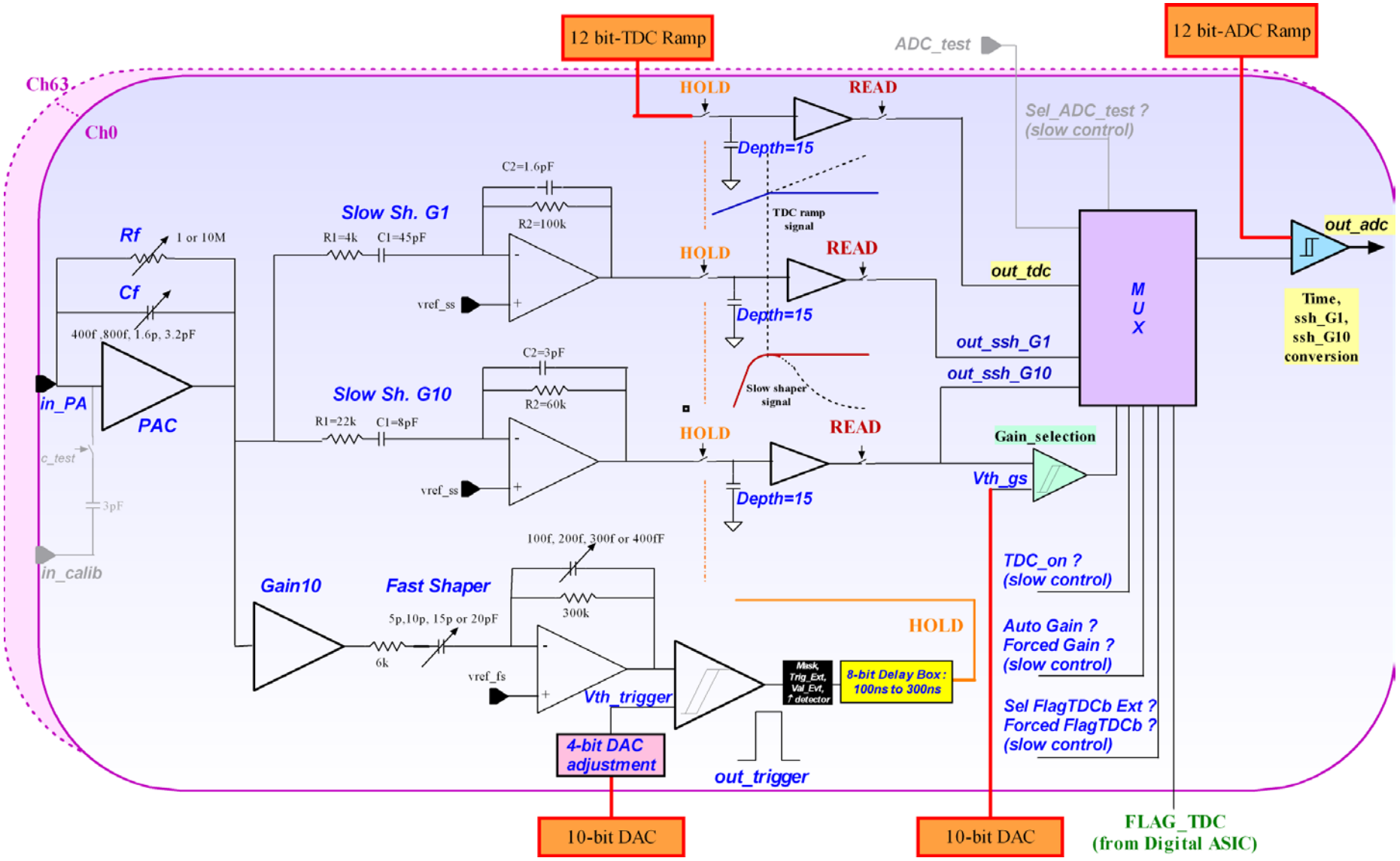
10/09/2013

CALIIMAX-HEP

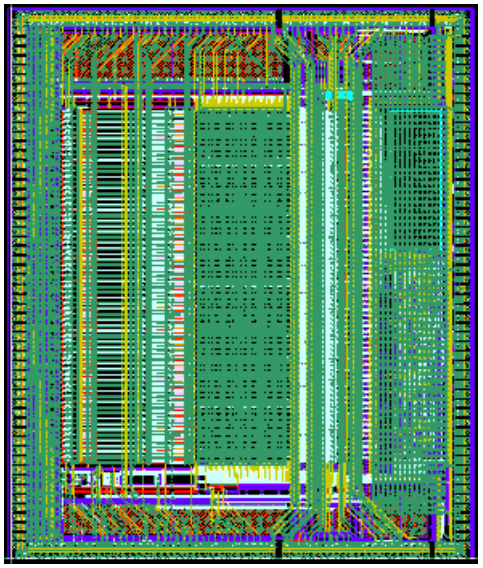
Design and industrial applications of an high granularity e-cal read out chip

- PhD student at LLR under the responsability of Rémi Cornat
- Funded by Weeroc, start-up created by Julien Fleury. Spin off of the Omega group (director: Christophe de la Taille)
- First step : Characterisation of SKIROC 2.

SKIROC 2 analog core

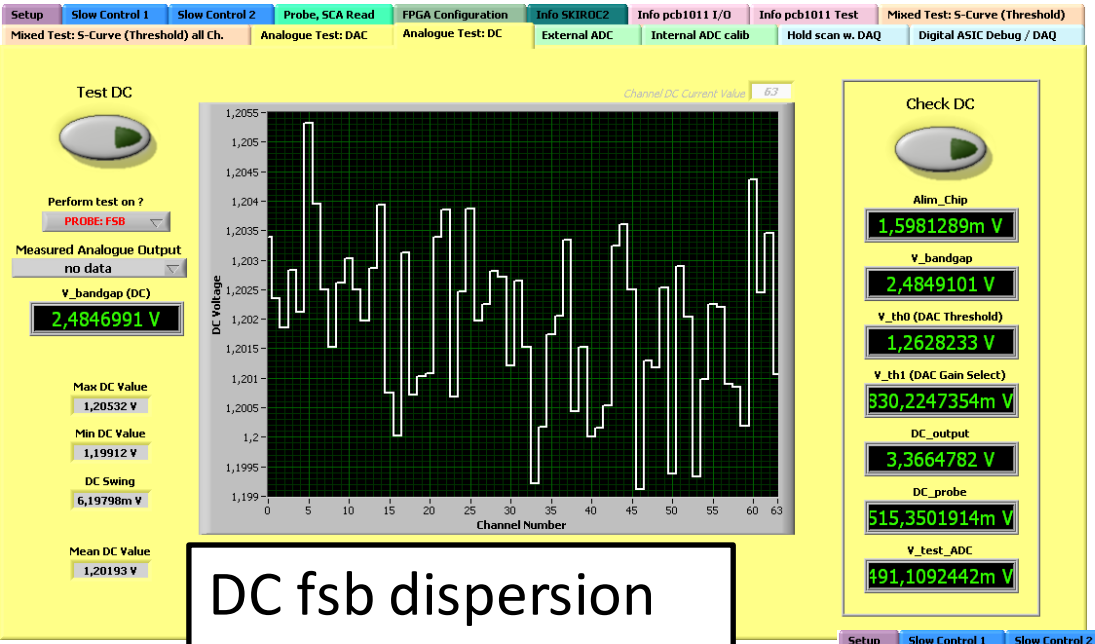


SKIROC 2



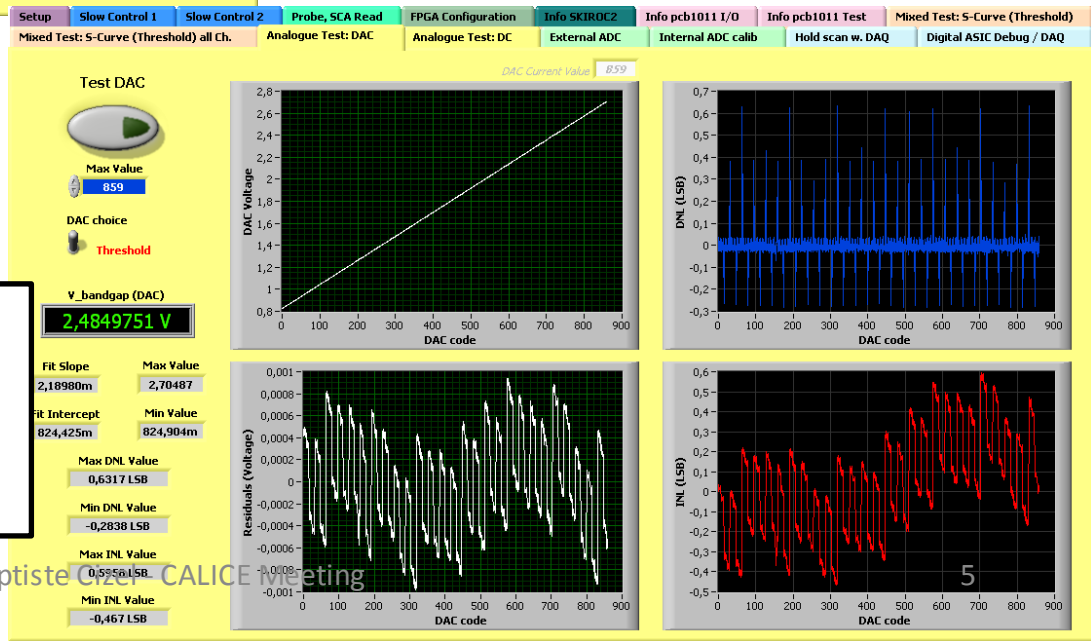
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC: **1 Mip (4fC)→ 2500 Mip**
  - Shaping time of 180ns
  - Mip/noise ratio > 10
- Auto-trigger on 1/2 MIP (2 fC)
  - MIP/noise ratio on trigger channel >10
  - Fast shaper : ~30 ns
  - Auto-Trigger on ½ MIP
- Analog memory for time and charge measurement : depth = 15
- 12 bit-ADC, 4k internal memory
- Daisy chain readout
- Low consumption : ~25 µW per channel (in power pulsing mode)

Test of 13 ASICs



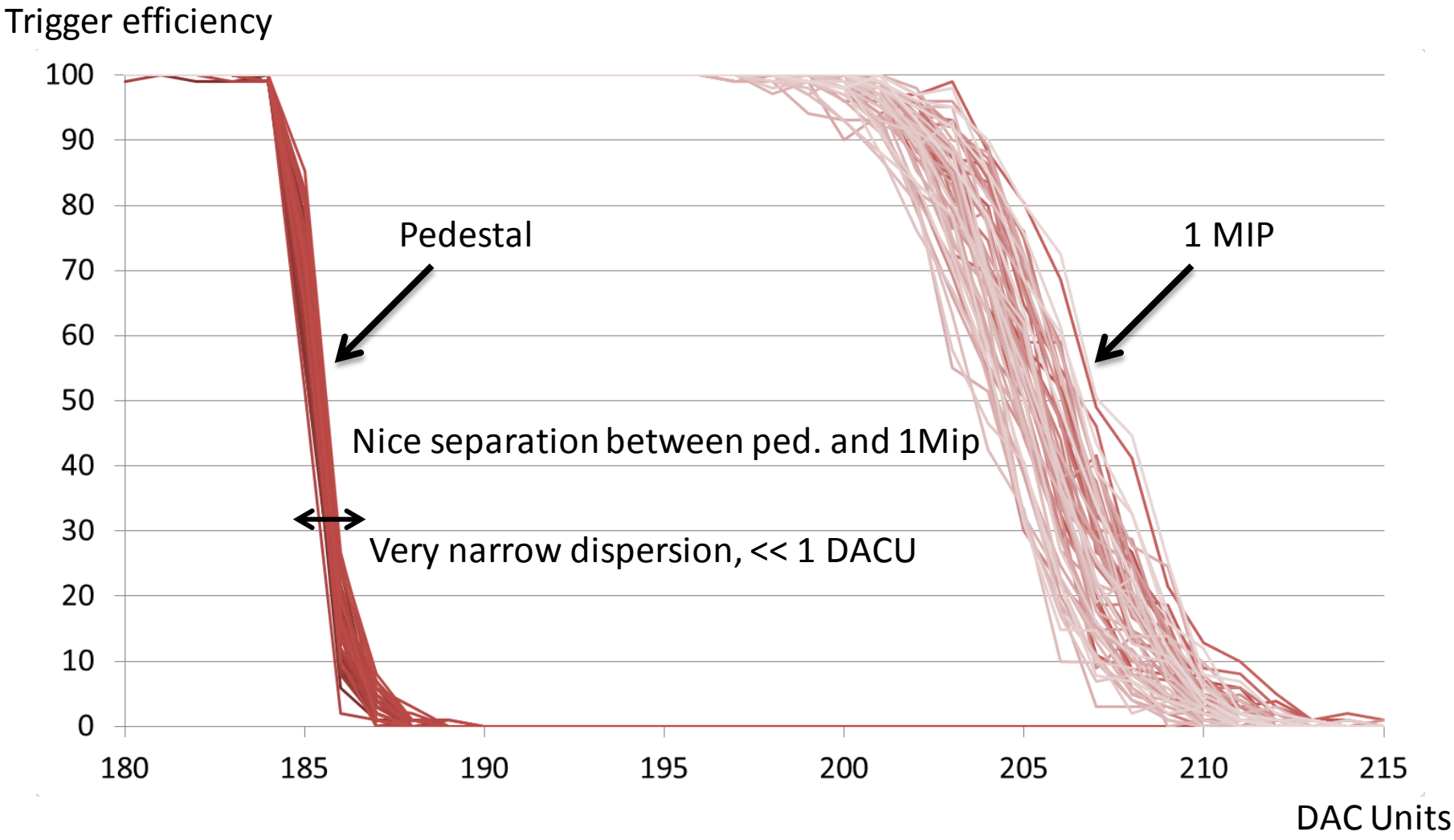
Test of 13 ASICs using a testboard without any decoupling capacitors on bias and reference voltages.

DC fsb dispersion
<DC> = 1.20193
DC Swing = 6.2 mV



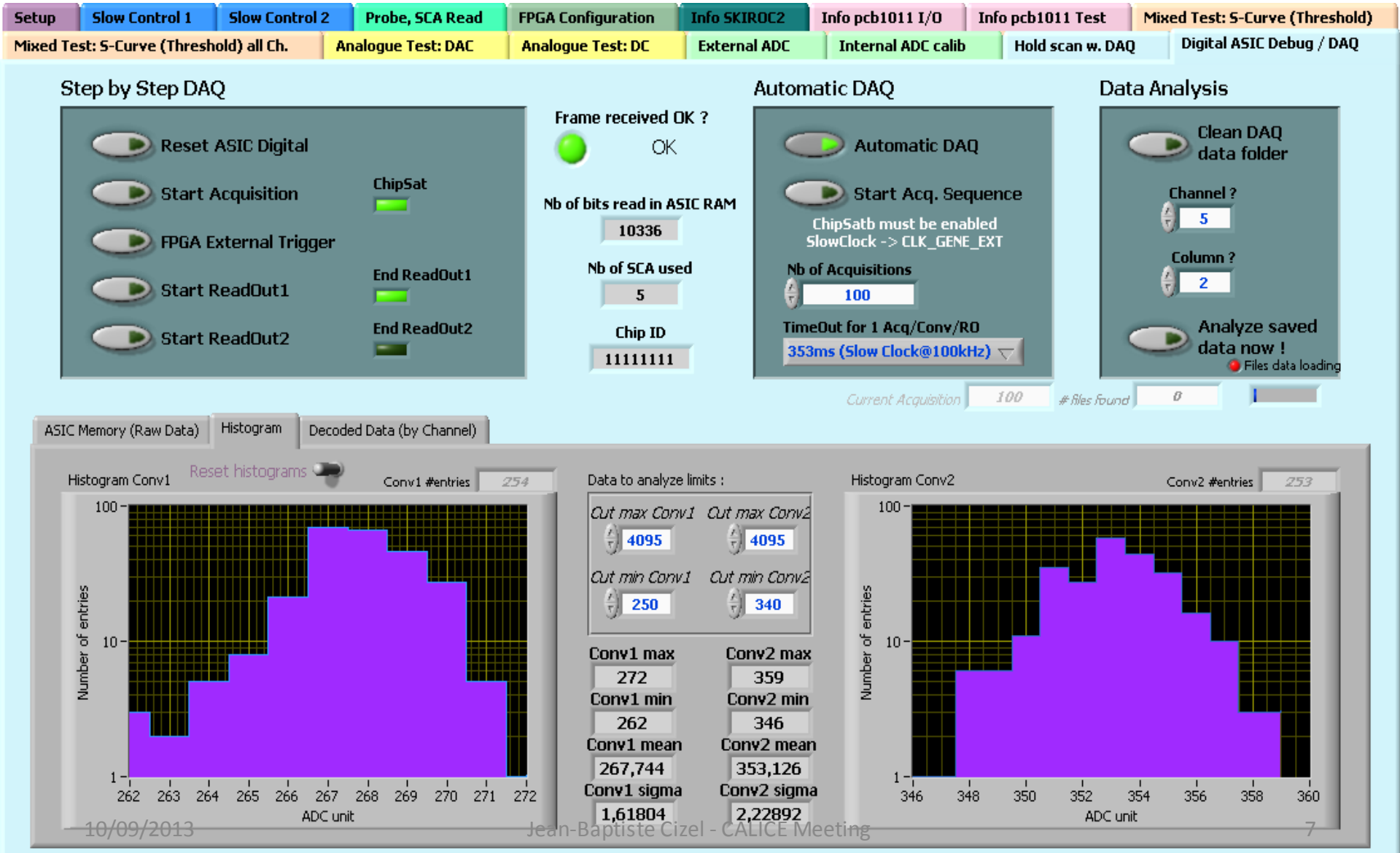
10 bit DAC linearity
Slope = 2.19 mV/DACu
INL = +/- 1 LSB

Scurves


Trigger efficiency
100
90
80
70
60
50
40
30
20
10
0
180
185
190
195
200
205
210
215
DAC Units
Pedestal
1 MIP
Nice separation between ped. and 1Mip
Very narrow dispersion, << 1 DACU

DAQ measurements

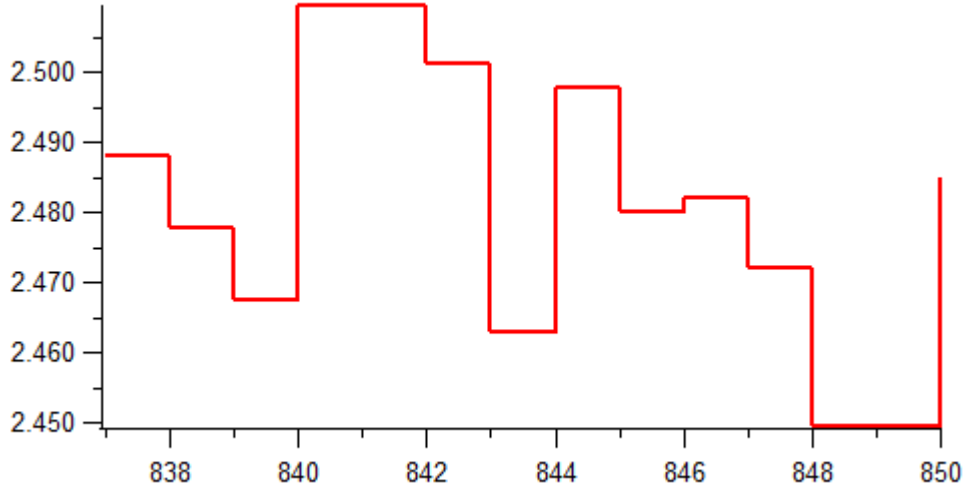
Made for 10, 20 and 40 MIP. 1 ADC unit = 400 uV.



Summary for 13 chips

Chip	Vbg	Dcfsbmean	Dcfsbmax	Dcfsbmin	Dcfsbswing	DCss1mean	DCss1swing	DCss10mean	DCss10swing	ped	1Mip	10Mip
837	2.48818	1.20955	1.21323	1.20666	6.57	0.99819	4.02	0.99576	6.08	185.3	209	471
838	2.47781	1.19365	1.19624	1.18939	6.848	0.994978	4.578	0.991346	5.53	182.95	207	472
839	2.46742	1.19041	1.19425	1.18752	6.73	0.986758	4.397	0.987963	5.06	185.65	209	470
840	2.50945	1.21013	1.21279	1.20743	5.36	1.00722	4.08	1.00567	4.91	181.85	204.5	462
841	2.50949	1.22449	1.22768	1.22116	6.52	1.00722	3.5	1.00409	4.597	187.35	209.5	458
842	2.50117	1.21095	1.21373	1.20774	5.99	1.00032	4.14	0.999516	4.64	183.75	206	457
843	2.46281	1.19746	1.20176	1.1941	7.66	0.99015	4.48	0.987648	4.9	188.3	209.5	470
844	2.49785	1.21576	1.21947	1.21318	6.3	1.00348	5.06	0.999859	4.6	188.7	211	462
845	2.48011	1.20318	1.2054	1.19953	5.87	0.993826	5.7	0.992698	4.2	186.45	209	468
846	2.48202	1.19625	1.20045	1.19337	7.1	0.994863	3.8	0.992484	4.3	183.9	204	464
847	2.47205	1.19417	1.1976	1.19142	6.19	0.995202	4.85	0.988176	4.23	182	203.5	460
848	2.44953	1.1785	1.18123	1.1753	5.93	0.980579	4	0.984563	5.52	180.5	203.5	469
850	2.48497	1.20193	1.20532	1.19912	6.2	0.99878	3.98	0.996672	5.33	184.1	207	468

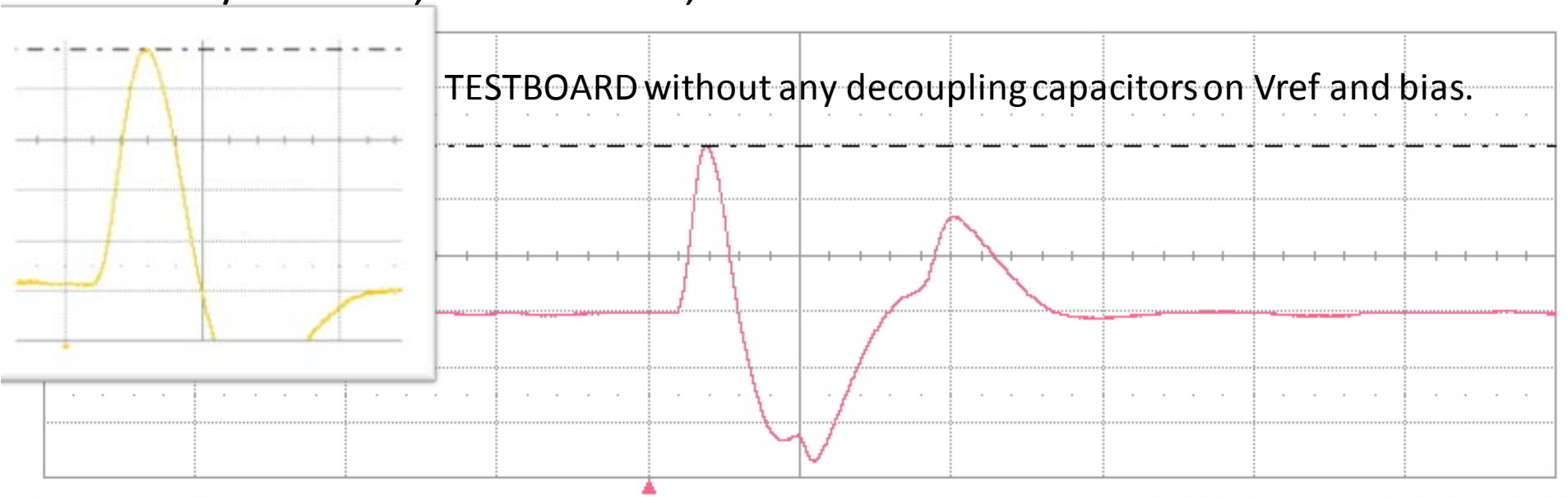
Vbandgap



All the results will be detailed in a report.

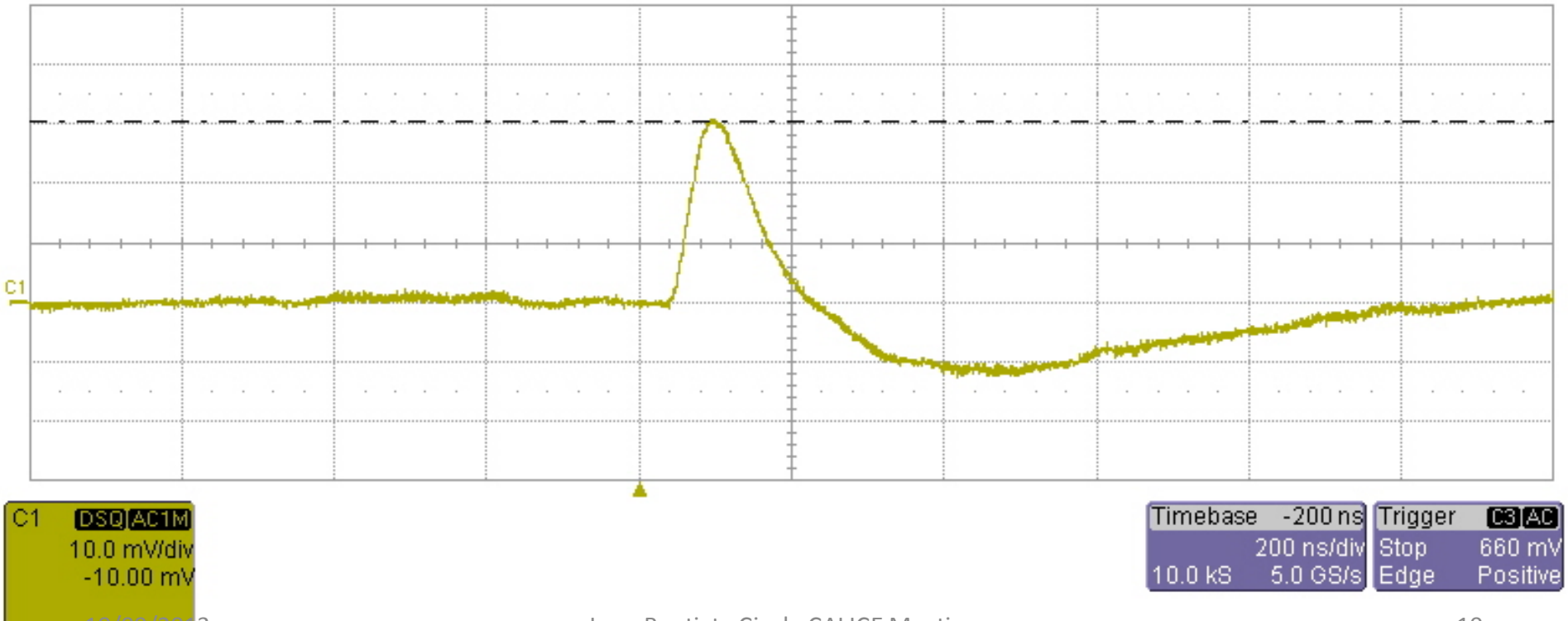
Analogue crosstalk

- 100 MIP are injected in channel 2
- We observe the fast shaper output of channel 3
- Signal of 58.8 mV (average on 100 steps). It corresponds to 58.8/46.8 = 1,26 MIP. => 1,26 %



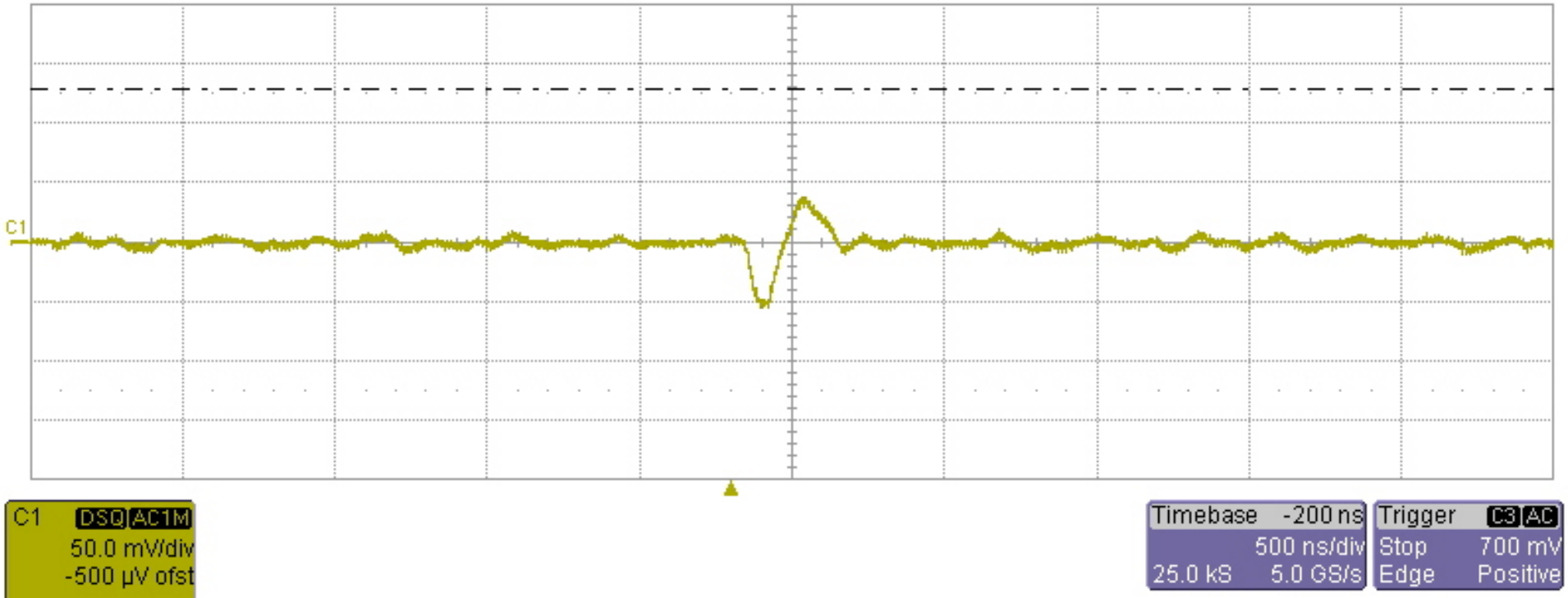
Analogue crosstalk

- 1000 MIP are injected in channel 2.
- Signal of 30 mV the slow shaper gain 10 output. It corresponds to 6 MIP. => 0,6 %



Long distance crosstalk

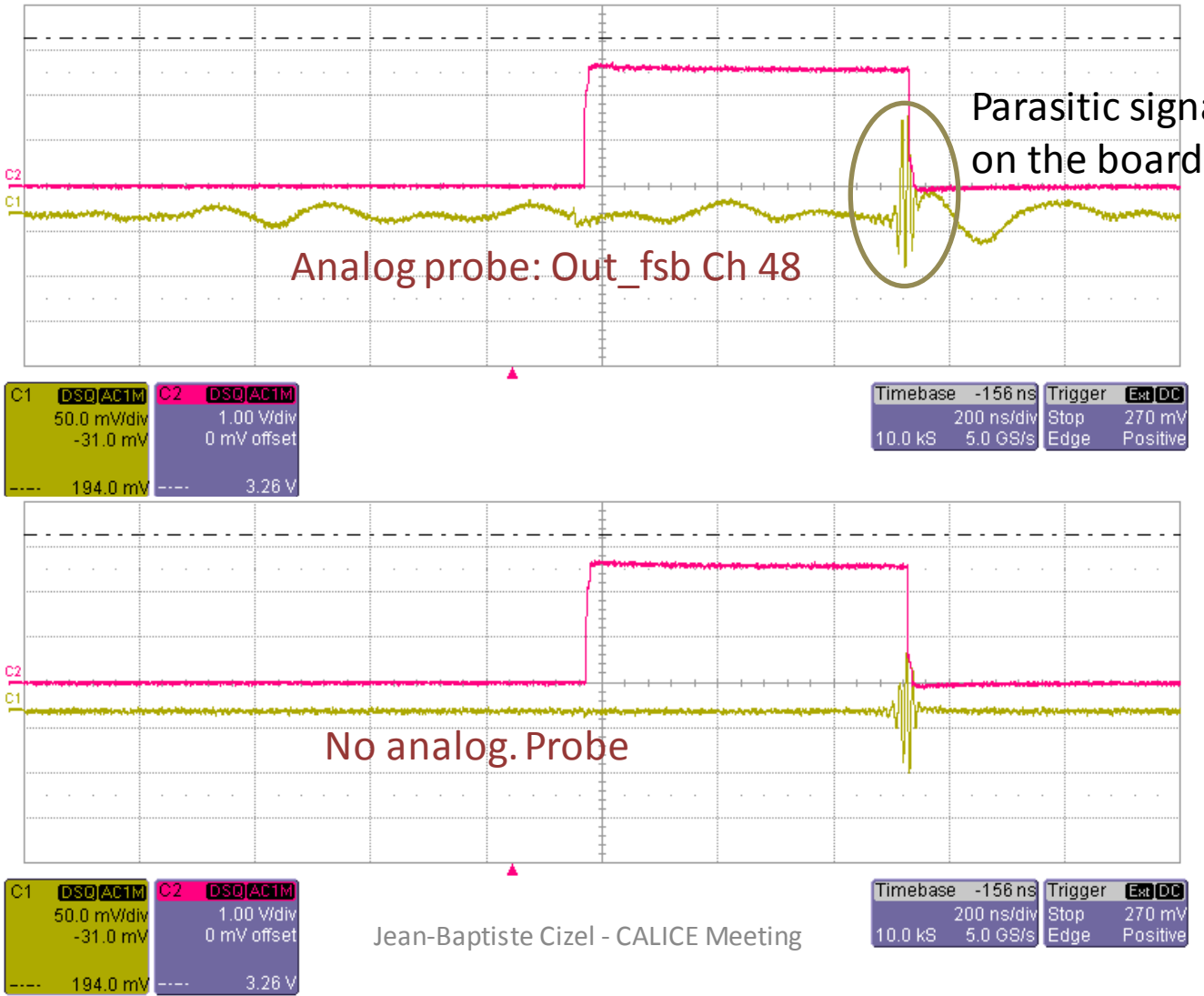
- 2000 MIP are injected in channel 2.
- Fast shaper output of channel 30 => 0,43 %



Digital crosstalk

Signal injected in all the channels except in channel 48

Effect of the discriminator outputs on the analog signals:

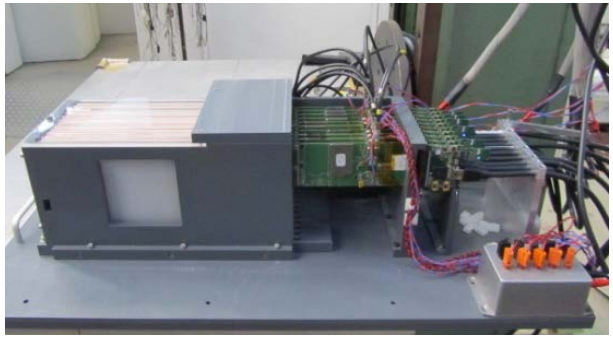


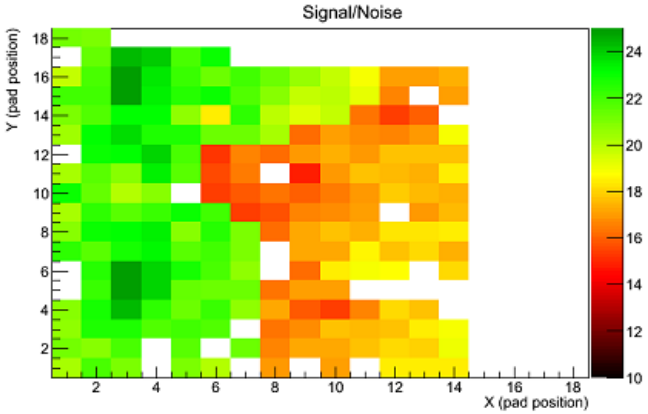
TESTBEAMs with SKIROC2

Courtesy
T. Frisson

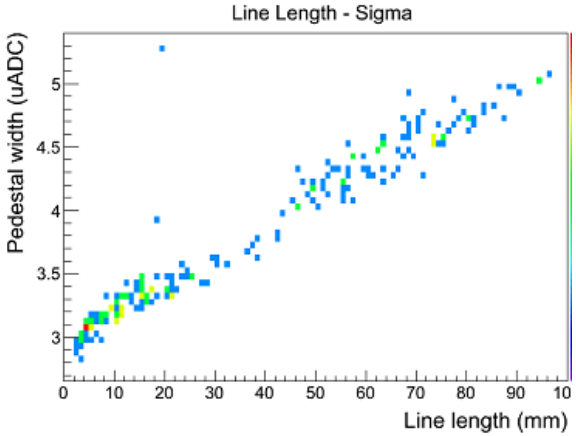
Successful test beams @ DESY in 2012 (1 to 6 layers) and 2013 (8 layers), power pulsing mode, autotrigger mode, e- (1 to 5GeV)

- ✓ 4 packaged skiroc2/slab
- ✓ Nice event displays



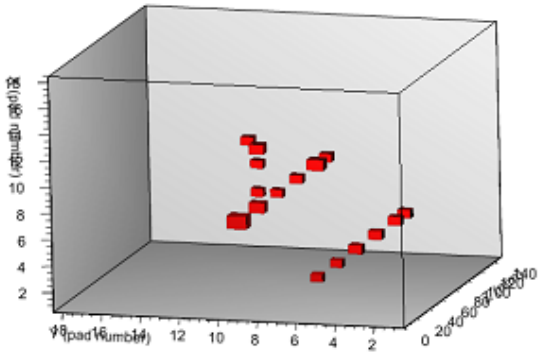


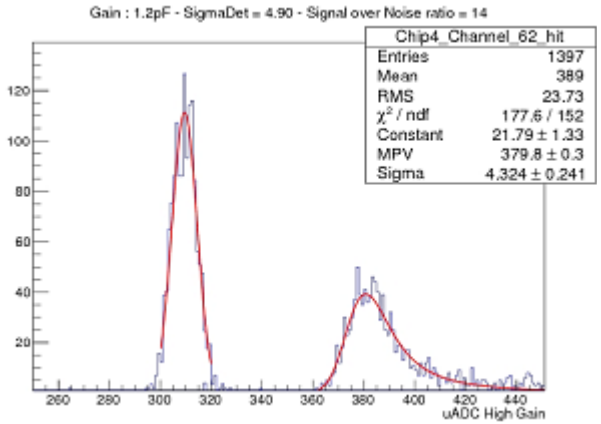
S/N > 10

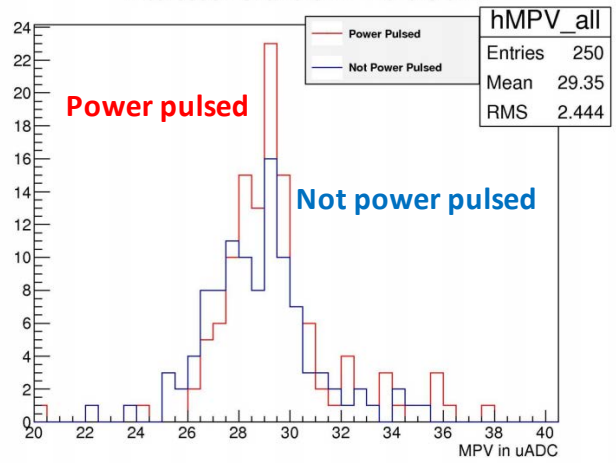


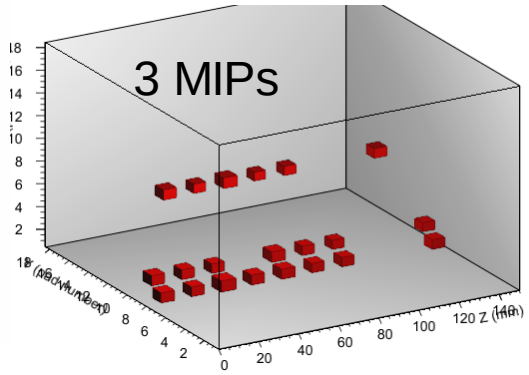
Beam is in the center of the detector

2 e- (3 GeV, no tungsten)



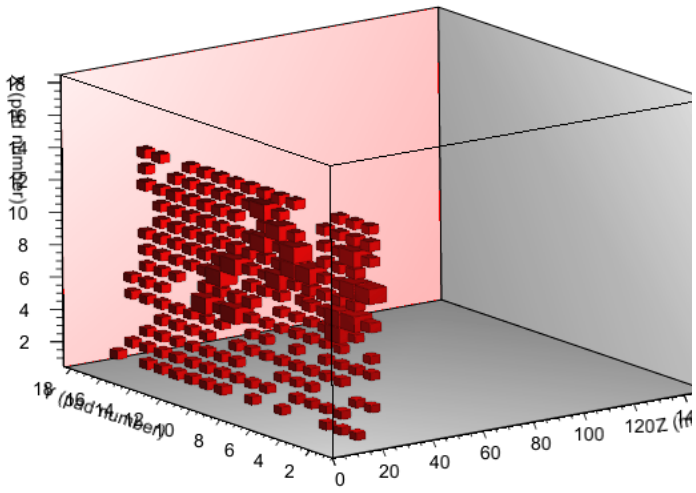


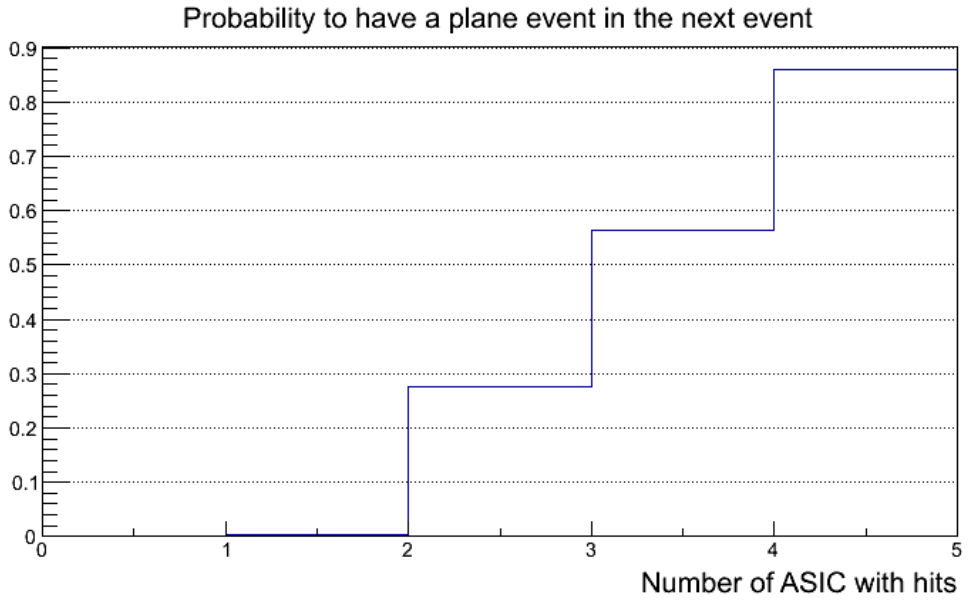




Plane events

Courtesy
T. Frisson





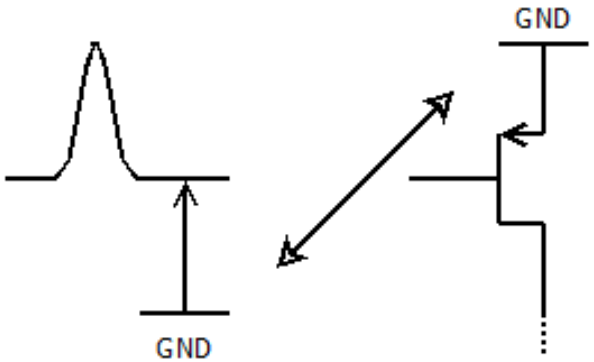
PA is referenced to the analog power supply

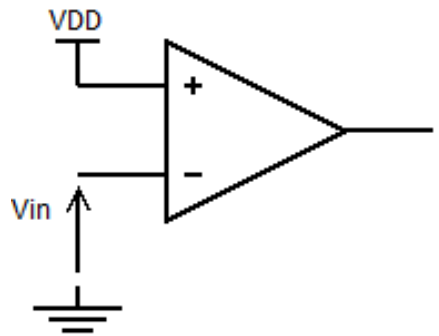
=> Sensitivity to Instabilities of power supply → fake events

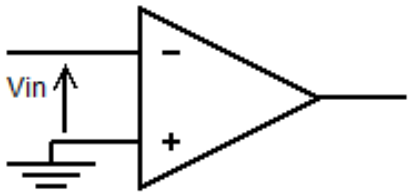
- Mistake: VDDD_delay/sca connected to analog power supply → increase instabilities of power supply
- Analog power supply common to the 4 ASIC
- Self-sustained → sometimes filled all the 15 ASIC memories
- Highly dependant of the number of ASIC with hits, dependant of the number of triggered channels
- **Issue solved when adding big decoupling capacitors on vdda on the existing FEV.**

New FEV design : power distribution

- Expected effect due to the preamplifier structure :
  - input PMOS transistor connected to analog VDD (successfully used for many years)
  - System on Chip with a lot of digital activity.
  - 64 channels => collective effects.
- Solution at system level :
  - use of GND as the positive voltage of the power supply
  - - 3.3 V as the negative voltage, we can solve the PSRR issue.
  - 2 new FEV with these modifications were made but wafers have been broken before any testing. One of these two FEV is under test at LAL.







Next steps (1)

Still **many measurements needed on SKIROC 2 on test bench and at system level** to identify and understand issues (which ones come from the chip and which ones come from the FEV/System?):

- Pedestal and signal stability versus number of hit channels
- Effects of the Power pulsing mode

Main modifications of skiroc 3 :

- The **64 channels** will be **independent**, meaning that only the hit channels will be memorized in the SCA
- I2C link for the slow control parameters

HARDROC 3 was submitted in Feb 2013 (funded by Aida). **Feedback tests** are necessary before submitting any other third generation chip.

Next steps (2)

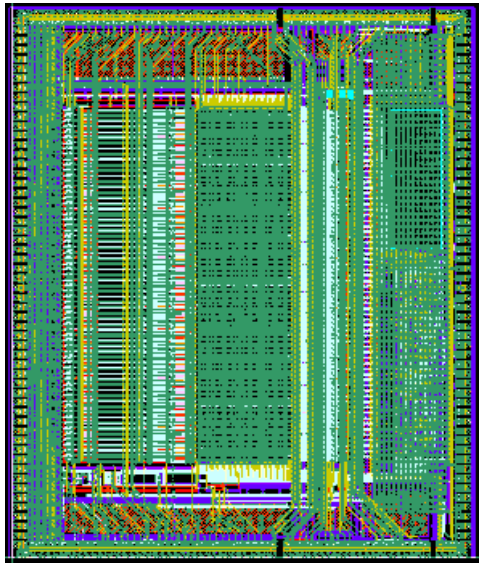
Plans to study a « SKIROC 2b » with similar architecture

- 64 channels
- Design in **XFAB 0.18 µm SOI HV technology** instead of AMS 0.35 µm SiGe
- Try to keep the **pin to pin compatibility**
  - Same FEV
  - Allows comparison of the results on test bench and at system level

Next steps (3)

Advantages of the XFAB 0.18 µm SOI HV technology :

- SOI -> less crosstalk via substrate
- Perenity ensured as it is used by the car industry
- Dimensions theorically reduced by a factor of 4 compared 0.35 µm. In practice : factor 2-3 expected
- Dedicated run compared to ams 0.35 µm SiGe
  -> Price/3 (to be confirmed)



SKIROC2 : 70 mm² => 70 k€ with AMS 0.35µm SiGe MPW run (proto)

Drawback: we never used this technology before => Building blocks might be necessary to be submitted before to check the technology: time consuming, test boards to be designed

Summary

- Still many measurements and simulations to be done on SKIROC 2

- Plane events are being understood: System effects on FEV boards (power distribution) to be confirmed with the results of new FEV boards.
- Plans to submit a SKIROC 2b in XFAB 0.18 µm SOI HV technology