Status of ROC chips

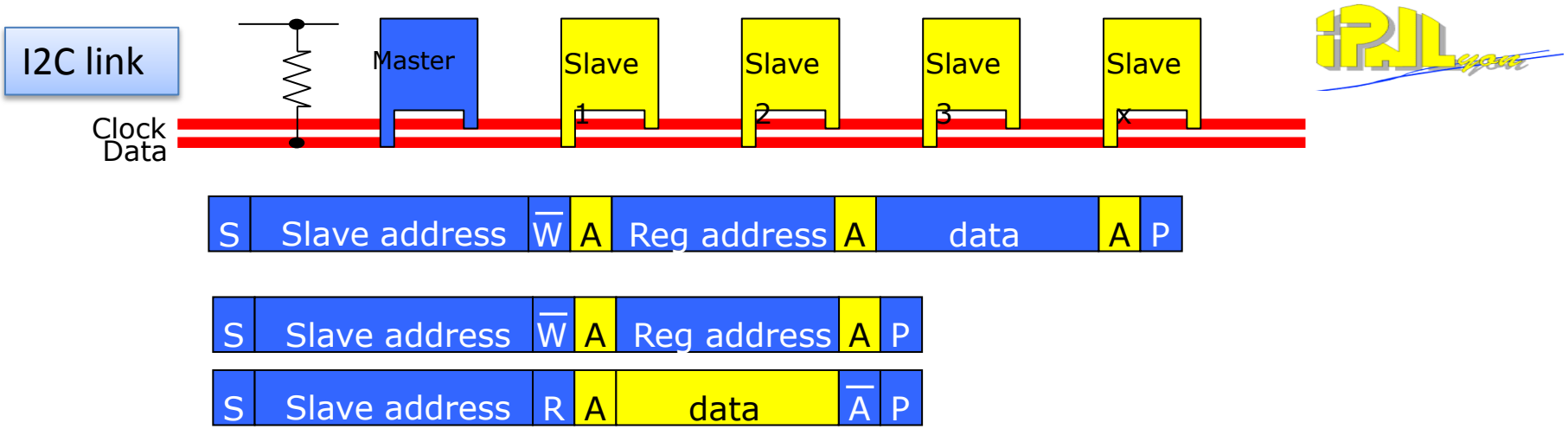
C. De La Taille for the OMEGA group

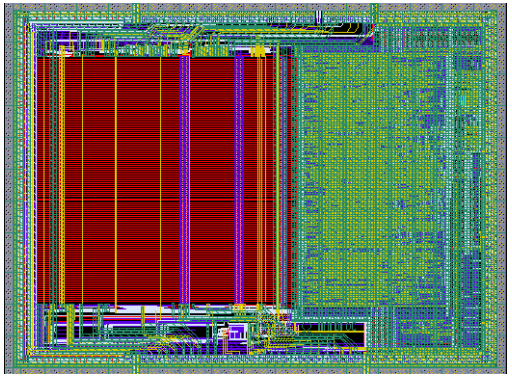
- 2nd generation ROC chips
  - Auto-trigger, analog storage, digitization and token-ring readout, common DAQ
  - Power pulsing : <1 % duty cycle

- 3rd generation ROC chips
  - **Independent channels (= Zero suppress)**
    - 64/36 address pointers
    - ReadOut, BCID, SCA (Spiroc and Skiroc) management

    => Digital part much more complicated
    - SCA depth: 8 instead of 16
    - Possibility to use "Roll mode" by Slow Control: circular memory very useful for Testbeam
    - New TDC with no dead time
  - **New Slow Control** (Triple voting) using **I2C link** (while keeping the « old SC » system)

- Geographical address on 8 bits
- 2 links for reliability





- No major modifications in the FE
  - submitted at the end of Feb 2013 (SiGe 0.35µm),
  - Received in June 2013
  - Die size ~30 mm2 (6.3 x 4.7 mm2)
  - packaged in a TQFP208
  - New PLL: integrated before in a builiding block, first measurements are very good : Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz available => **only slow clock distribution on ASUs**
  - New Bandgap : with a better temperature sensitivity
  - New Temperature sensor: tested in a building block, slope – 6mV/°C
  - Delay with testboards, expected end september

  - **HARDROC3 = AIDA Milestrone**
  - **2013: dedicated to the test of HR3 before submitting other chips**

- Technically feasible after HARDROC3 tests
- Expensive chips (area 40 and 100 mm2)
- Difficult tests : independent channels, zero suppressed !
- Remaining bugs in analog part will be much more difficult to investigate/understand
- New slow control : difficult to integrate with existing setup