Front End board for ECAL V9

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FEV8

We used FEV8_CIP until now (CIP = Chip In Package)

COB (Chip On Board = naked die bonded on the board) version exists but has flatness issue = problem to glue the sensor.

Improvements to be done concerning FEV8:

- FEV8 is referenced to GND while chip reference is 3.3V (nobody checked this…)
- On FEV8 some digital power supplies of the chips are wired to the analog supply
- The board has 4 chips only
- CLK lines are not good at long length

So, we took decision to design a new version : “FEV9”

- With a new version of adapter board (power supply, line drivers)
- Packaged chips : 400 balls BGA
- Fix reference, decoupling
- 16 chips
- Transmission lines for 2m & ~80 chips

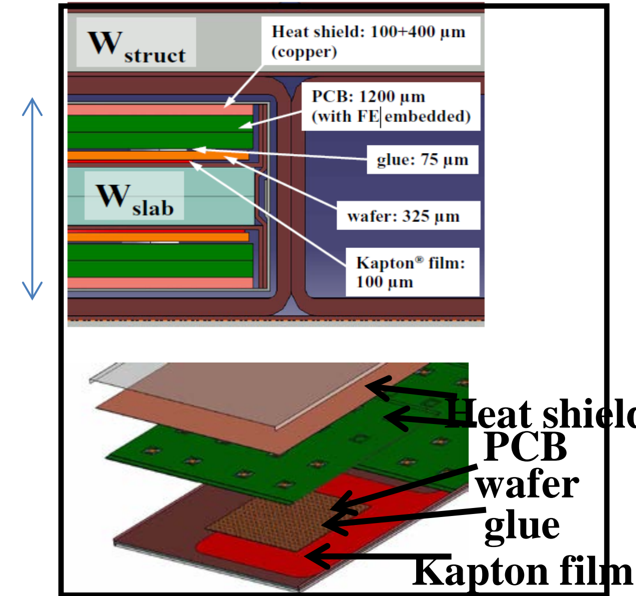
The board is being routed (finished by the end of the week)

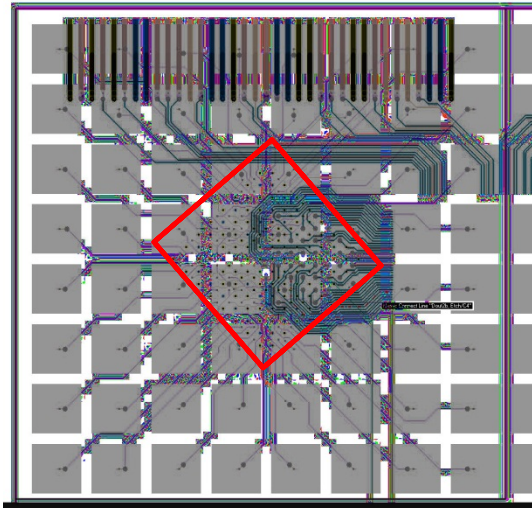
design of SLAB

SLAB design for FEVx_BGA has started

Same principle as before, 1 or 2 layer designs

Will be 30% thicker than with COB version



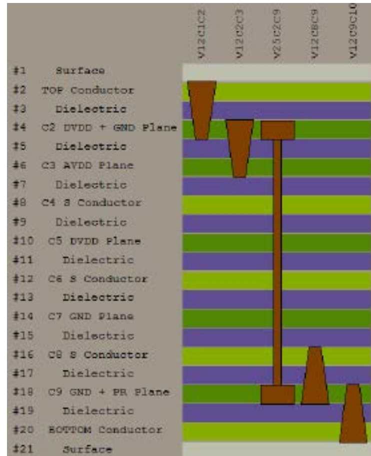


BGA pattern : 1/16th of the PCB

Advanced package technologies

- Longest analog trace is 2cm long
- Less risky 1.7 mm thick “classical” BGA (could be as thin as 0.9 mm)
- Allow efficient routing of pcb traces and digital/analog separation

FEV9 design



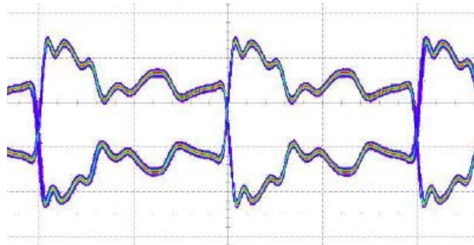
Symmetric stack will improve flatness, good for wafer gluing

Analogue signals shielded with AVDD

Digital traces shielded with GND and kept away of analogue (as much as possible)

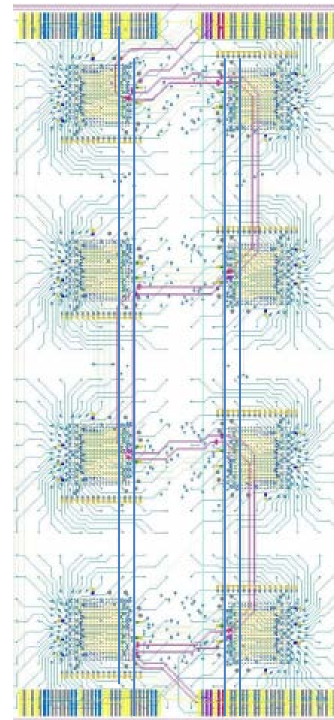
FEV9 1st version will implement two partitions of chips with differential signals routed with 2 options : straight lines (needs 2 times more buffers & connectors) or snake line (maximize load)

FEV9b is planned

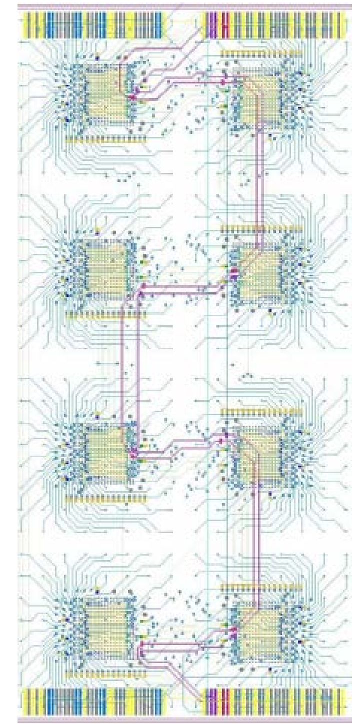


Measuring at the end of 2 FEV8…

Option 1

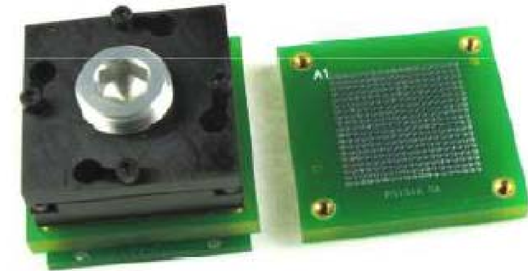


Option 2

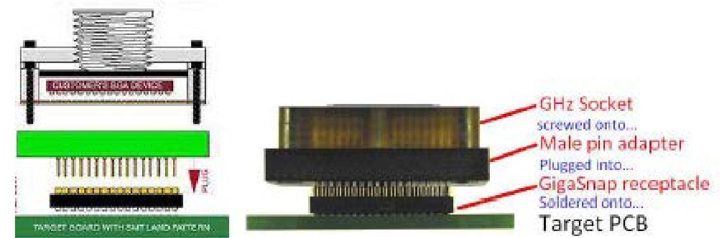


Chip packaging

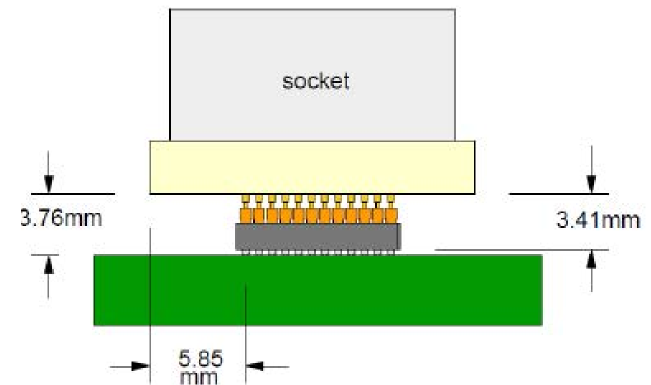
Pin mapping carefully made (S. Callier)
Digital and analogue well separated
Numerous power supply pins
Individual chip can be tested before soldering (not the case with naked dies)



Should receive 100 packaged chips by 1.5 month

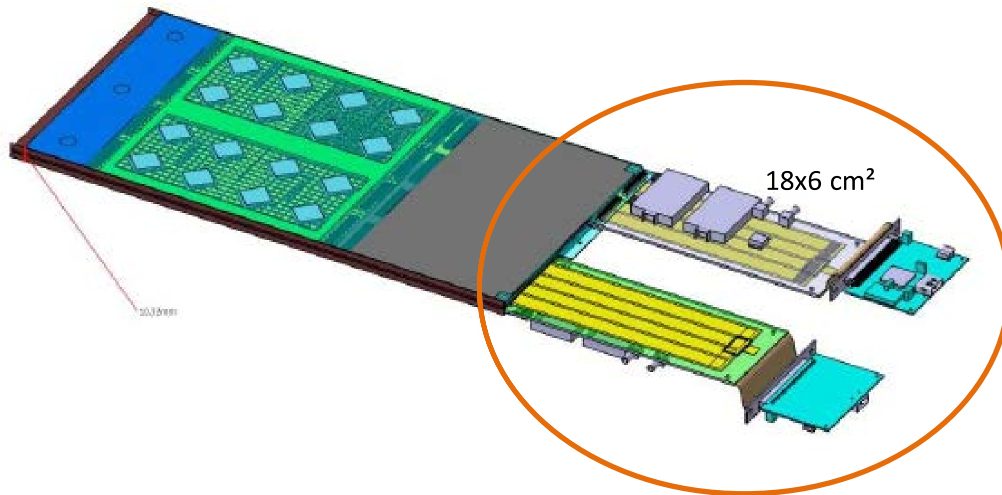


Will use test socket(s) at the beginning (1k€ each), it can be soldered on the same footprint



Then will have version with 4, 8 and finally 16 chips.

Next steps for SLAB



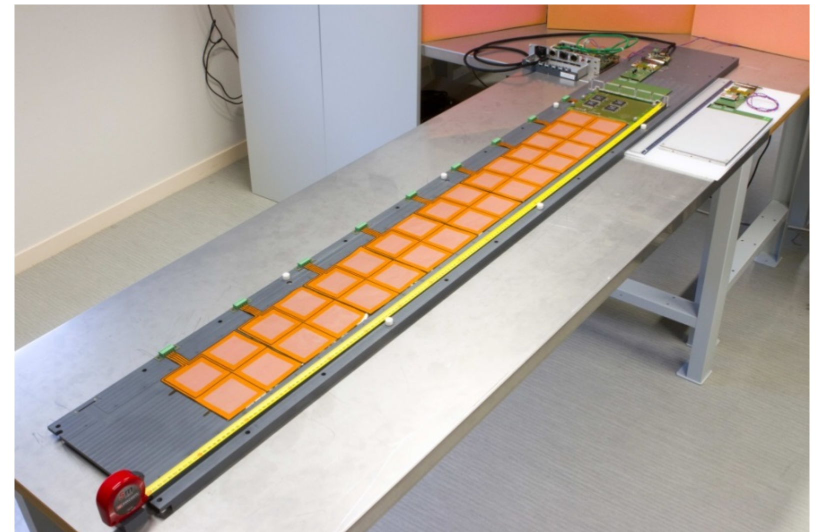
Have to work on front-end board:

- Power supplies (regulators, sequence)
- Local power storage
- line drivers
- Short SLABs will be of ‘U’ type
- Long SLAB will be of ‘aH’ type

(see M. Frotin’s talk)

It is urgent for us to test long slabs:

- Up to 10-12 ASUs long
- Complex transmission line
  - Loads
  - Stubs and connectors
- Power distribution
  - 12A pulses !
- Maintenance ?
- Test bed ready



Mid term goals

- Have one or 2 slabs with 4 chips+1 wafer for deep tests
- If correct, increase to 16 chips, 4 wafers (may require a FEV9**b**)
- Build a few slabs

- Assemble a long slab ASU per ASU up to ~10 ASUs on the test bed
- Characterize clock transmission along the slab + onen collector lines

- Then build a small-long slab of 5 to 6 ASUs

In parallel :

- Continue moderate effort on DAQ
- Prepare a compact version (one credit card) of the front-end board
- First look to boards integration in ILD
- Develop tooling for production at lab (gluing robot, assembly robot, test benches,…)

Schedule

- 20/09 : FEV9 order
- 20/09 : start designing adapter board (SMB V4)
- 25/10 : will receive FEV9
- 01/11 : will receive BGA chips
- 01/11 : cabling of test socket
- 15/11 : start test with SMB V3 and test socket
- 01/12 : routing SMV V4
- 15/12 : ordering SMB V4
- 01/01 : FEV9 + 4 BGAs
- Etc…
- 01/02 : 1 wafer glued
- 01/03 : FEV9b …