News about DAQ2

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What's new ?

The DAQ2 system has been successfully used during Si-W ECAL test beams (March & July'12, February'13). Up to : 1 PC+3 LDA+10 DIFs, ~2000 channels, 150 events/s, synchronization with CCC if several PCs are used (tested with 2PCs)

- Note : using 10 DCCs, the number of DIFs could have been 90 (~20k ch. of Si-W Ecal)

Small packet loss (from PC to DIF) can disturb the configuration process

- Can be difficult with increasing number of slabs
- SW procedures must be improved for robustness (capability to configure a part of the setup, FSM per component)

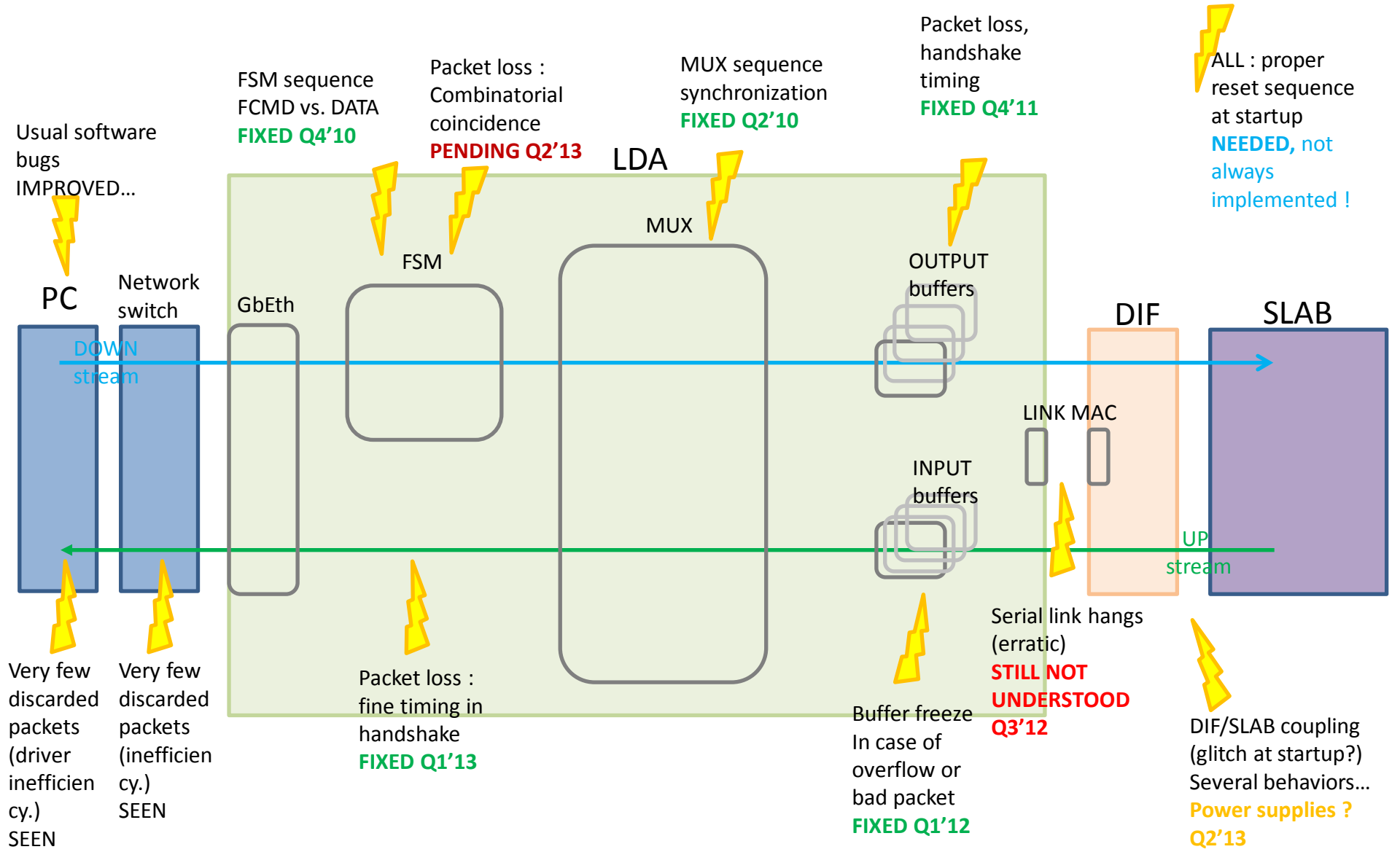
Have seen mutual influence between SLAB and DIF

- Erratic : not easy to understand
- Fixed separating the power supplies (were common in initial SLAB design)
- LDA-DIF link hangs sometimes (critical, need full restart)

New setup with GDCC used in July'13

- New "packet loss" bug due to different timing wrt. LDA (bug exists in LDA but was not detected, specific to internal FPGA routing, change with versions)
- Makes difficult the configuration step of a detector (a very small error makes the whole process failing)
- Being fixed (have a bug free firmware –temporary- : SAFE situation)

Where were bugs ?



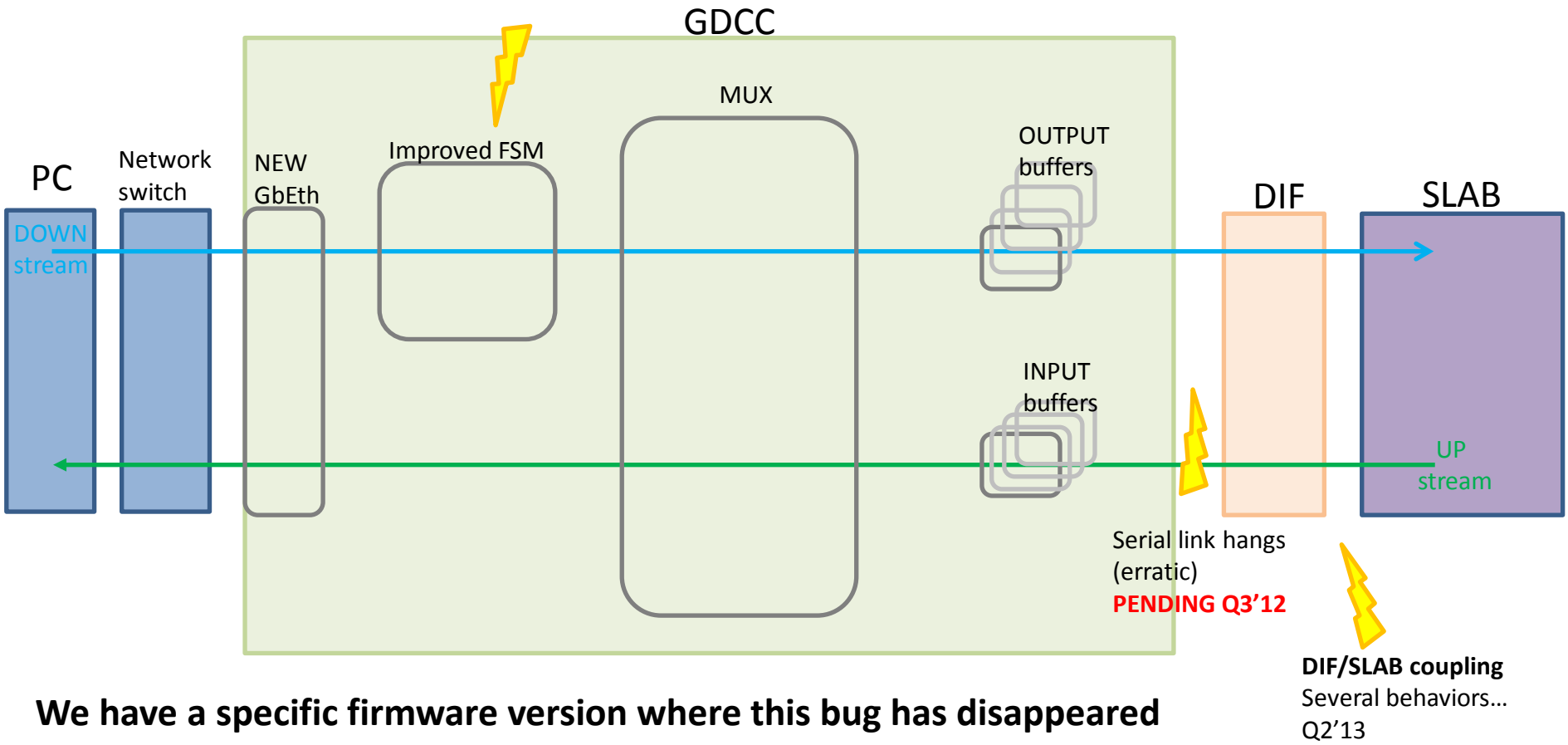
Debugging

- Upstream packets have been count everywhere using local & external stat. counters
  - Loss is residual (always the same number at DIF, LDA in, LDA out, switch in levels)
  - Upstream can be considered as SAFE
- Downstream : combinatorial timing is critical & implementation dependent
  - Small packet loss (orders/data not received at DIF level)
  - Makes configuration unsafe for large setups
  - Negligible in LDA
- DIF/SLAB coupling
  - several effects seen
    - Chips behavior do not correspond to config (even checked ok)
    - DIF enters in timeout
    - Links unlocked
    - DIF do not load correctly
    - SPILL signal required to restart/reload (!)
    - Etc…
  - Using separate power supplies helps to restart (DIF reset=power off)

- All these effects are **RARE**
  - but when cumulated in large setup, configuration or acquisition start is disturbed (software procedure do not allow incomplete configuration)
- Hope not to find other bugs

And with $GDCC_{LDA}$?

Re-use part of the LDA firmware, so it has the same bugs
Most of them have been FIXED for 2012 test beams
except the latter one, which is even more critical in the particular GDCC implementation



We have a specific firmware version where this bug has disappeared thank to a conjunction of good timings
Not considered as fixed

GDCC

LDA : Xilinx's GEMAC IP bloc is obsolete : code is no more supported.

- Only used for desktop test benches.

GDCC is now the replacement board (ECAL)

- **Can work at high SPILL rate (>100Hz, kevt/s)**
- Mezzanine for DIF connectors : allow future changes
- Discrete fan-out for clock and trigger
- Cost : ~1500€ proto (note: LDA prod =1600€)
- Have just received V1 (V0 had some layout errors)

GDCC firmware will be improved

- Preliminary $GDCC_{LDA}$ firmware is acceptable and implements all LDA functions
- Will add / rewrite functions :
  - UDP/IP
  - New & simplified FSM
  - Robust MUX & buffers
  - Synchronous structures
  - Removal of UK serial link under study

Still need mechanics to hold cables and pay attention to cabling
+ Reset system base on arduino board
Software components are to be improved

- Packet capture (some losses, negligible @10Hz spills)
- Framework Integration (XDAQ…)
- "Failsafe" procedures

GDCC V0

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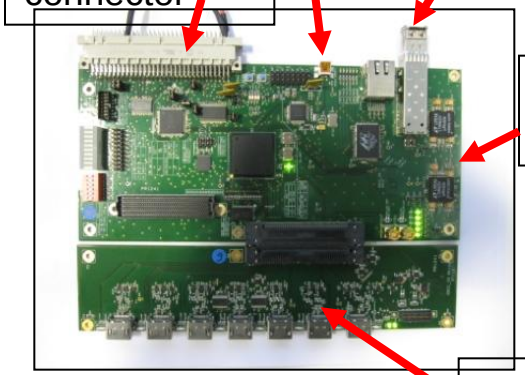
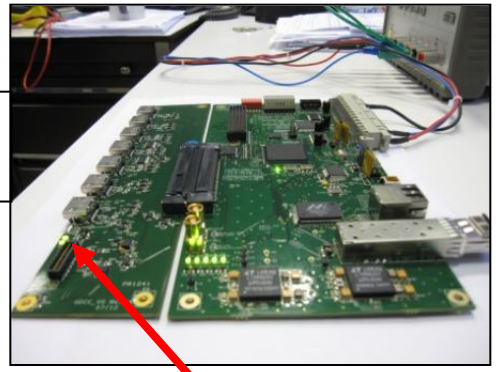
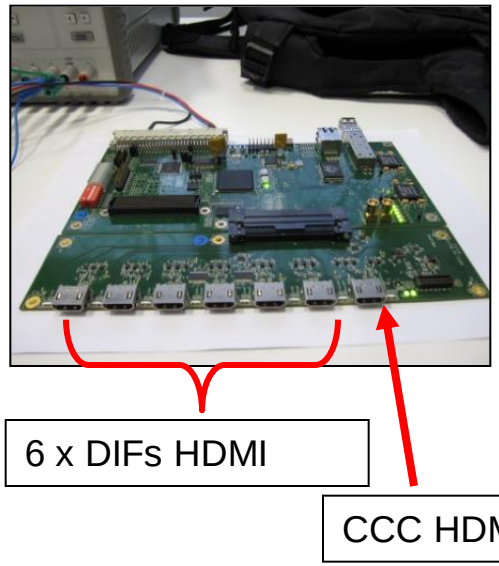
- 3 prototype boards have been produced and received at the end of 2012
- The PCB is made up of 2 boards: a main board and a mezzanine (HDMI connectivity)

GDCC
12 layers
Size : 233 x 106.66 mm
Thickness : 1.81 mm

Mezzanine
12 layers
Size : 233 x 52.8 mm
Thickness : 1.81 mm







Setup tests at LLR (V0)

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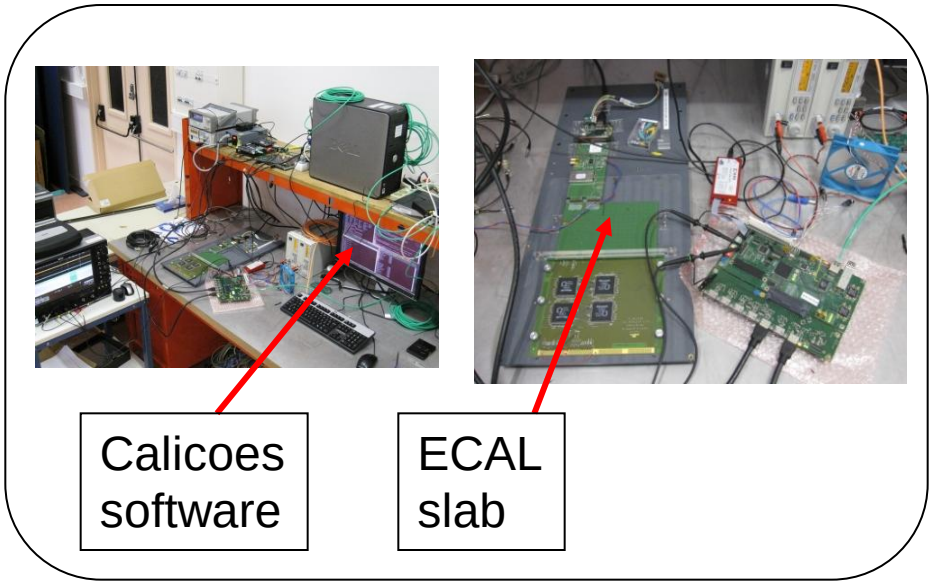
Used with Calicoes software – GDCC connected to one slab

First few bugs have been resolved during the basic tests

- Mainly on PCB routing
- After several tests with a slab, we have observed a packet loss between 1 and 2 % (fixed)
- When a DIF packet close of the max length (1kB) is follow by small packet, we lose the Ethernet preamble part (0x55) and the 2 packets are merged. This bug is now fixed.



Cosmics tests at LLR

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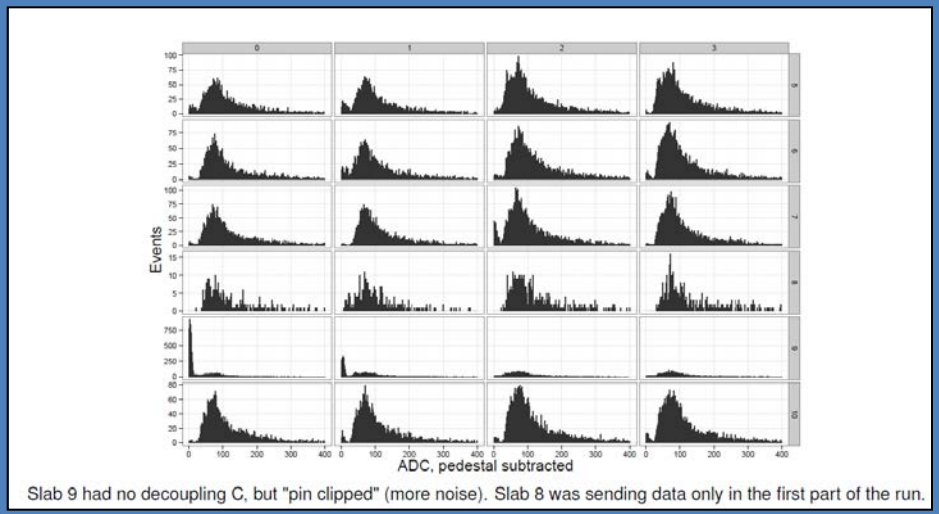
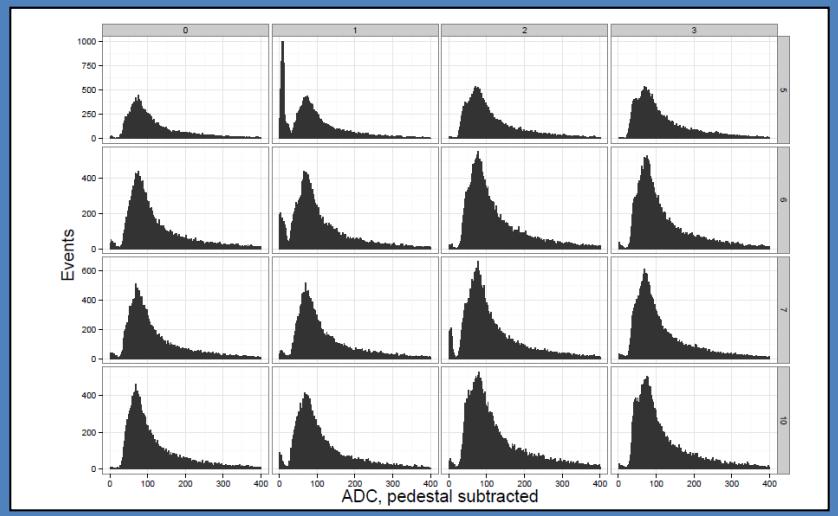
- Tests made in May
- Run with all 6 GDCC channels

From Balagura slides shown at ECAL meeting in June



Slab 9 had no decoupling C, but "pin clipped" (more noise). Slab 8 was sending data only in the first part of the run.

Run with spill rate 50 Hz ***(impossible with a LDA)***



GDCC V1 Status

July'13 Test beam at DESY has been made

- 2 GDCC V0 and 1 LDA has been connected
- 4 and 3 slabs on the 2 GDCC
- 1 slab on 1 LDA

DAQ ran after some difficulties configuring

the detector due to the "downstream packet loss" bug

- This problem is currently under investigation
- Reset controller was not in service

3 new GDCC V1 boards received last Wednesday, mezzanines returned to the company due to missing components, tests OK (PC-GDCC-DIF)

- Improvement about the mechanical aspect.
  - Improvement of the HDMI connectors (screwed onto front panel) 
  - Improvement of the mezzanine connection (mechanical adjustment with the samtec connector)
- Improvements of the routing
  - Minor modification to fix footprint bugs and few un-routed signals
  - Minor modification improving signal integrity

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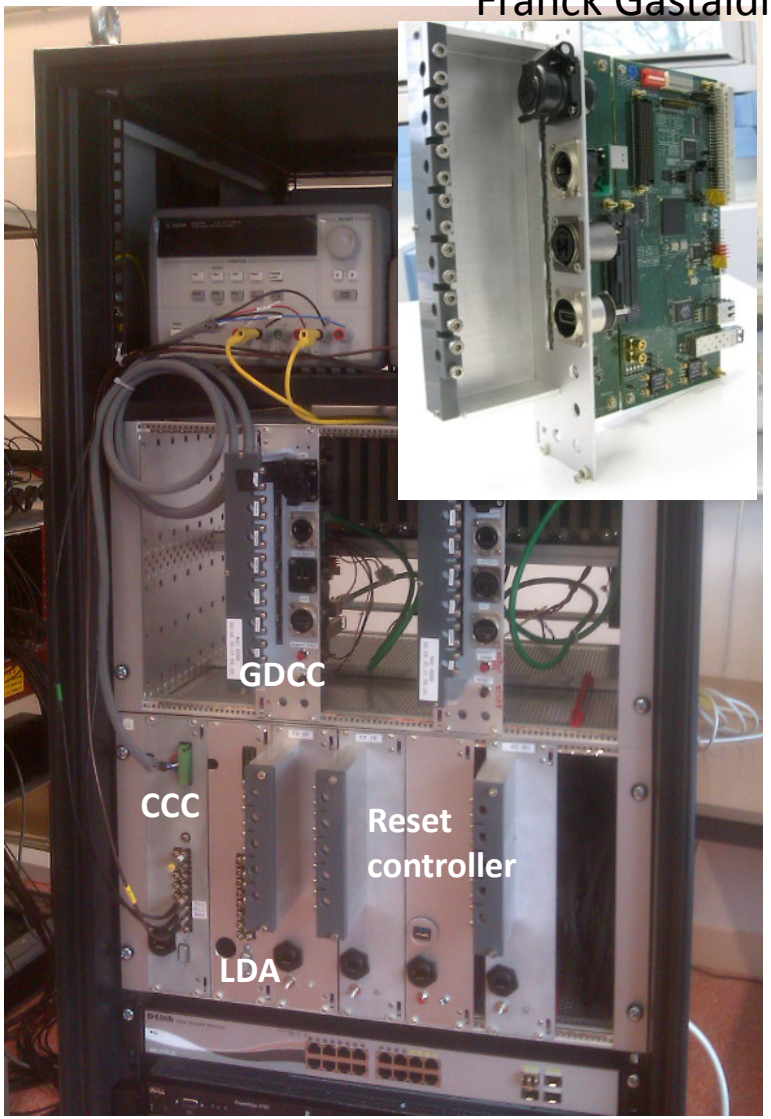

Conclusion

Many bugs fixed since Q2'10, the trickiest of them are remaining and are under investigation (need very specific tests, not easy to perform)

Trend for removing as much as possible of original components step by step (20% removed now in LDA/GDCC)

(would have preferred to rewrite everything from scratch if we had no test beams to prepare)

Overall system is acceptable to run ~10 SLABs, stable once started (had performed hundreds of configurations to get "S curves", weeks of data taking…).

Slow but constant progress for overall improvement

Others :

CCC : Fast Ethernet being added for 60€ (commercial module)

Will use a physical reset generator based on arduino module (relays controller).

Questions ?