

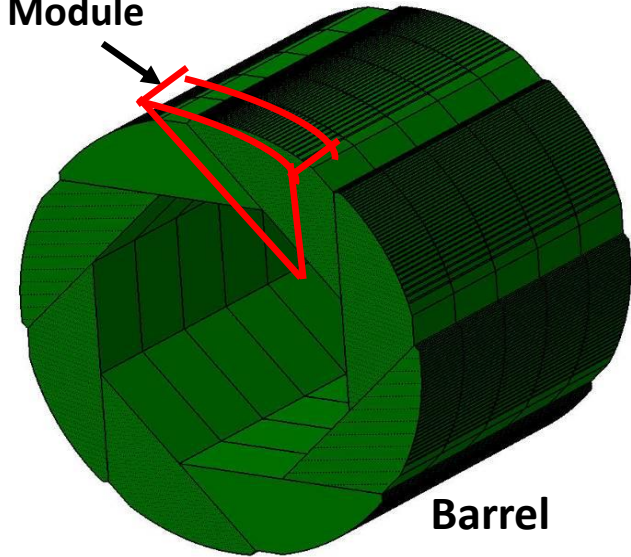
# SDHCAL R&D status

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On behalf of the SDHCAL-GRPC groups

# Beyond SDHCAL technologic

Module



Mechanical structure proposed  
SDHCAL for ILD is made of 48-  
detector module.

A prototype with 48 GRPC of 1 m<sup>2</sup>  
was conceived and realized as a first  
technological demonstrator

Then what next?



# Road map beyond the DBD

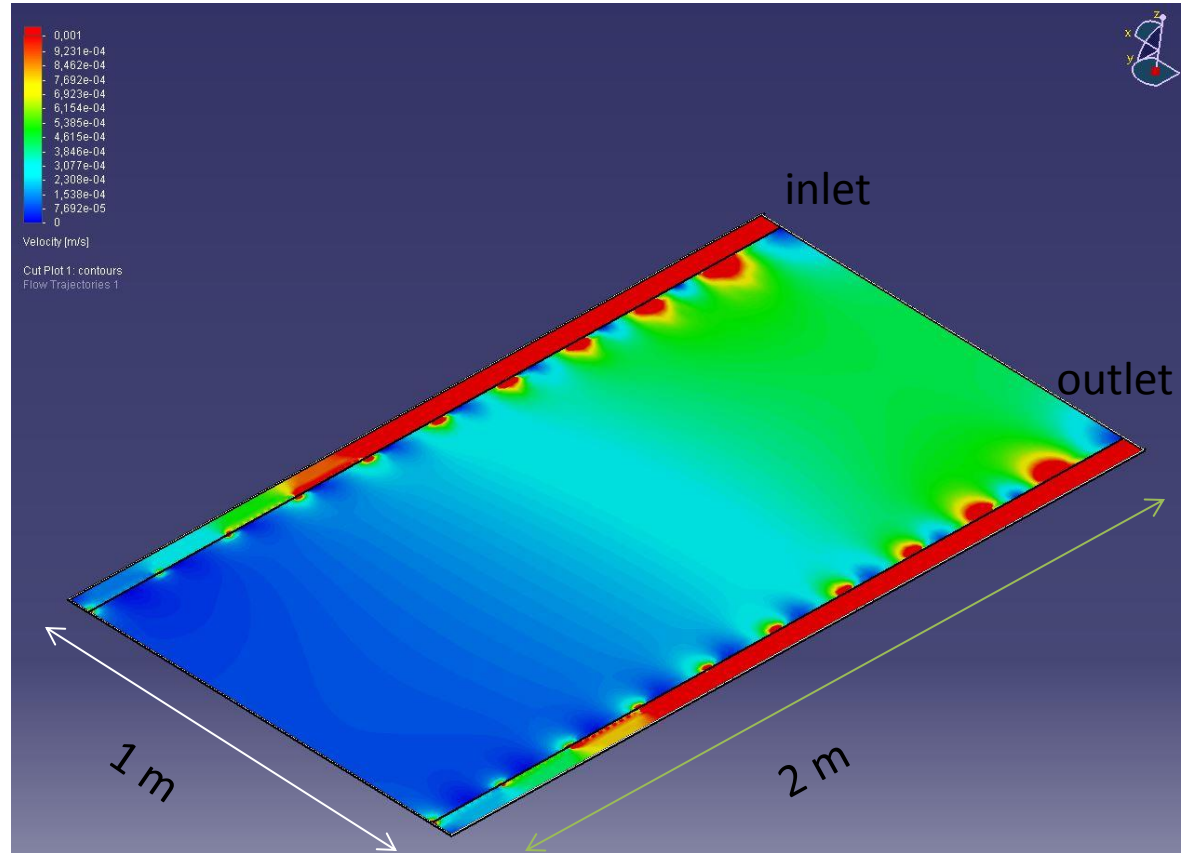
- 1- Build few very large GRPC detectors (2-3 m<sup>2</sup>) : Gas circulation system, thickness...
- 2- Improve on the readout electronics (I2C, roll mode..)
- 3- Design a new ASU capable to read the large GRPC (up to 3 m<sup>2</sup>)
- 4- Develop a new DIF ( low consumption, reduced size, new functionalities)
- 5- Build a small mechanical prototype to host the few large chambers

Large GRPC for ILD:

GRPC with a surface  $\leq 3 \text{ m}^2$  are needed.

We intend to build a  $2 \text{ m}^2$  GRPC (glass are already there).

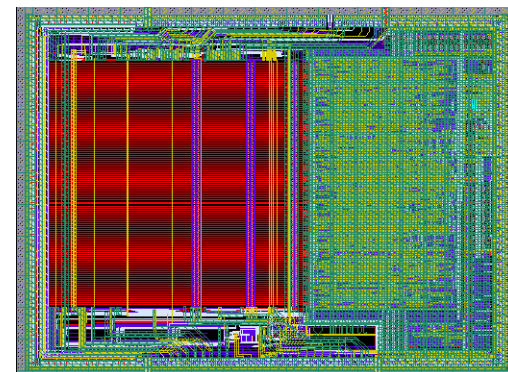
We are currently studying the gas distribution system to ensure a good gas renewal.



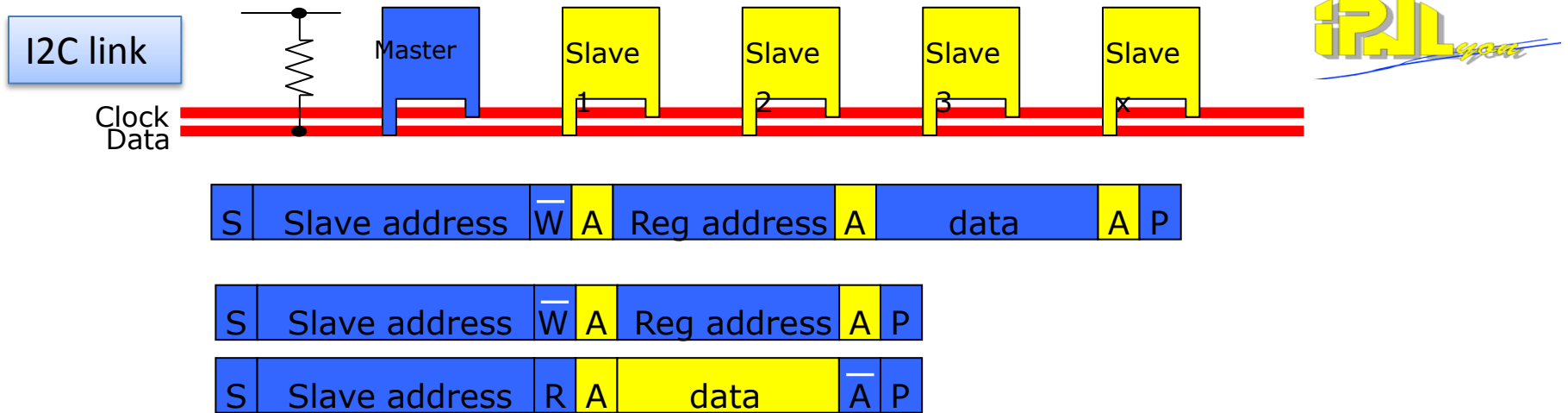
## Readout electronics :HARDROC3

Main issue: To communicate with each ASIC

- **64 independent channels**
- **I2C link (@IPNL)**
- PLL: integrated before in a building block, first measurements are very good
  - Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz available
- Bandgap: new one with a better temperature sensitivity, tested in a building block
- Temperature sensor: tested in a building block, slope – 6mV/°C
- Die size ~30 mm<sup>2</sup> (6.3 x 4.7 mm<sup>2</sup>)
- To be packaged in a TQFP208
- Test board is designed and being produced
- Tests to start soon.

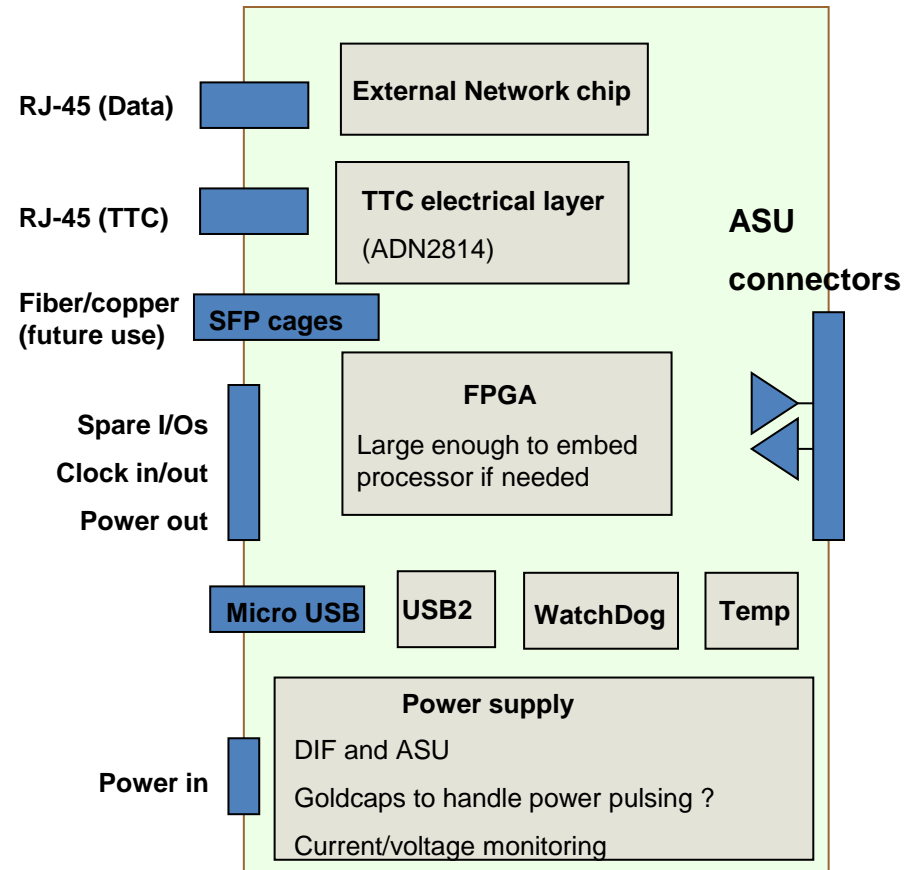


- 3<sup>rd</sup> generation ROC chip
  - Independent channels (= Zero suppress)
    - 64/36 address pointers
    - ReadOut, BCID
  - ⇒ Digital part much more complicated
  - ⇒ Possibility to use “Roll mode” by Slow Control: circular memory very useful for Testbeam
  - New Slow Control (Triple voting) using I2C link (while keeping the « old SC » system)

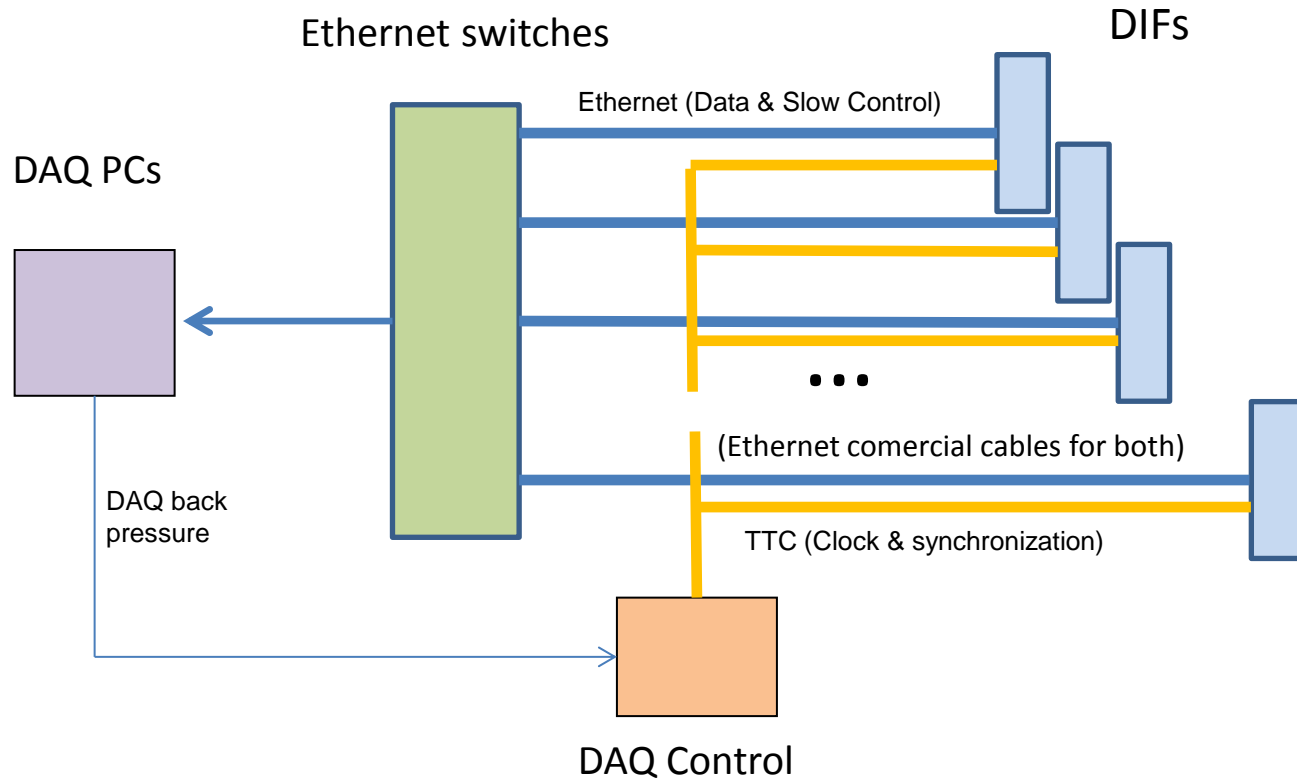


# DIF: Designed for ILD SDHCAL

- Only one DIF per plane. For the maximum length plane (1x3m) the DIF will handle 432 HR3 chips
- Slow control through the new HR3 I2C bus
- Data transmission to DAQ by Ethernet using commercial switches for concentration
- Clock and synchronization by TTC
- USB 2.0 for debugging



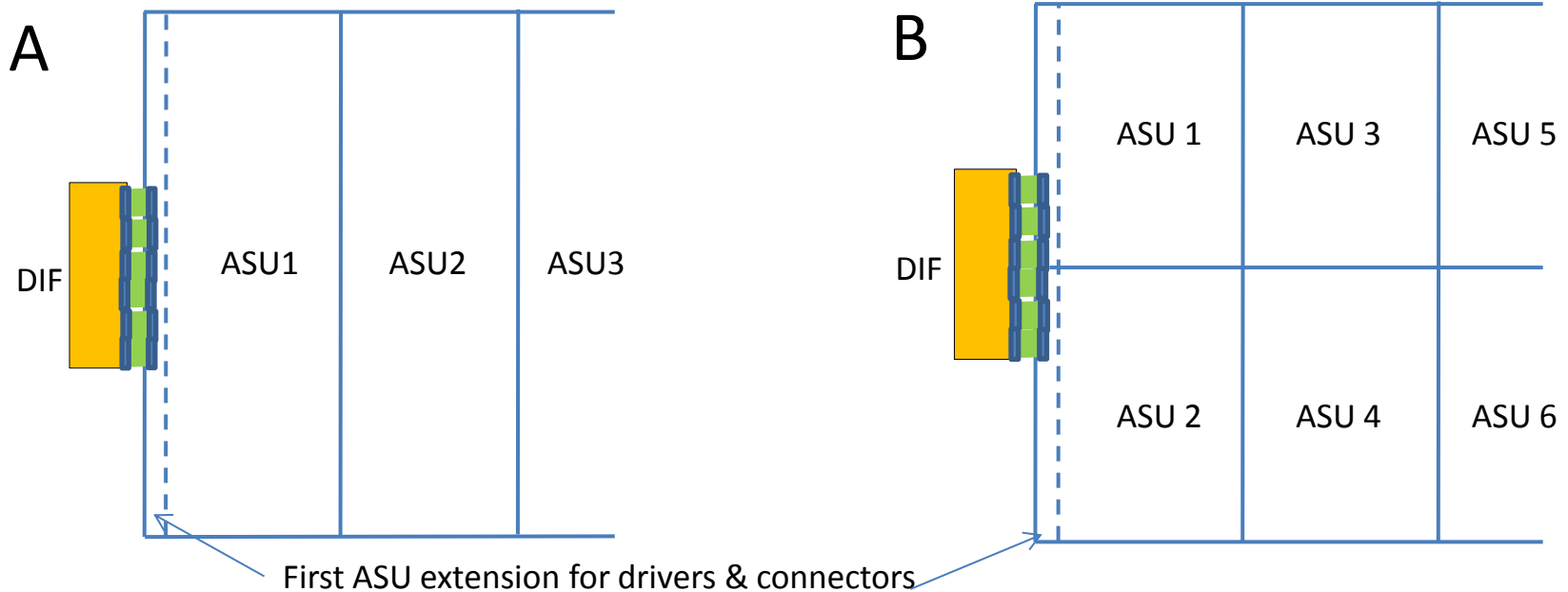
# New SDHCAL DAQ architecture





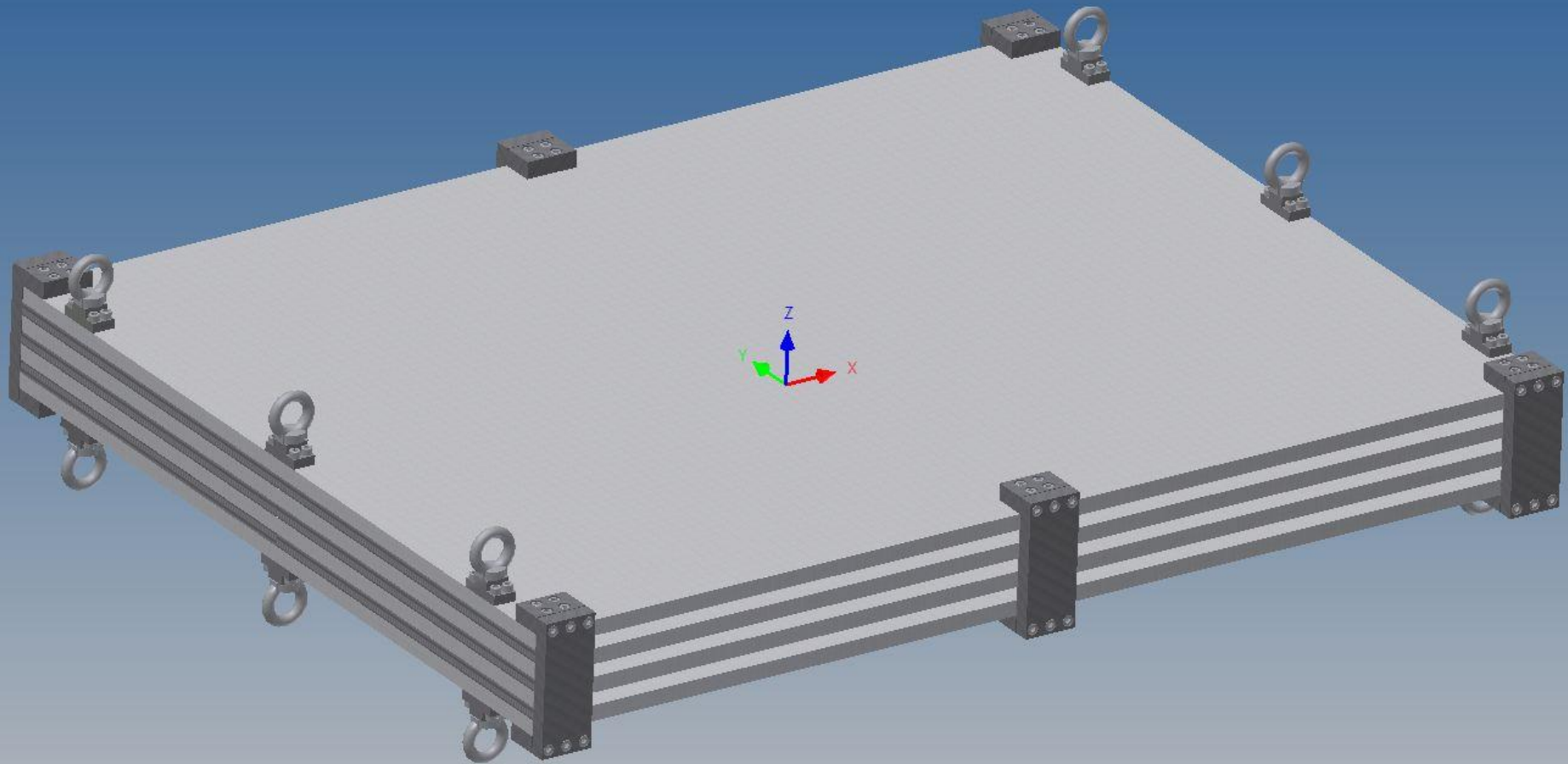
# New ASU layout options

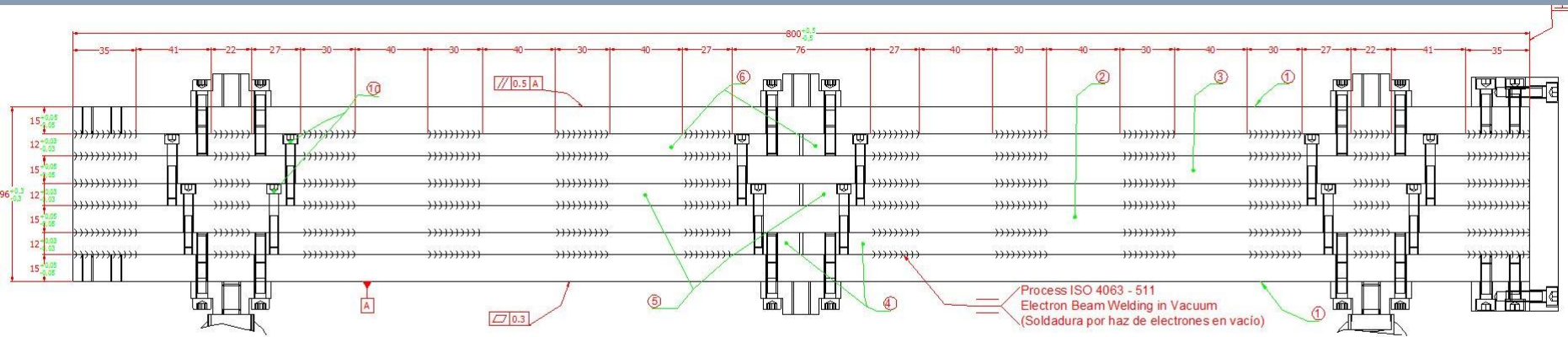
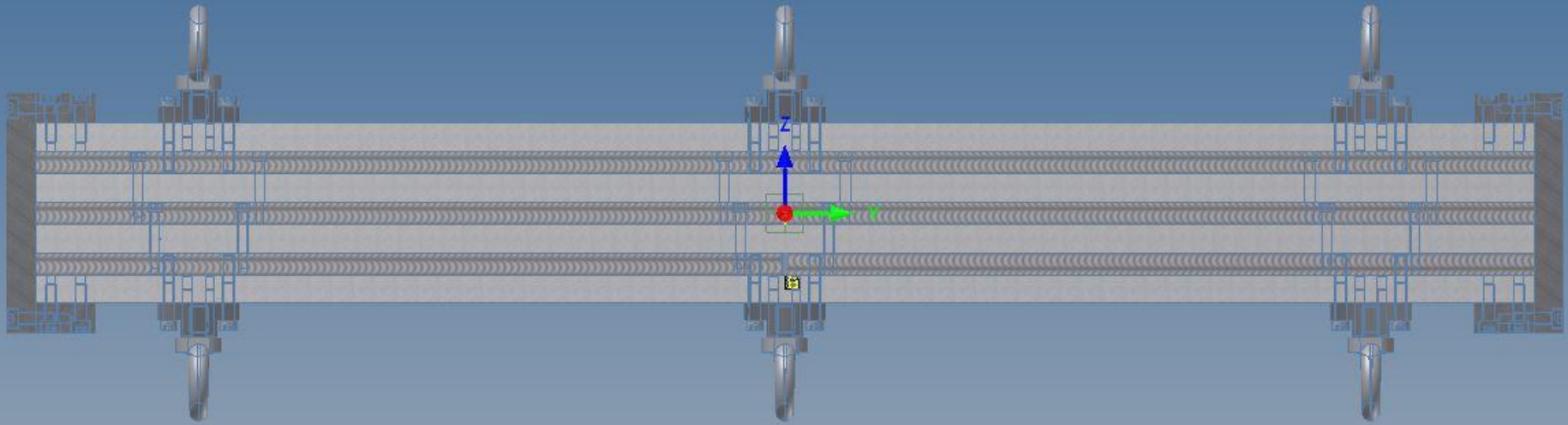
As there will be only one DIF per plane, the distribution of the ASU boards in the plane will be rearranged to reduce the number of connections between the DIF and the plane



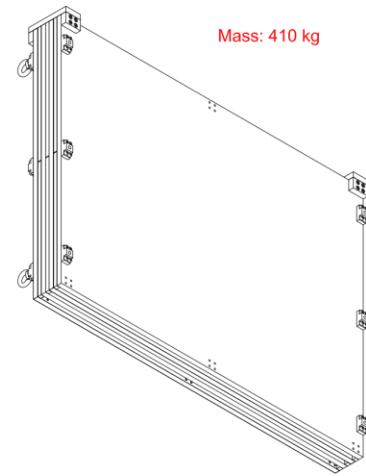
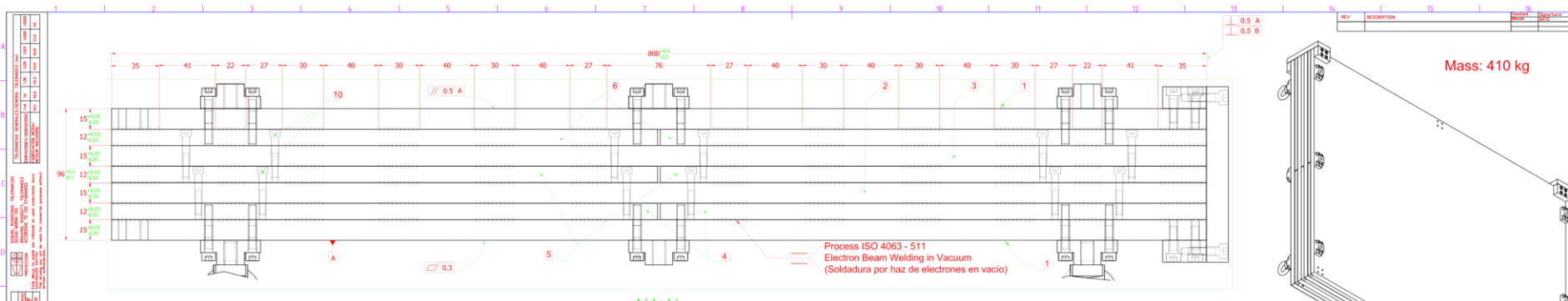
- In option B the common signals for the plane have to be sent twice (one per slab) while in option A they can be sent only once
- But, option A looks more risky from the point of view of the feasibility of the 1m long ASU boards.
- In both options the ASUs connected to the DIF will be a bit longer to host the connectors and the buffers for driving the long lines. This extension provides more freedom for the connectors selection and moves the drivers heat dissipation to the ventilation area

# Self-supporting mechanical structure



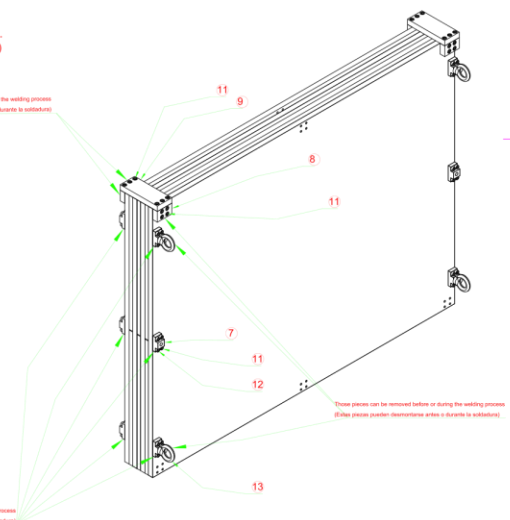
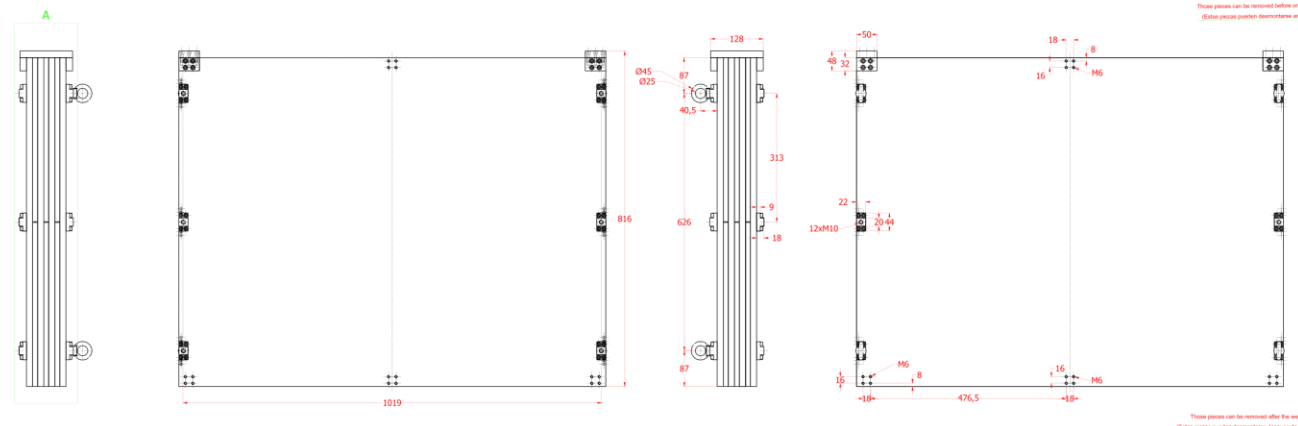
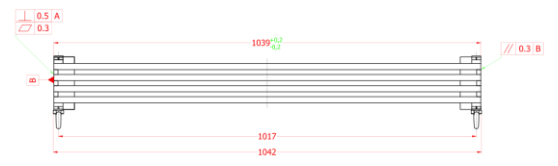


Made by Electron Beam Welding process in Vacuum.  
Welding deep of 5 mm.



Made by Electron Beam Welding process in Vacuum.  
Welding deep of 5 mm.  
(Realizado mediante soldeo por haz de electrones en vacío.  
Profundidad de la soldadura de 5 mm)

Do not break sharp edges and prepare for Electron Beam Welding process in Vacuum.  
Clean for this process and protect in hermetic double bag.  
(Dejar esquinas a 90° y preparar para soldadura por haz de electrones en vacío.  
Limpiar para este proceso y dejarla protegida dentro de doble bolsa hermética )



Setup for use.  
(Disposición final de utilización)

Rest of tolerances according Norm ISO 2768-1, Class m.  
Resto de tolerancias según Norma ISO 2768-1, Clase m.

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# Conclusion

- The work on large detector GRPC for ILD is ongoing but at low
- The HARDROC3 test results will determine the pace of this whole readout R&D chain in the future months.
- The detector conception and realization should be achieved soon.