SiW ECAL status and beam test in July

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Outline

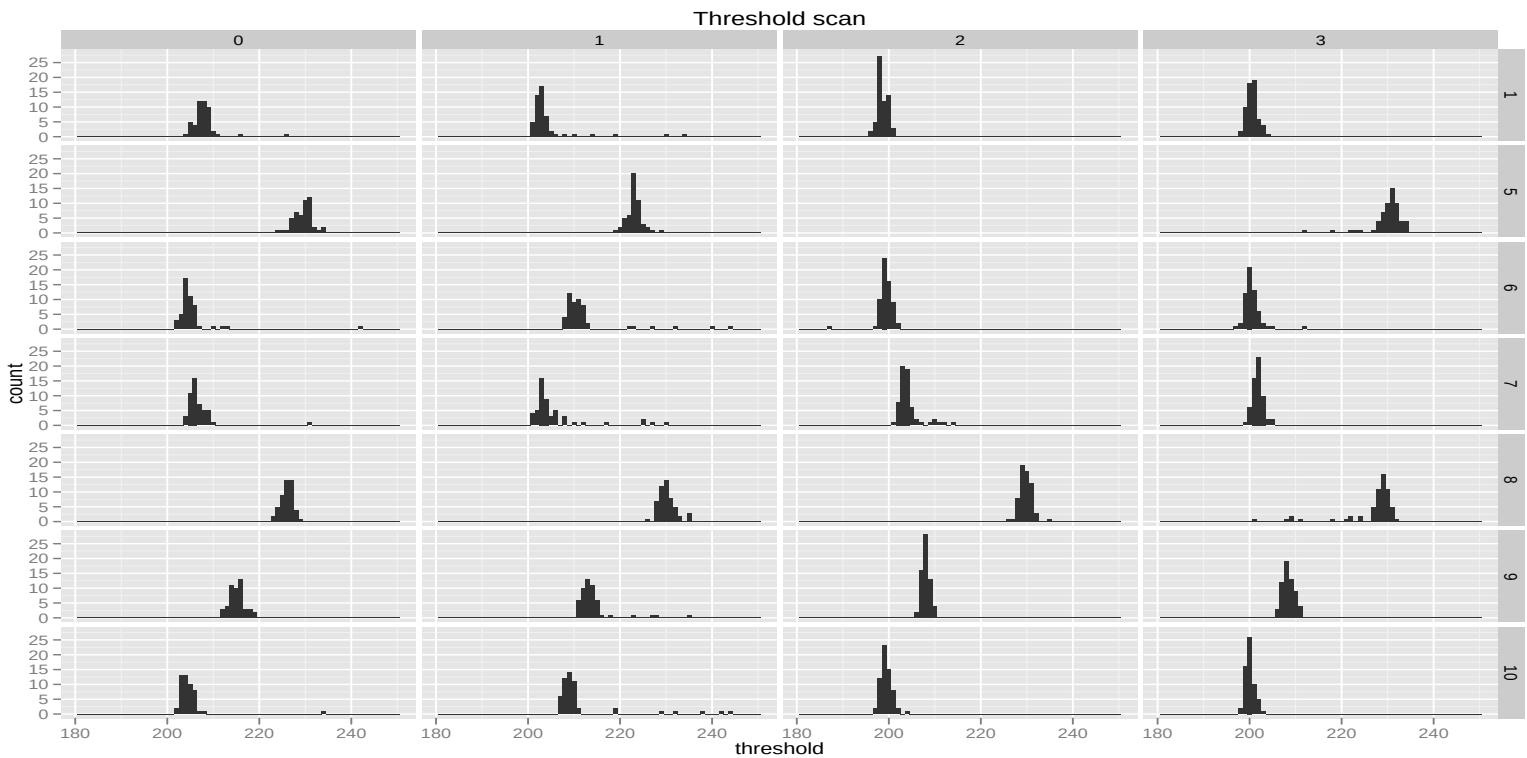
Topic

Improvement due to decoupling capacitances

One triggered channel may fire a sequence of multi-channel triggers in successive bunch crossings. Caused by noise in SKIROC power lines. Can be reduced by decoupling capacitances and (less important) by fixing PCB bug (swap of analog and digital voltages).

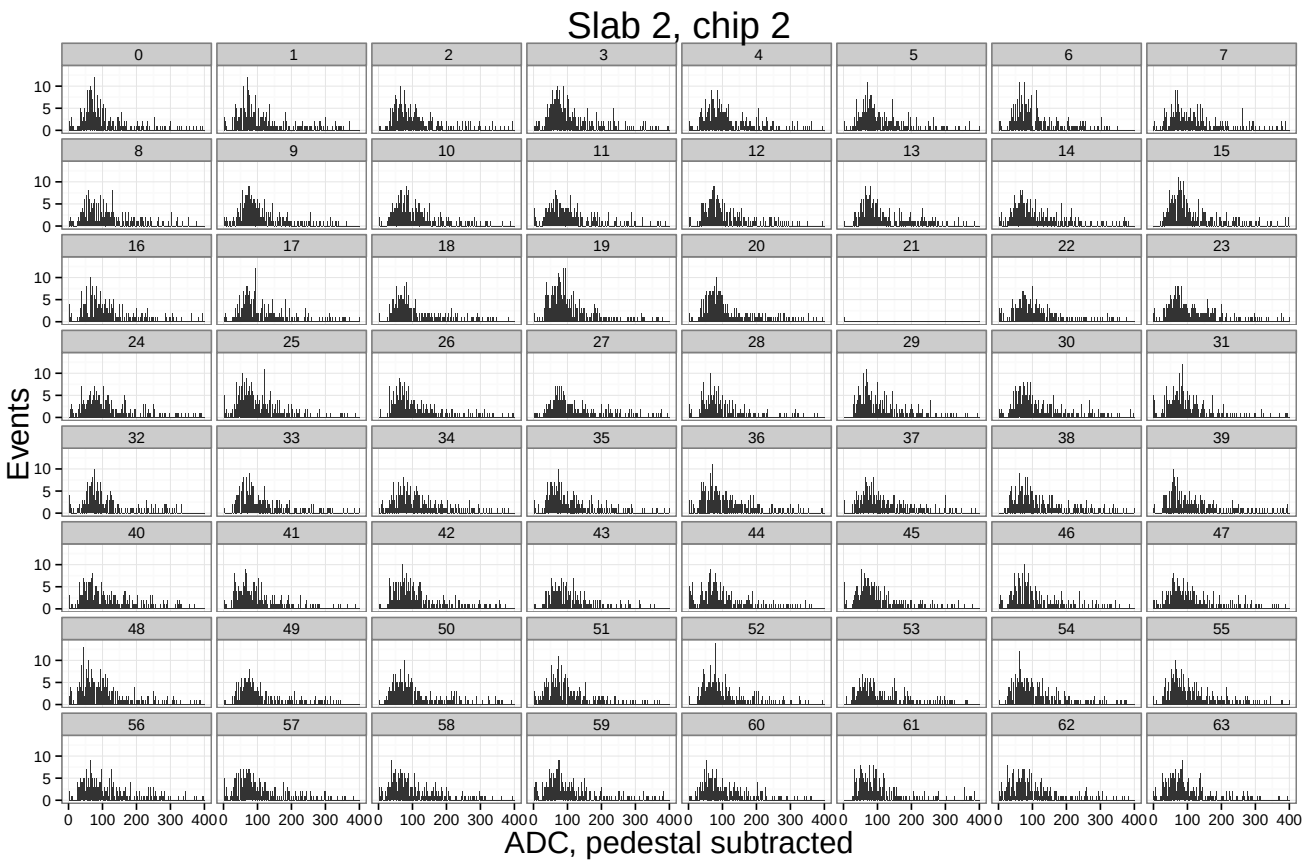
May 1 automatic trigger threshold scan, 4 chips X 7 slabs (hist. entries = chip channels)

- Slabs 5,8 not modified (worst, highest thresholds),
- 9 with fixed PCB bug, no decoupling C (improved)
- 1,6,7,10 with decoupling C, with PCB bug (best)



Cosmic run

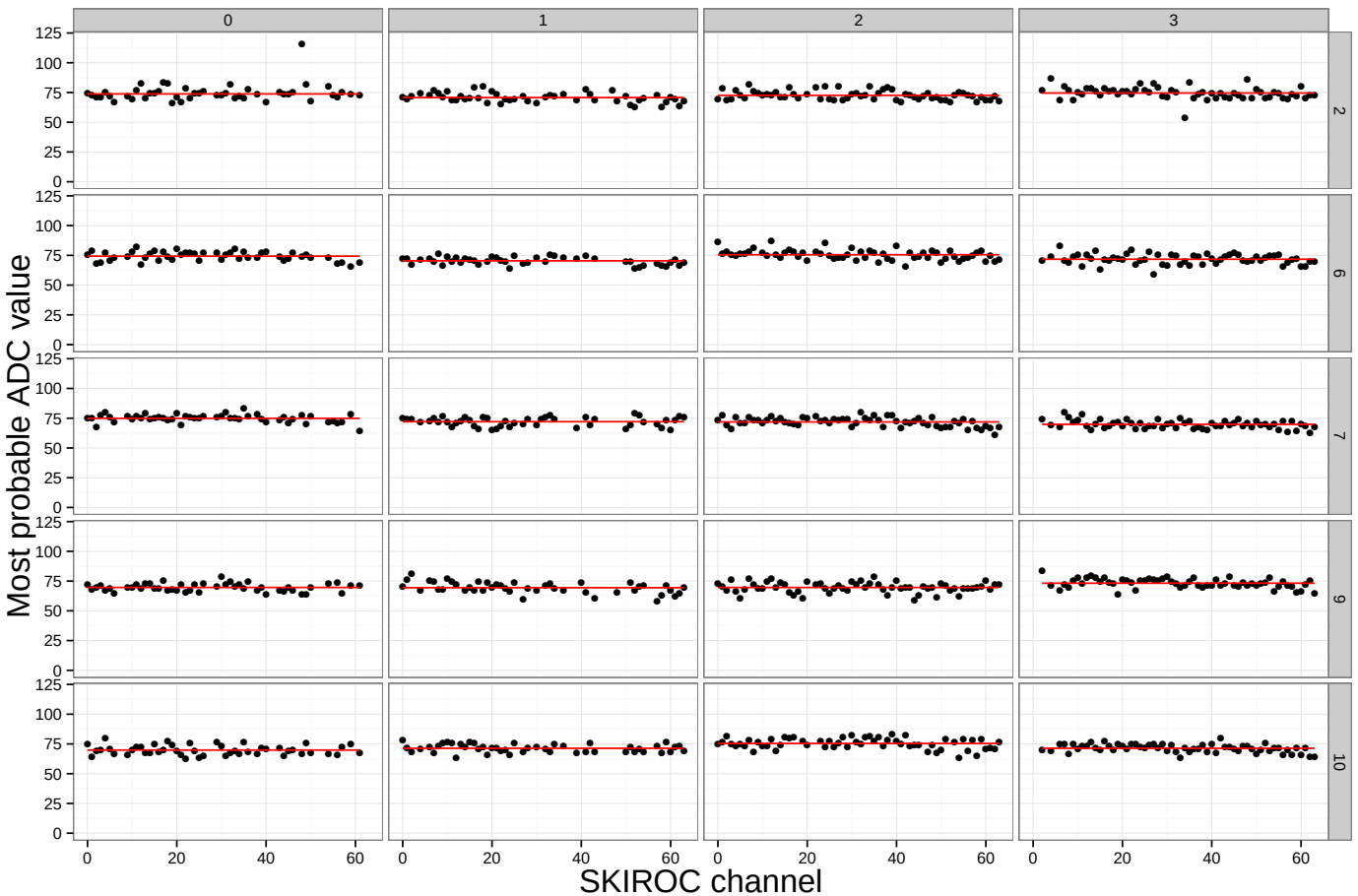
In the past, without decoupling C no good cosmic signals: power line noise fills up SKIROC memory before first muon arrives.
Low rate; contrary to ILC, duty cycle $\approx$ 100%. One can make per channel calibration in one week of running, 250 muons per channel. Channel statistics is iniform within $\pm 4\sigma$ except for 1.1% of channels. 14.5% are noisy and masked, out of which 9.4% connected to 2 or 4 cells, will be 0% in FEV9. Threshold $\sim 0.5 \times$MIP = 35 ADC (1.2 pF gain).



Cosmic calibration, 4 chips X 5 slabs

In %	spread	stat. error	above stat.	physical prototype
All	6.1	∼5.1	∼3.3	∼5
Within chip	5.5	∼5.1	∼2.1	
Between chips	2.9	∼0.7	∼2.8	

Further details in my report at ECAL ILD meeting in June in Paris
https://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=6036



Topic

Jul'13 beam test

- Improvements
  - Many thanks to Franck Gastaldi (LLR), GDCC is in operation instead of LDA. Two GDCC were used in the test beam (and no LDA). Two LDA firmware bugs discovered, rate of lost packets reduced to $\leq 10^{-3}$ (a few % in LDA).

    Difficulties with LDAs:
    - no possibility to maintain firmware (Xilinx licence is needed for Ethernet interface, current version is obsolete; understanidng of packet management requires reverse engineering)
    - not sufficiently reliable (grounding, shielding, connections)
  - decoupling capacitors in all slabs to reduce retriggerings, PCB bug fixed in one board
  - all slabs can be power pulsed, capacitors and new DIF firmware
  - minor improvements in DAQ software
- Problems
  - Retriggerings are reduced but still exist
  - Configuration often fails, may require many iterations. 0.5 slabs out of 7 were excluded, trigger threshold scans with lots of reconfigs impossible after CAEN failure and associated power cut
  - No beam during 1 + 1.5 days (out of 6 planned, DESY problems)
  - Production of 2 new slabs started before TB (in LLR, LPNHE, LAL). At the very last step of assembly in LAL in connecting HV Kapton cable to silicon wafer too much glue was deposited which caused a short circuit. Both slabs became not operational. One recoverable.

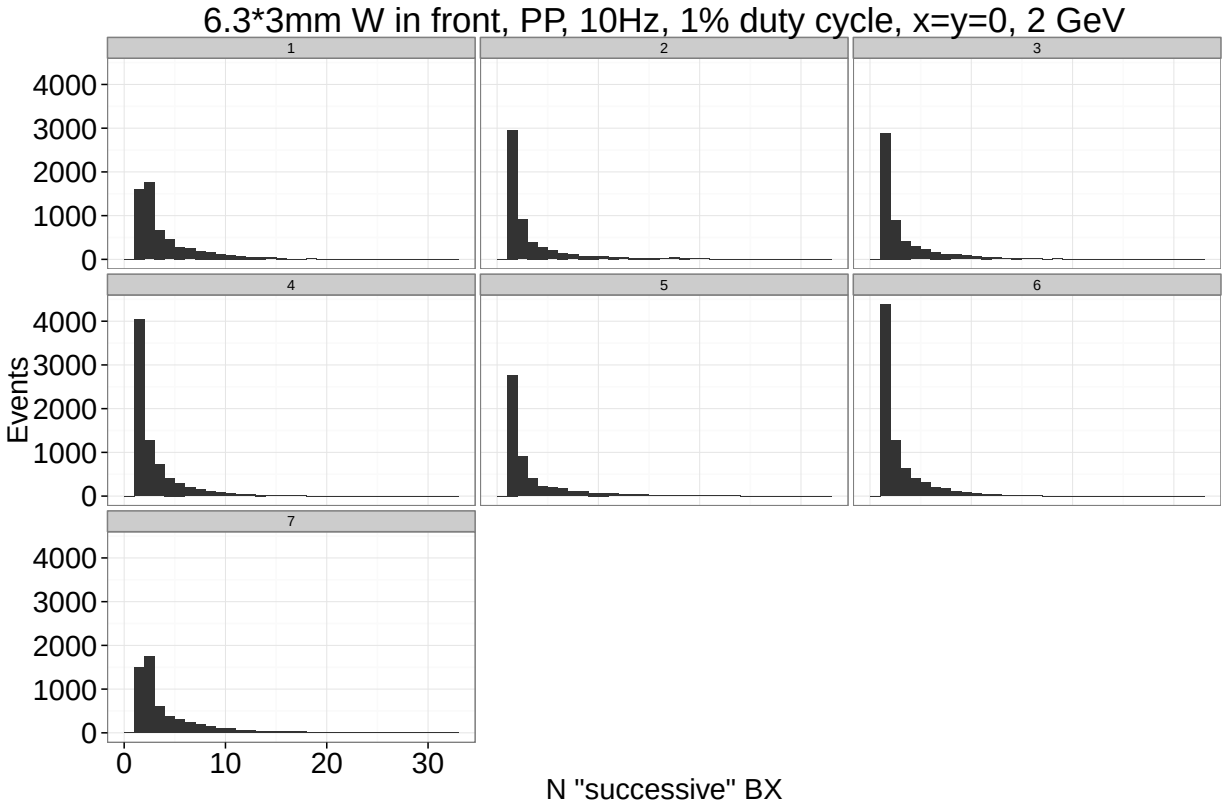
Jul'13 beam test

6-7 slabs, power pulsed / continuous modes

MIP position scan, 1-5 GeV energy scan with $6X_0$ W,

$5.4X_0$ in front + 0 / $7.2X_0$ at 2 GeV, Si+Sc run, GDCC spill frequency scan.

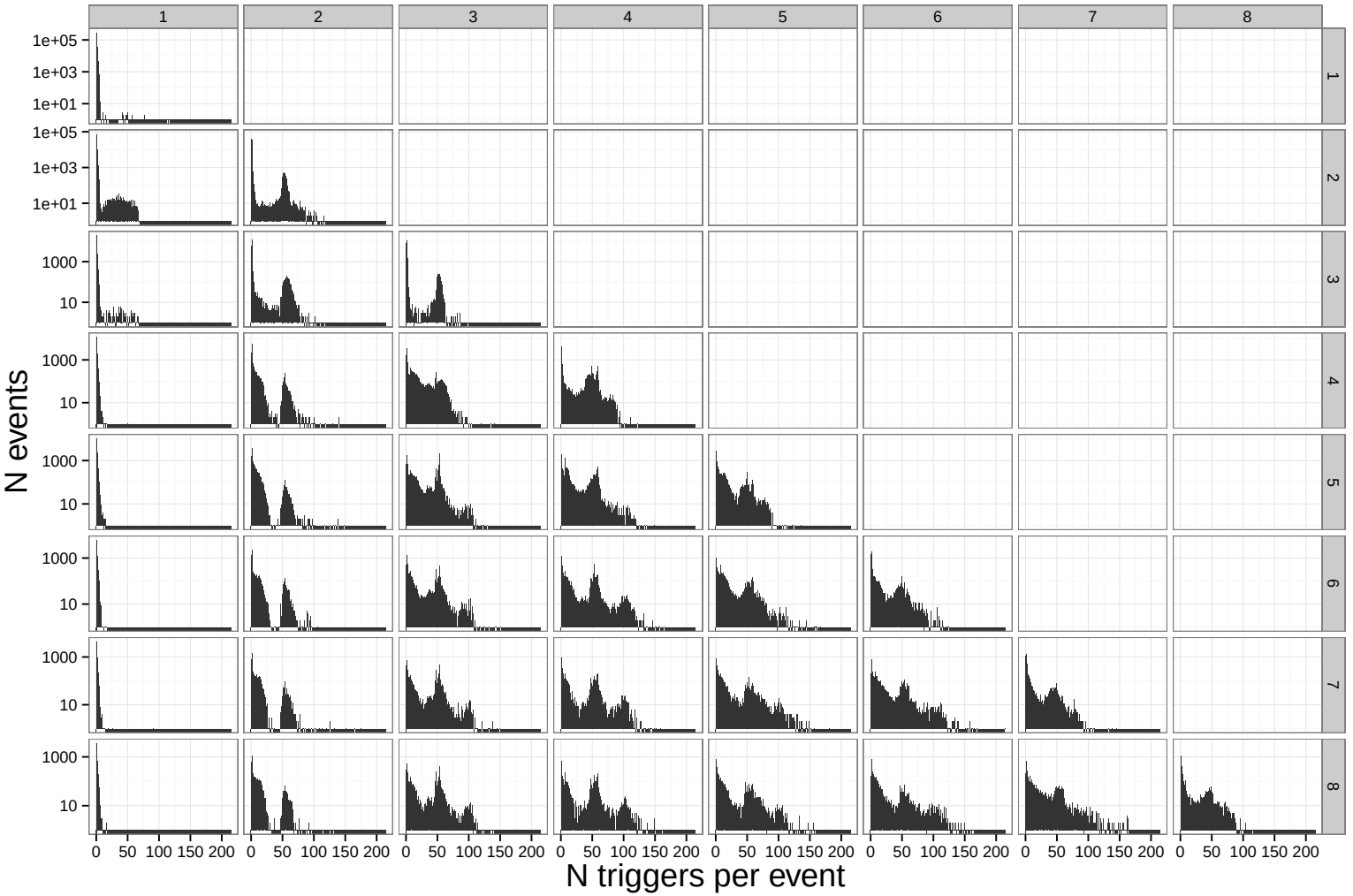
Thresholds significantly lower than in Feb'13. 13.7% of masked channels (out of which 9.4% connected to 2 or 4 cells, will be 0% in next PCB FEV9).



N events with "successive" (differing by at most 4) bunch crossing numbers. In the past: often peaked at N = 15 overfilling SKIROC memory. Retriggers still exist, though stop earlier and thresholds are lower. Note, significant fraction here comes from random coincidences (see later).

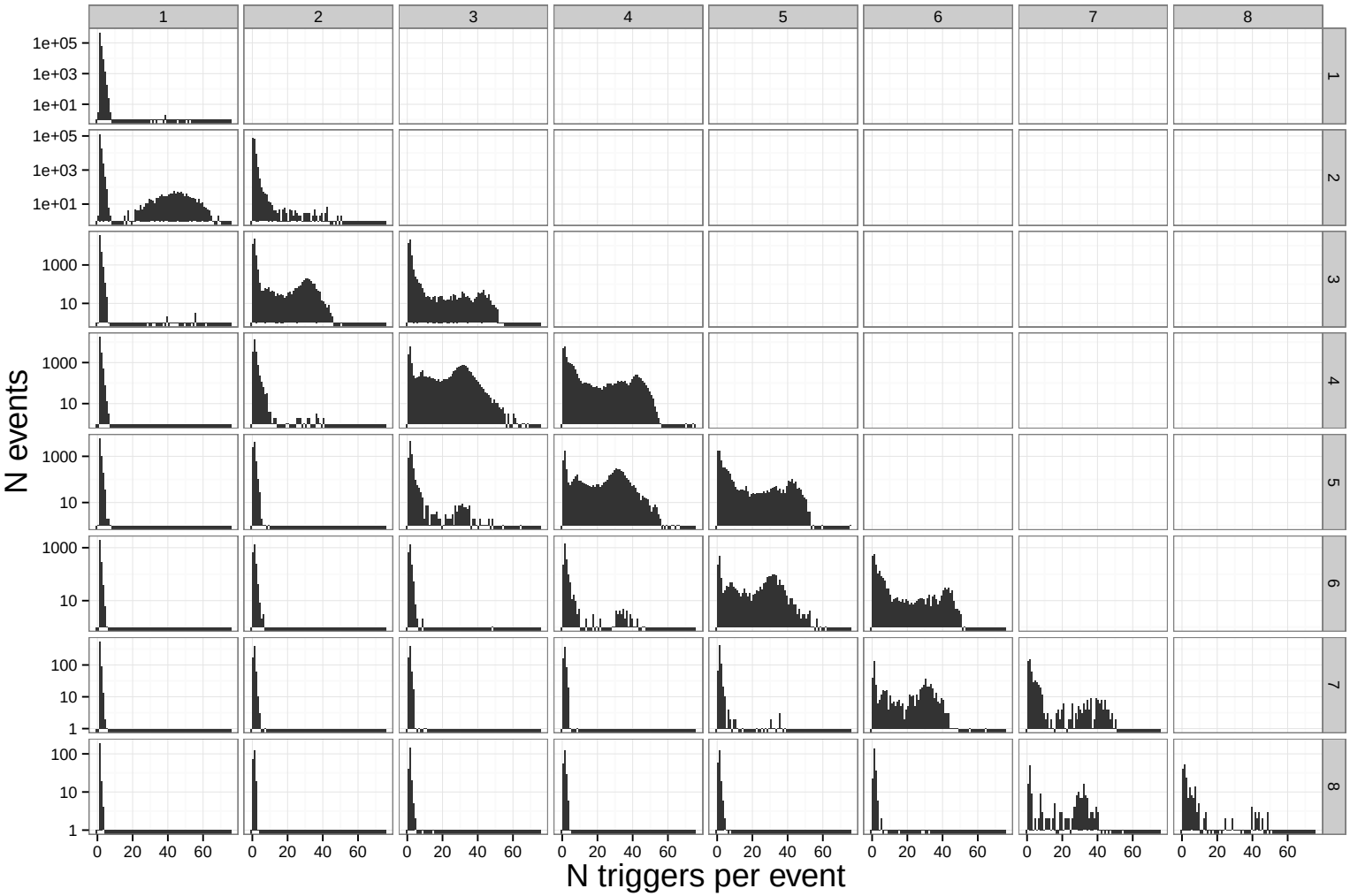
Hit multiplicity, plane events, PP mode

Number of fired channels in the slab as a triangular matrix: number of "successive" events N versus sequential number in group 1. . . N.
"Plane" events with $\sim$ 50 triggered channels can appear even in first retrigger BX+1.



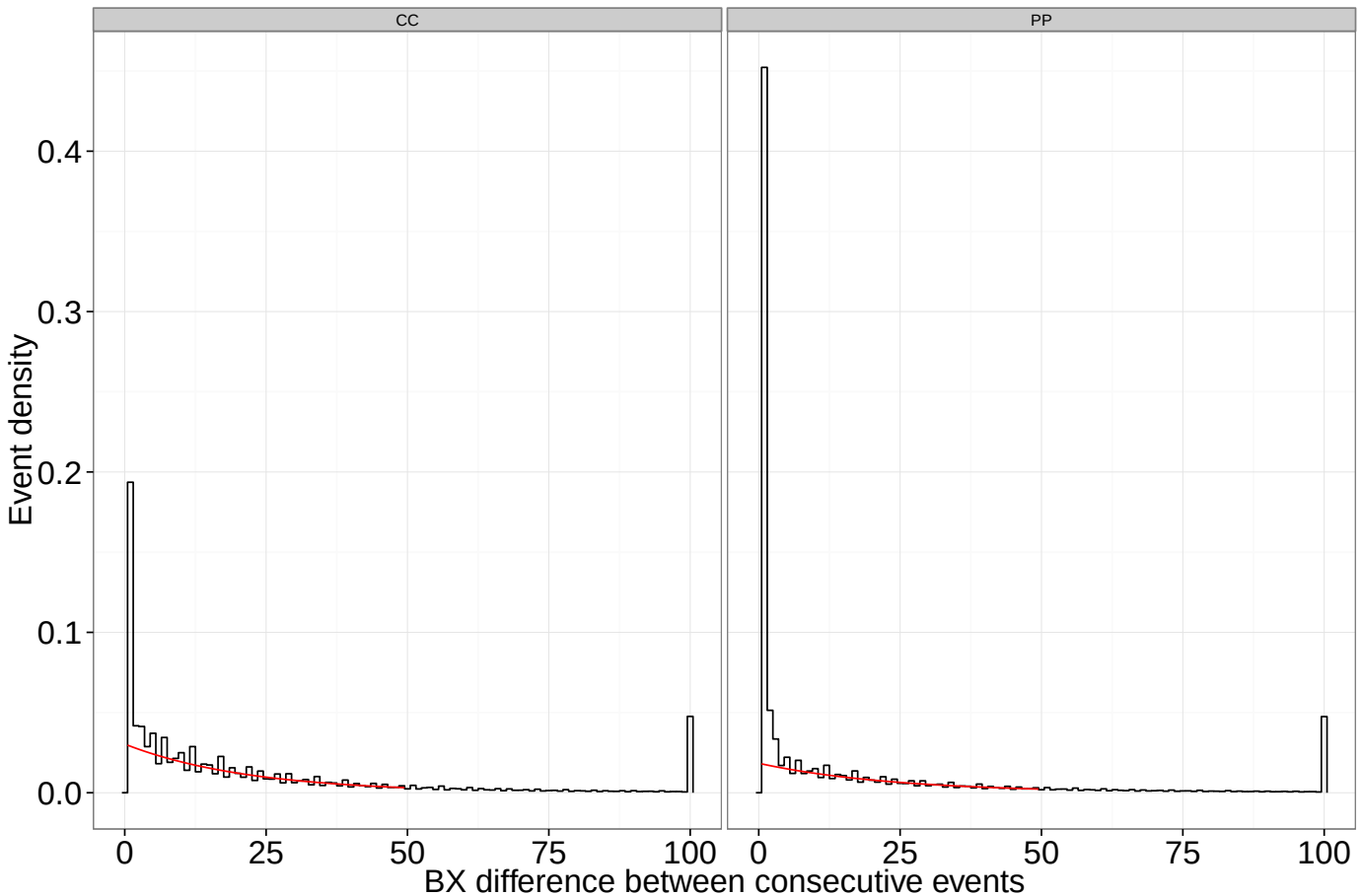
Hit multiplicity, CC mode

In continuous mode retriggers fire plane events only before very end. Note, off-diagonal histograms contain random coincidences, but not only, there is a fraction of retriggers, so retrigger != plane event, see next slide.

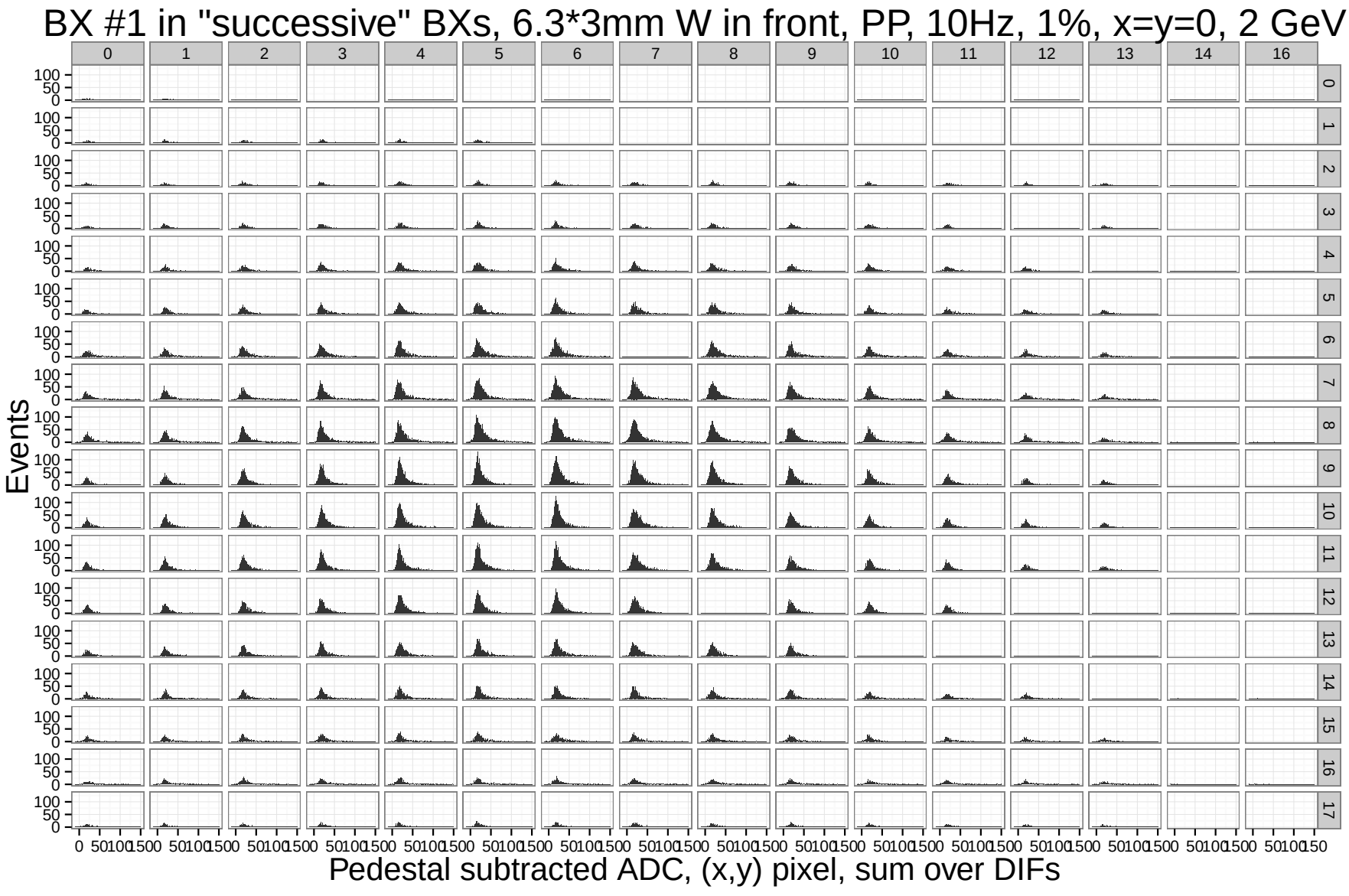


Fraction of retriggered events

Time to next event for slab 9, CC and PP modes (runs 4, 5). It should be exponentially distributed. Peak in beginning is due to retriggers. Fraction above exponential fit, CC: 0.23, PP: 0.51. Curve is not smooth probably because of bunch structure of the beam (it is not exactly continuous).
Peak at zero remains even when events with only one hit are selected. Therefore retrigger != plane event, retrigger may contain only one hit.



Retriggres removed, sum over slabs (same masking)



Next step: build full event out of independent slabs (never in the past).

Synchronization of slabs with different timing

DIF	Slab	Delay before BX counting	First BX with data
2,4,6	8,2,10	250 usec	49-50 usec, $\sim$ 125 BX
1,3,5,7	9,5,7,1	500 usec	98-100 usec, $\sim$ 250 BX

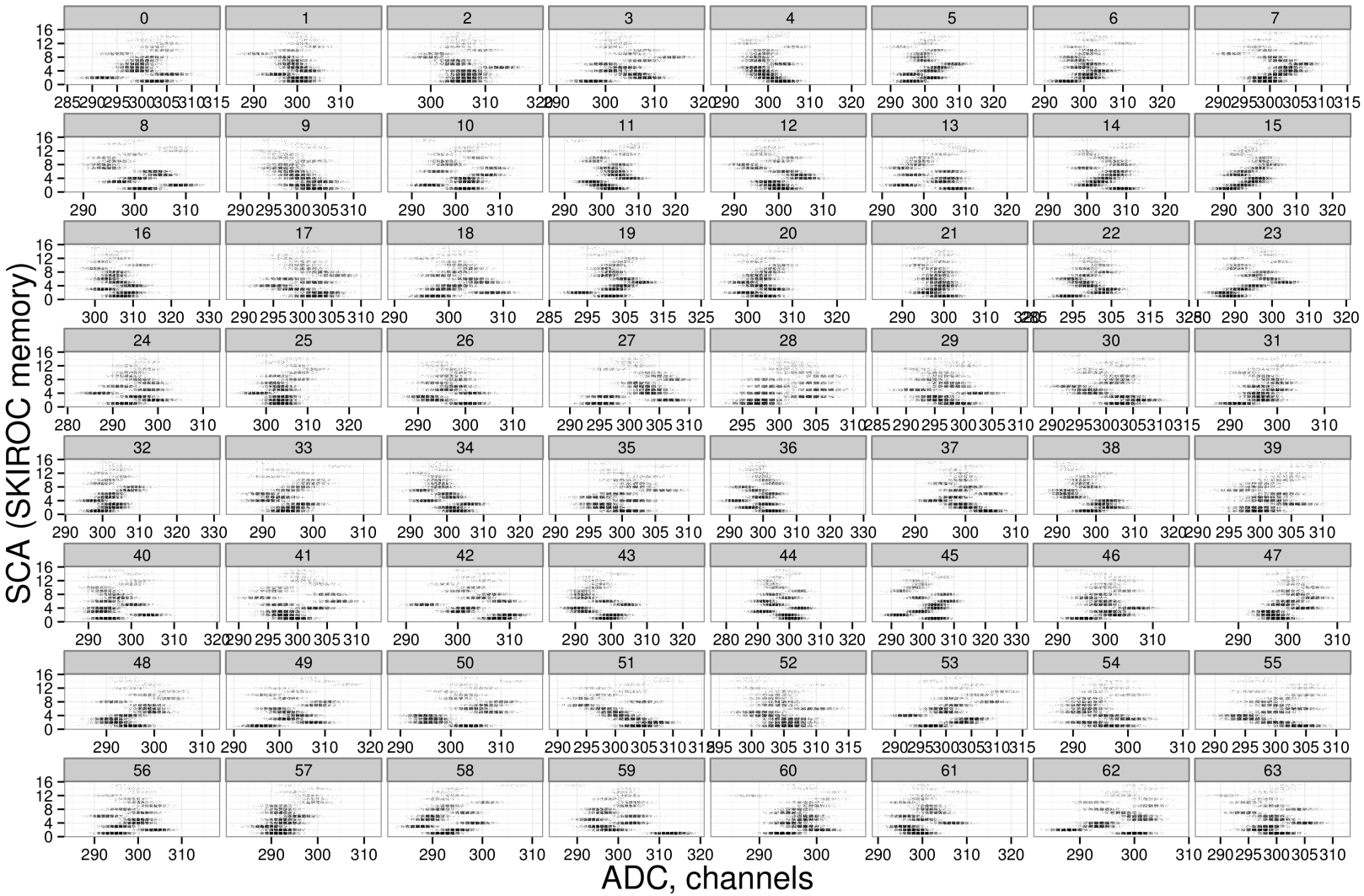
To align BX: **subtract 626** from BX in DIFs 2,4,6. Then, slabs are synchronized within Δ BX = -1,0,1. There is a small timing mismatch (may be constant) even after sending a common synchronization signal in the beginning of run.

When one SKIROC becomes full, data taking in other SKIROCs may either continue or may stop. This is determined by CCC rotating switch. In July beam test it was continued ("SPILL" mode). Therefore, "fast" slabs could sometimes stop before "slow" could take data, and there could be no coincidence.

Topic

Pedestal dependence on SCA

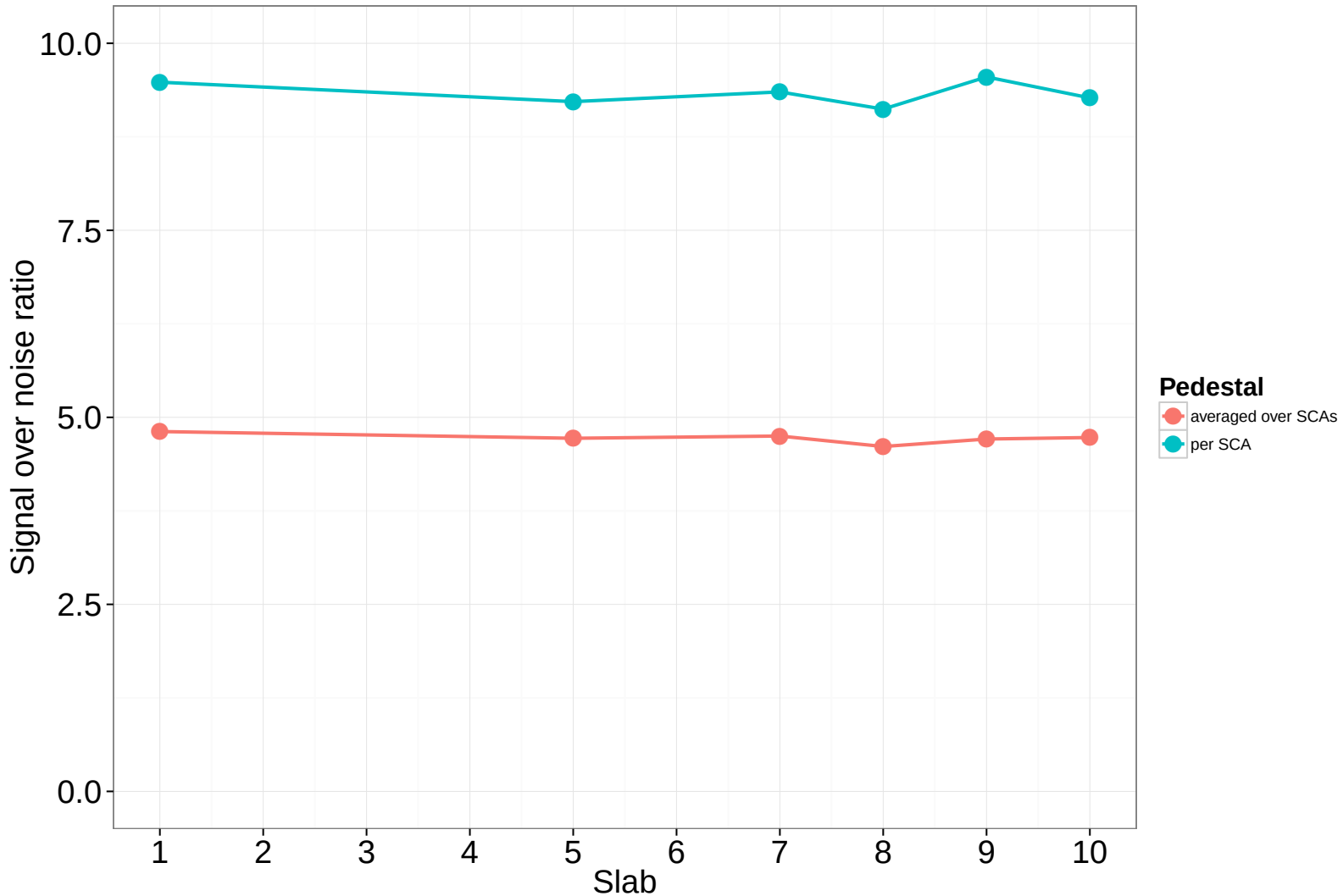
Pedestals versus SCA (SKIROC memory index, 1. . . 15) for 64 channels in 1st chip of slab 9, DIF 1. Jul'13 beam test, run 4, CC mode, not triggered channels, first BX out of group of consecutive BX's, lowest gain (6pF).



Signal/noise improvement, 6 pF, CC mode

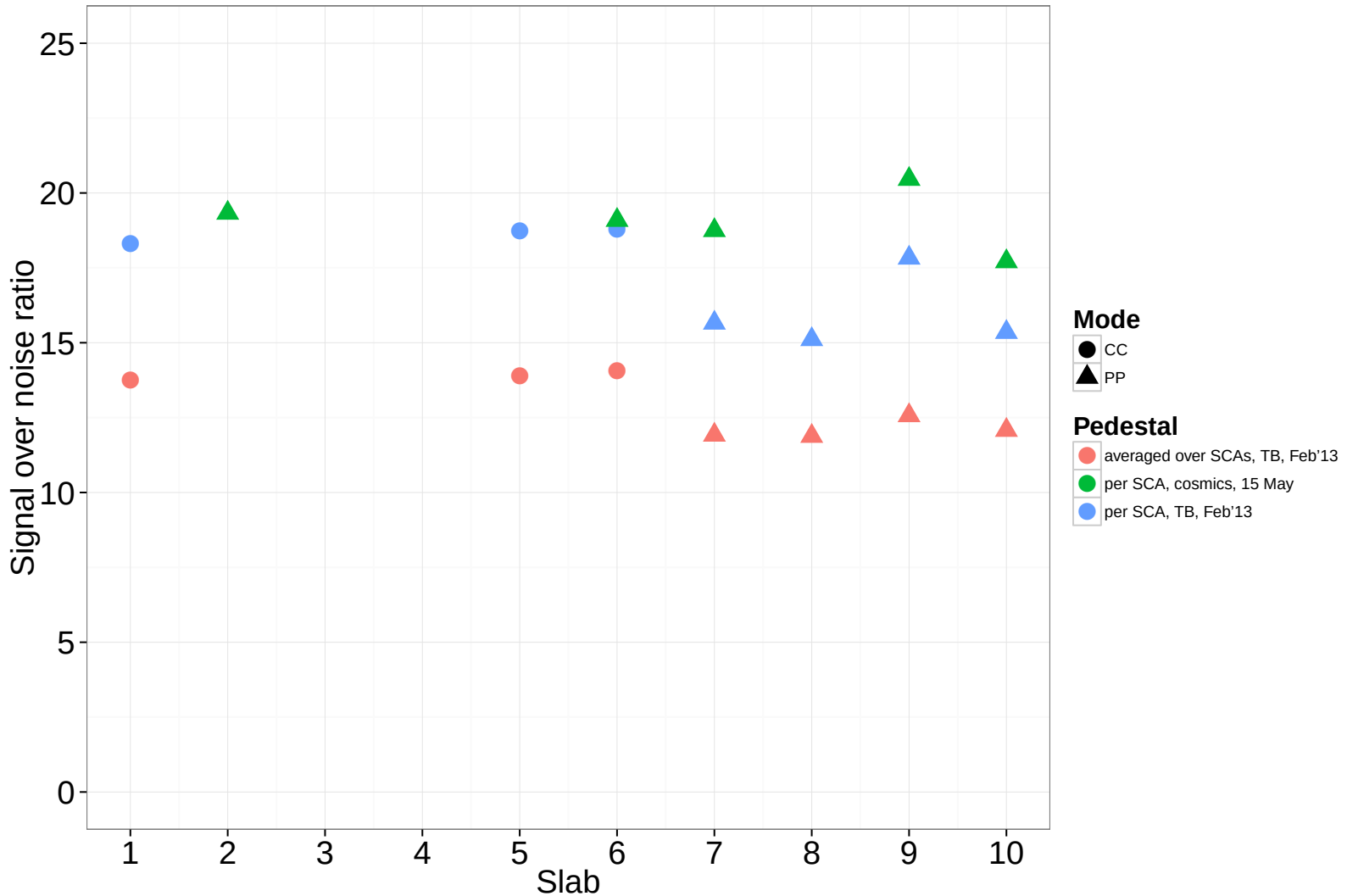
Continuous (not power pulsed) mode.

S/N when pedestals are calculated per SCA or averaged over SCAs.



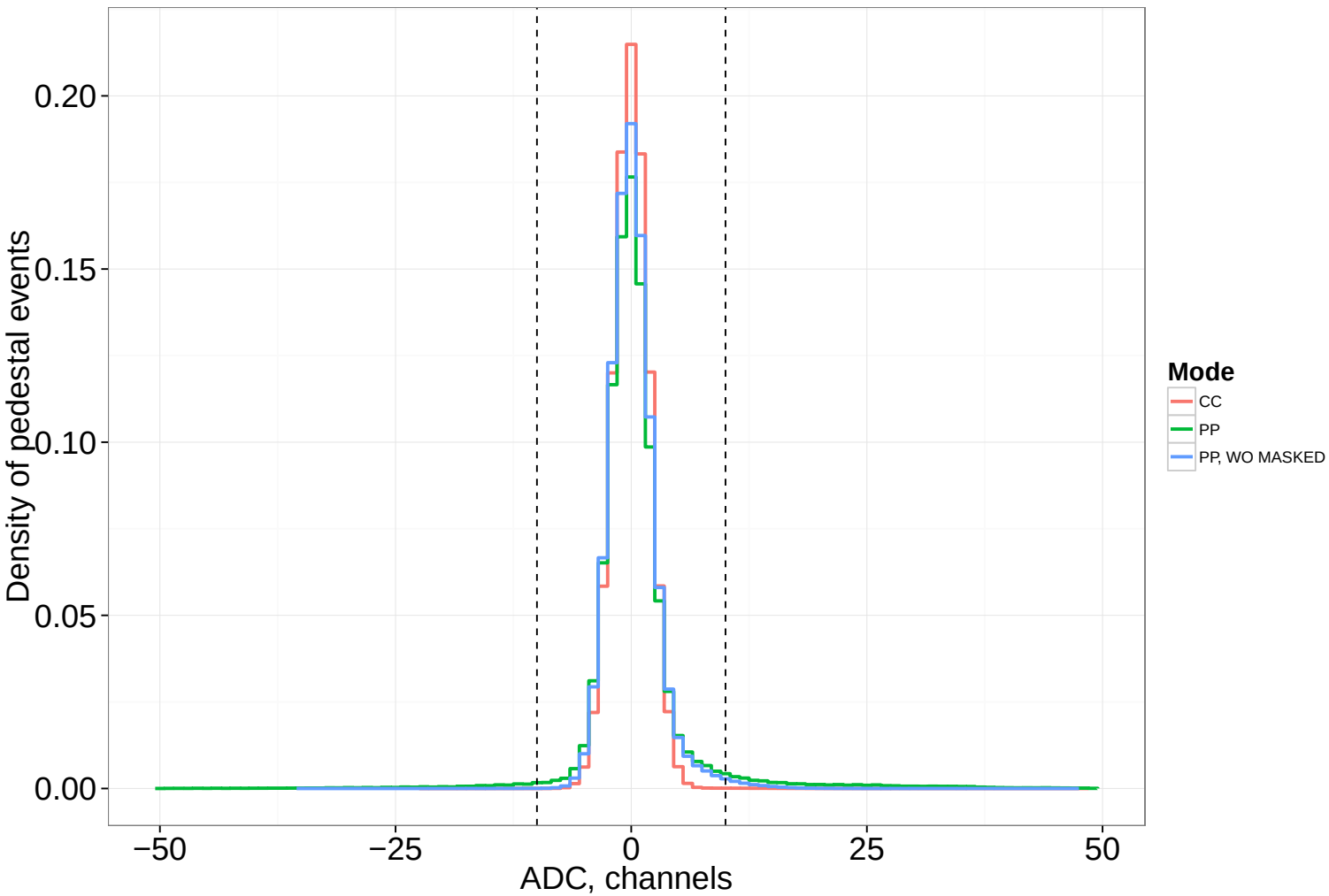
Signal/noise improvement, 1.2 pF

Same for 1.2 pF, Feb'13 beam test and cosmic run started on May 15. Power pulsing is worse than continuous mode, except for cosmic run with duty cycle $\sim$ 100%.



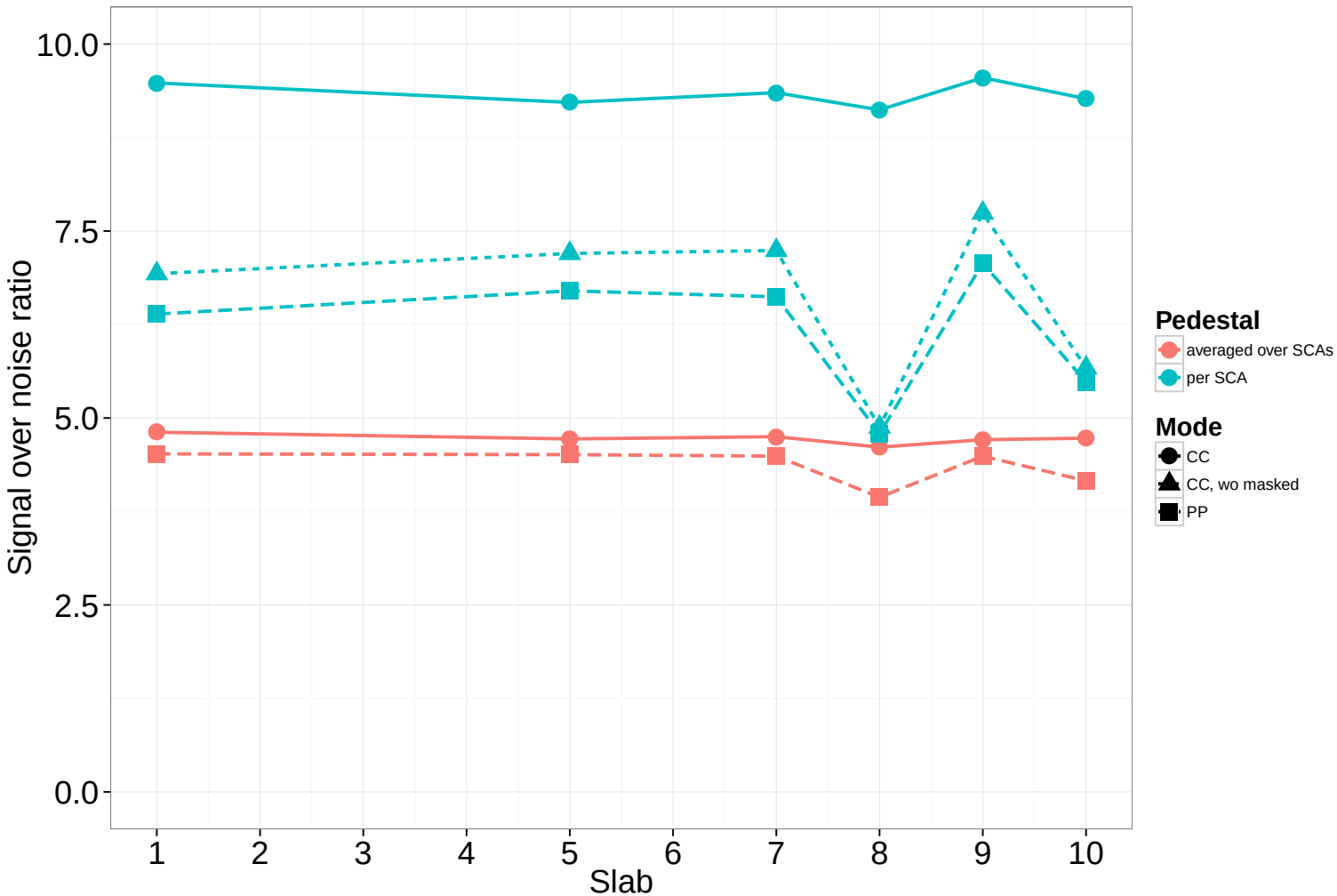
Pedestals for CC and PP modes

Jul'13 beam test, lowest gain (6 pF), runs 4 and 5.
Pedestal sum over all channels in DIF 1 (slab 9). PP mode has long tails, especially for masked (noisy) channels. Without masked channels (blue) tails become a little smaller.



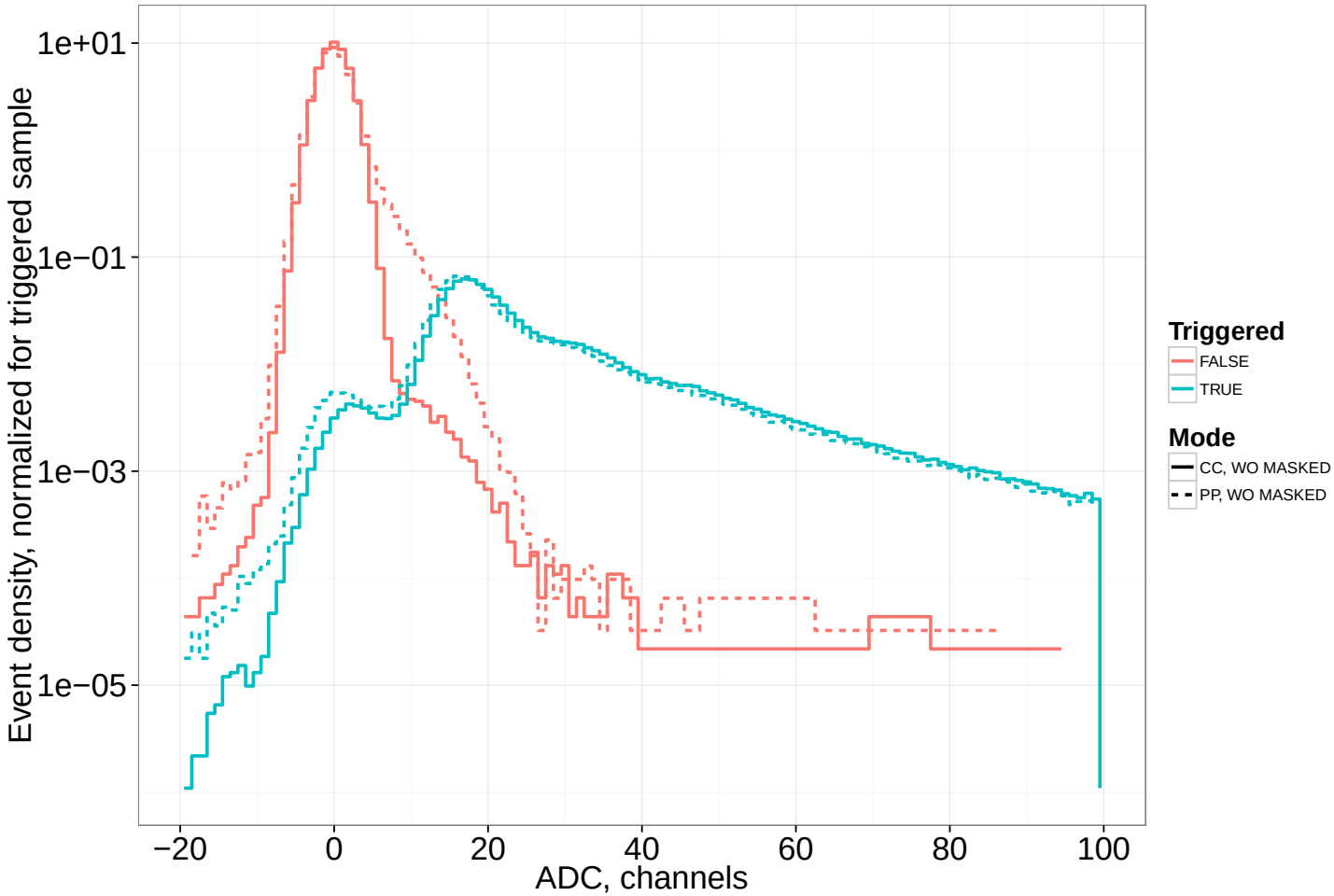
Deterioration in PP mode at 6 pF

Noise is estimated as RMS in [-10, 10] interval.
Jul'13 beam test, lowest gain (6 pF), runs 4 and 5.
Long pedestal tail in PP significantly degrades S/N. If masked channels are removed, S/N slightly improves (triangles).



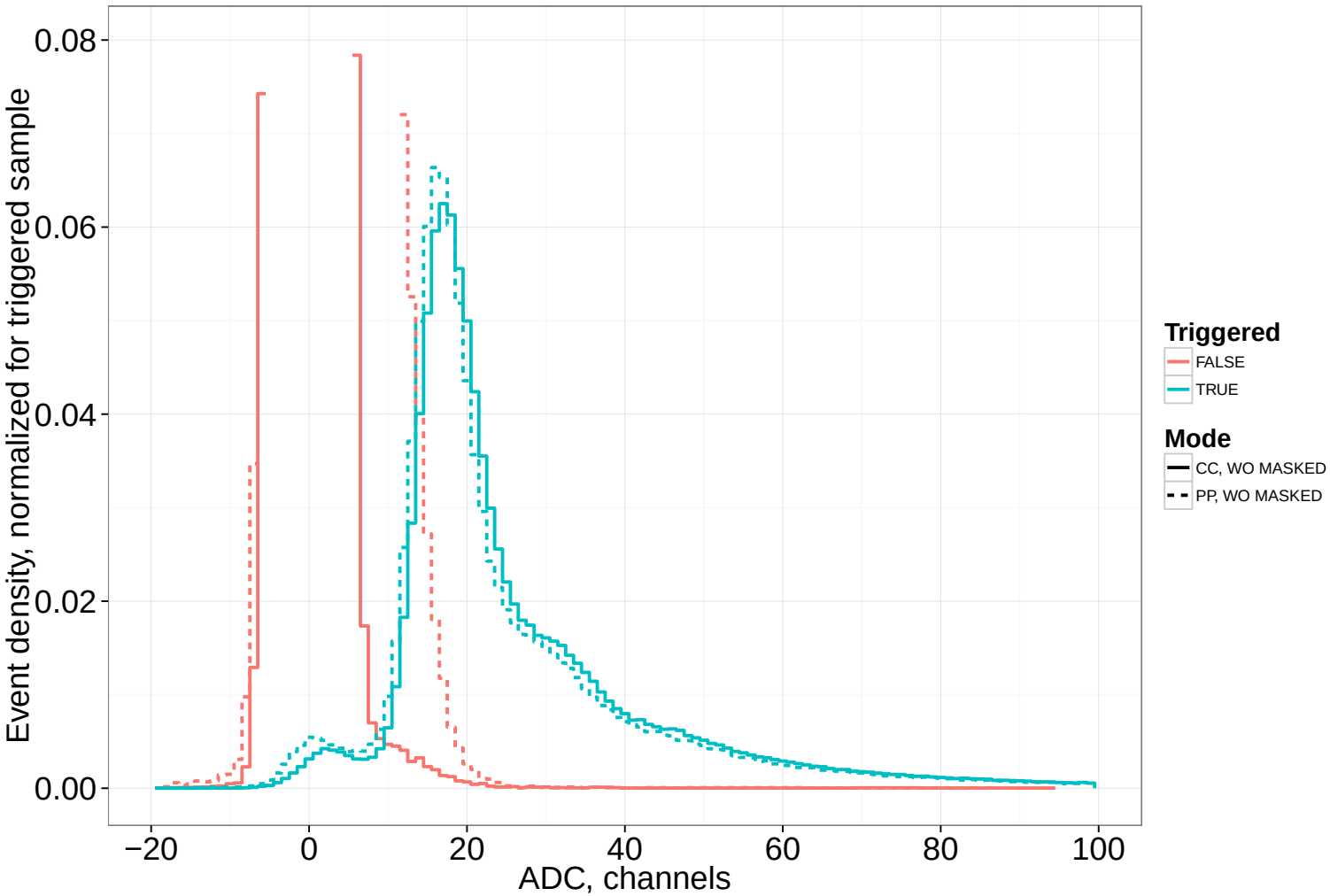
Triggered and not triggered events, 6 pF

Jul'13 beam test, no tungsten, runs 4 and 5. Sum over all not masked channels in DIF 1 (all chips, slab 9), first BX in group of consecutive BX's. Pedestals are calculated per SCA as median in not triggered sample, and subtracted. Note, due to wrong timing of not triggered MIPs (readout at random clock edge), they should be smeared and shifted to lower values. Note logarithmic scale.



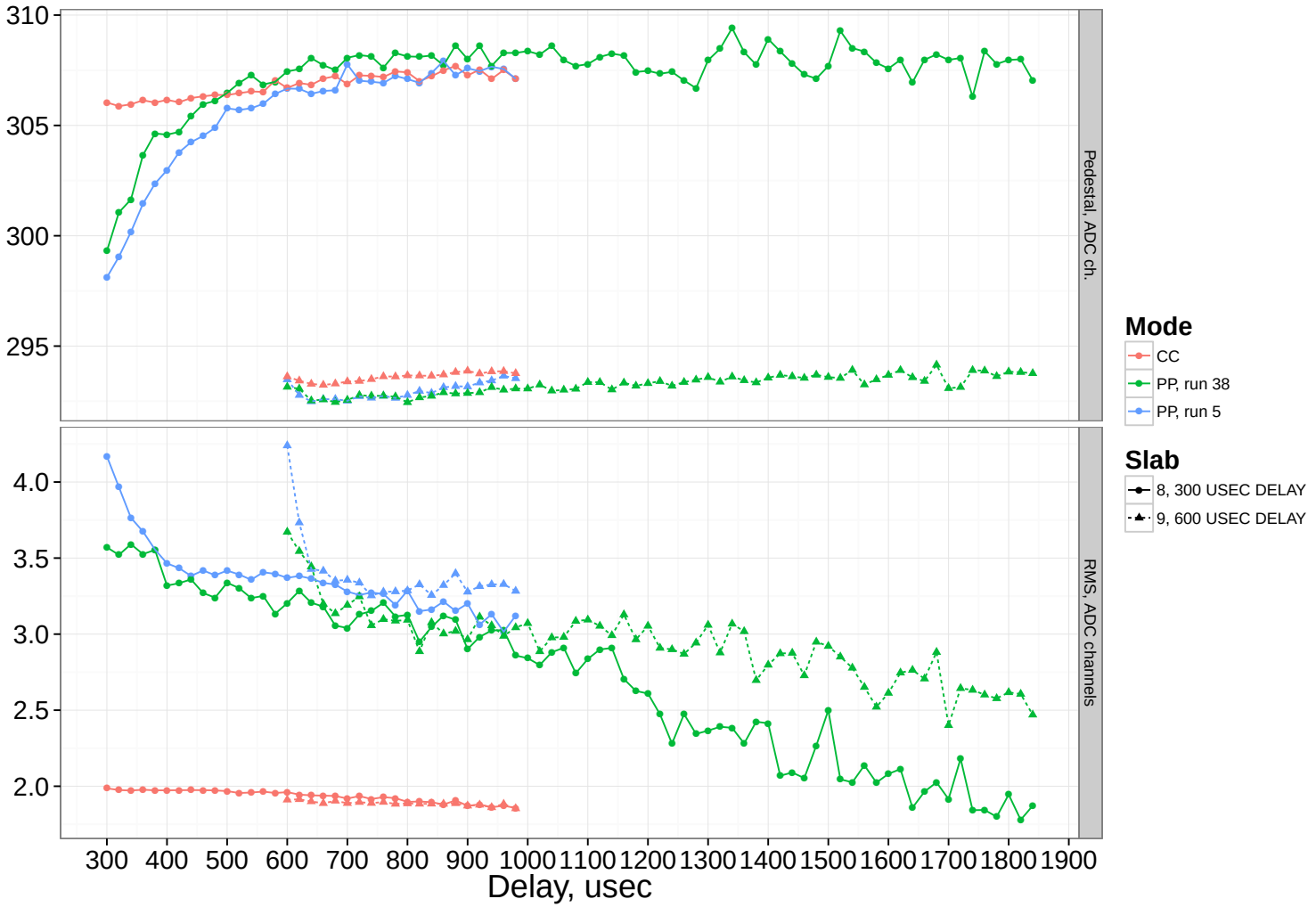
Same, linear scale

Note, one triggered hit causes readout of $\sim$ 50 not triggered channels in the same chip (64 - 1 - 13.7% of masked channels). Number of events in not triggered histogram is, therefore, $\sim$ 50 times larger.



Time evolution of pedestal width and RMS

Time evolution of pedestal position and pedestal width for slabs 8 and 9 with (250+50) and (500+100) μsec power pulsing delay. Average over not triggered sample, all channels in 4 chips; first BX in group of consecutive BX's. Run 4 (CC) and 5, 38 (PP). Run 38 has longer spill duration.



Conclusions on pedestals

- Pedestals depend on SCA!
- In PP mode pedestals have long non-Gaussian tails (esp. noisy channels), except in cosmic running with duty cycle $\sim$ 100%.
- Time evolution of pedestals
  - after spill start, center drifts during $\sim$ 500 usec;
  - RMS approaches CC value in > 2 ms. In cosmic run with duty cycle 95% it is the same as in continuous mode.

Conclusions on pedestals (cont.)

- S/N ratio

	6pF	1.2pF
CC	9.3	18.6
PP	6.6	16.0

(Contrary to SKIROC simulation?) it is much more advantageous to run with higher gain. Possible solutions for keeping dynamic range for high energy showers:

- run at 1.6 pF (MIP at 50), increase high gain / low gain ratio in SKIROC3 from 10 to 40. High gain is linear up to 2000 ADC channels (after pedestal subtraction), so low gain can be cross-calibrated in a range up to 2000/40 = 50.
  Dynamic range $\leq$ 1500 MIPs (improved by 7%).
- Or add third gain in SKIROC3, keep 1:10 ratio between the three.
- Or make precisely controllable non-linear response of SKIROC ("saturation") to increase dynamic range. One-point MIP calibration may be not enough for saturation curve.

Topic

PHIL accelerator in LAL

1-3 MeV e^-, minimal measurable bunch intensity 10^8, very short duration.

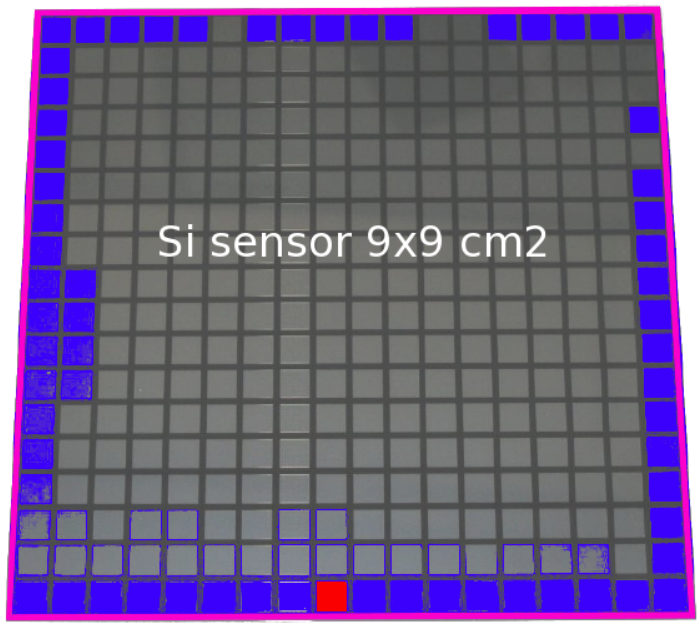
$\sim 100x100\ \mu m^2$ collimators (eg. 5-10 mm of steel) can reduce intensity from 10^8 to $\sim$ 2500 MIPs.

Can mimic high energy showers. Suitable for Si guard ring cross talk study ("square events"). This request was presented on Jun 18 meeting in LAL with Hugues Monard (responsible for PHIL).

So, we'll need

- collimators
- motorized table

PHIL availability: uncertain, next year.



Topic

Status and plans

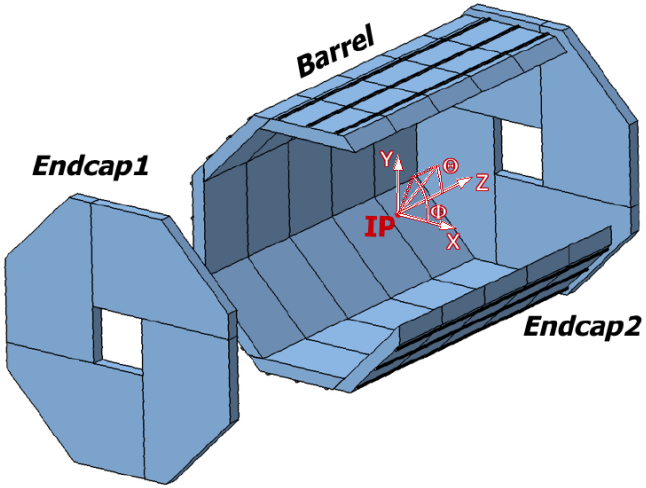
- GDCC works fine, lost packet rate $\leq 10^{-3}$
- FEV9 design should be finished soon
- BGA packaging for SKIROCs is ordered
- New slab with spring Si contacts instead of glue
- Plan: test next year at CERN full scale mechanical prototype equipped with long slab and short slabs in all alveolars.

Status and plans (cont.)

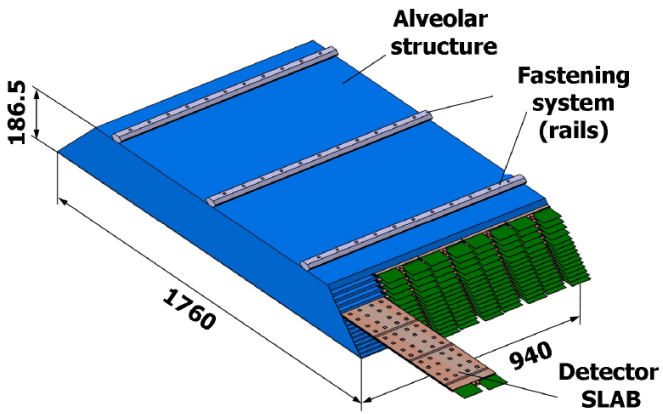
- Slab assembly should be improved, toolings, quality control
- Next bottleneck: problems in configuration
- Spill number bug
- Signals in masked channels
- Cosmic and Jul'13 beam test data are available
- S/N degrades in power pulsed mode. Can be improved by increasing gain (eg. with high gain / low gain ratio = 40).
- Pedestals depend on SCA.
- SKIROC3 should be able to get pedestals eg. with random trigger. Probably, one needs charge injection line on PCB.

Topic

Possible changes



For 30 layers: $\sim$2600 m^2 Si, $\sim 10^8$ channels, $\sim$130 t W

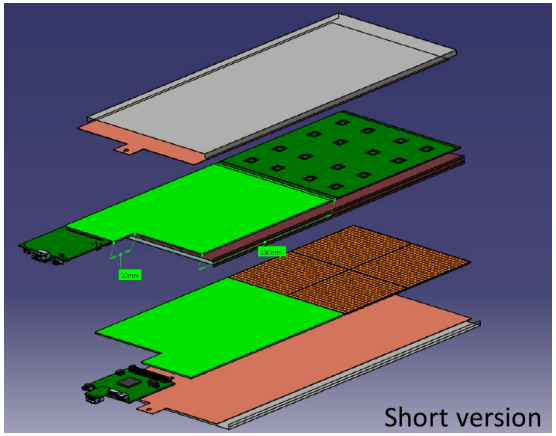


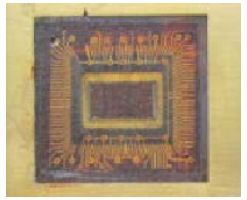
- R = 1.8 m - can be reduced? Compensation by higher B field and granularity in HCAL (RPC, micromegas) and ECAL? Big impact on full ILD cost.
- Endcaps will also contain endcap "rings" close to beam pipe. No detailed design yet, high e^+e^- backgrounds from beam-strahlung ($\lesssim$ 170 hits/chip/spill)
- 30 layers $\rightarrow$ 20?
- ECAL thickness:
  $\rightarrow$ 19 cm for naked die chips inside 1.2 mm PCB (difficult),
  $\rightarrow$ $\sim$23 cm for BGA packaging. For 20 layers: $\sim$19 cm.
  Cu 0.5 mm thermal drain in barrel: can be thinner (slab end: ΔT=2.2°C)?

Thickness of PCB + embedded electronics

Two options:

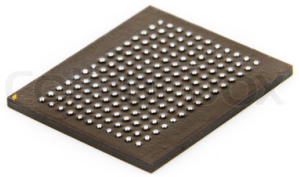
- "extreme" design (difficult):
  - naked die chips in PCB hollows, bonding connection
  - PCB with 8 layers, 1% flatness
  - only 1 mm thick (slab 7 mm)

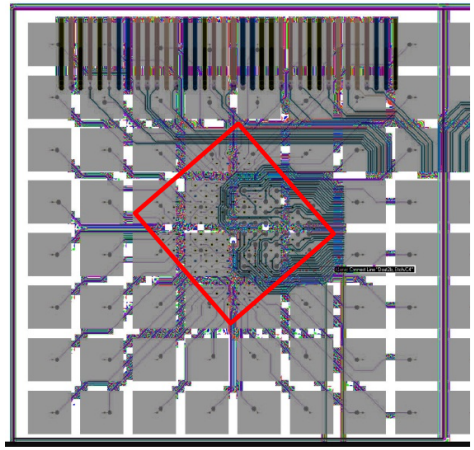




- conservative design (currently preferred, next step in R&D):
  - BGA chip packaging
  - 2.5 mm thick (slab 10 mm)

$\rightarrow$ 2-3 times less length of chip-cell traces w.r.t. current prototype

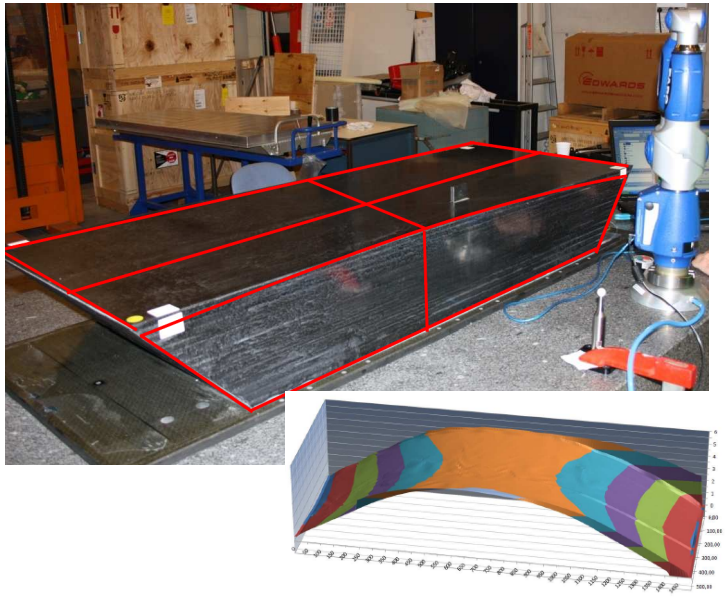




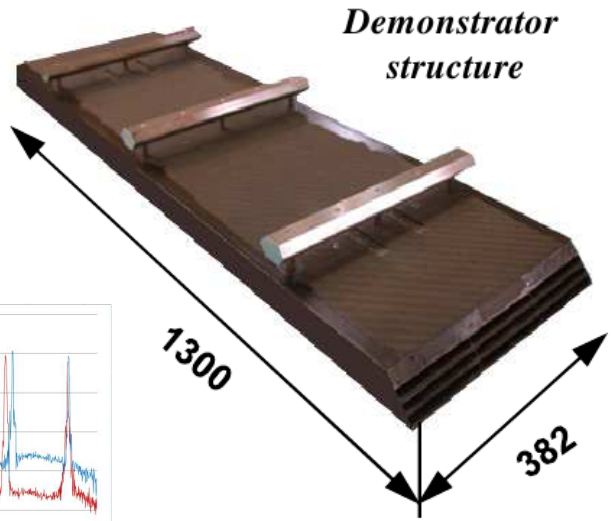
Mechanical structures

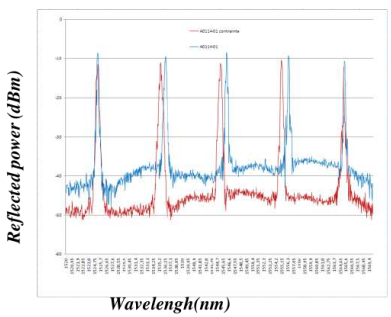
Prototype: 3/5 of one module, $\sim$ 600 kg.
Separately built layers "cooked" together.
Simulated mechanically & thermally.

	Exp.,mm	Measured
Height	552.78	552.65 ± 0.05
Width	205.3	$205^{+5.28}_{-0}$



Another prototype: 60 kg alveolar structure with 3 slots with molded Bragg grating fibers.
Plan: precisely measure deformations under stress by measuring frequency shift of light reflected by fiber.



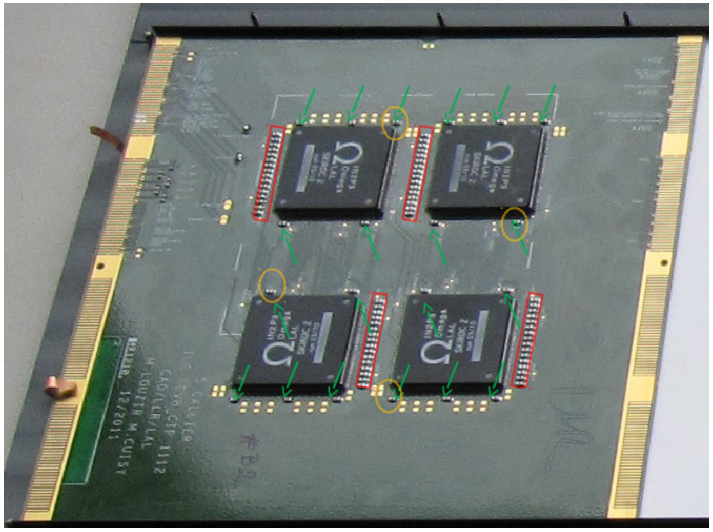


Improvements in technological prototype

Retriggerings and plane events are clearly caused by noise in SKIROC power lines. About 1/10 of analog power noise is propagated to SKIROC input.

Two improvements:

- decoupling capacitors (of two types to cover large range of frequencies) - all 8 slabs in LLR modified, big improvement
  (capacitors on photo: orange - add, green - change, red - remove for power pulsing)



- bug discovered: one analog power line was connected to digital
  $\rightarrow$ fixed in one slab (SKIROC "pin clipping"), also helps

Two new slabs are in production. Both improvements will be implemented (plus resistors for individual adjustment of thresholds per channel).

Long term: Jean-Baptiste Cizel (following Remi's advice) studies a modification for SKIROC3 to suppress sensitivity to power noise by 10.

Calibration and quality control for mass production

Si signal depends only on depletion region thickness $\rightarrow$ no dependence on external factors like temperature has been observed in physical prototype. Robustness and stability over years at % level (variations due to cable length change etc.)

Calibration spread $\sim$ 5%.

Mass production: possibly, one calibration only. Muon beam and cosmics. More steps for sensor / front end electronics validation to detect failures early, before final assembly.

ASIC front end chip linearity range: 1...1500 MIPs. A few % non-linearity at lower end due to shaper timing dependence on signal amplitude. Can be calibrated with electrical charge injection.

DAQ electronics: GigaDCC

Link Data Agregator (LDA):

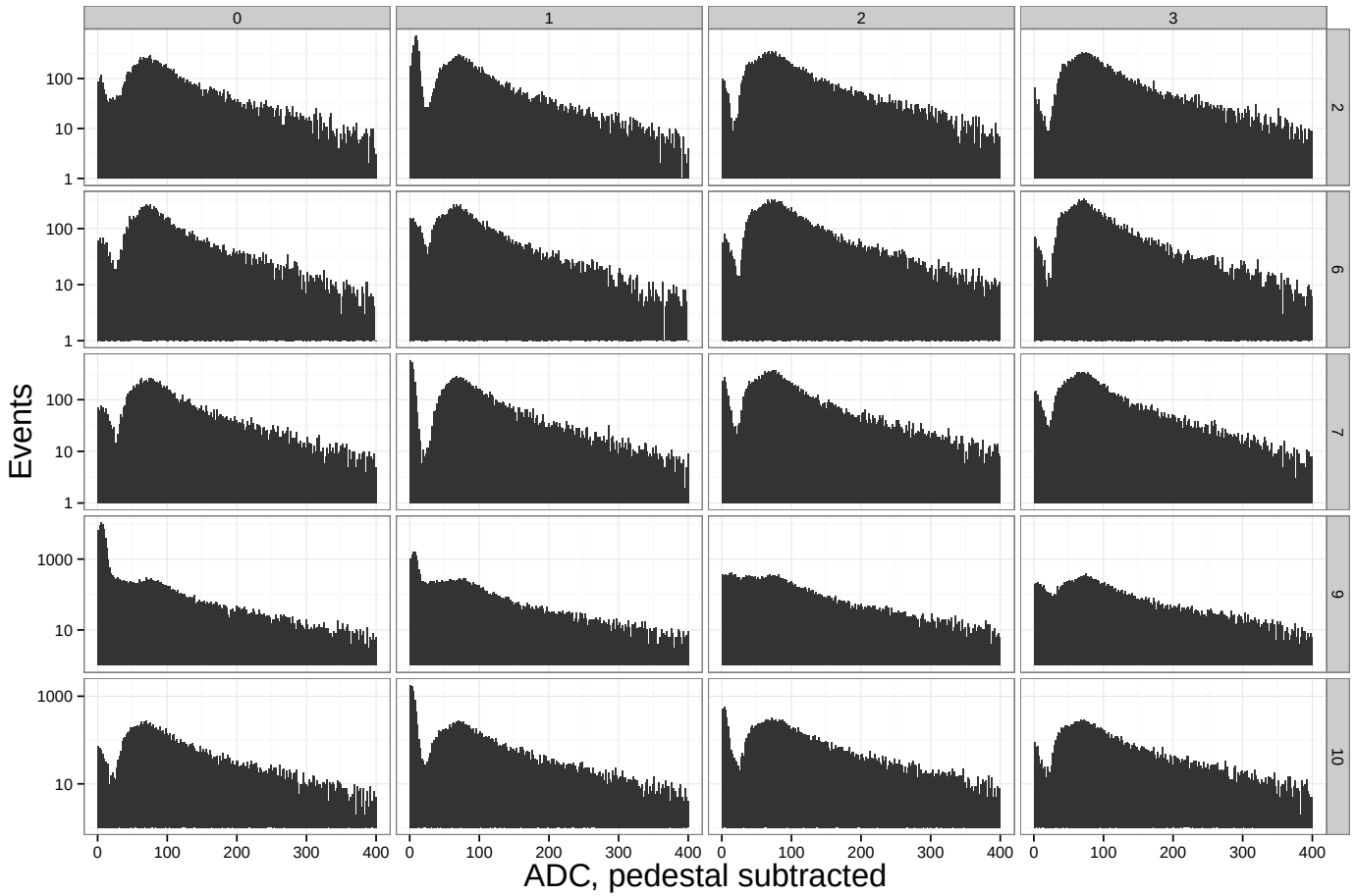
- difficult to maintain firmware (Xilinx licence is needed for Ethernet interface, current version is obsolete; understanidng of packet management requires reverse engineering)
- not sufficiently reliable (grounding, shielding, connections)

Gigabit Data Concentrator Card (GDCC) will replace LDA. Same software, reuse of some hardware parts.

Cosmic runs in May in LLR

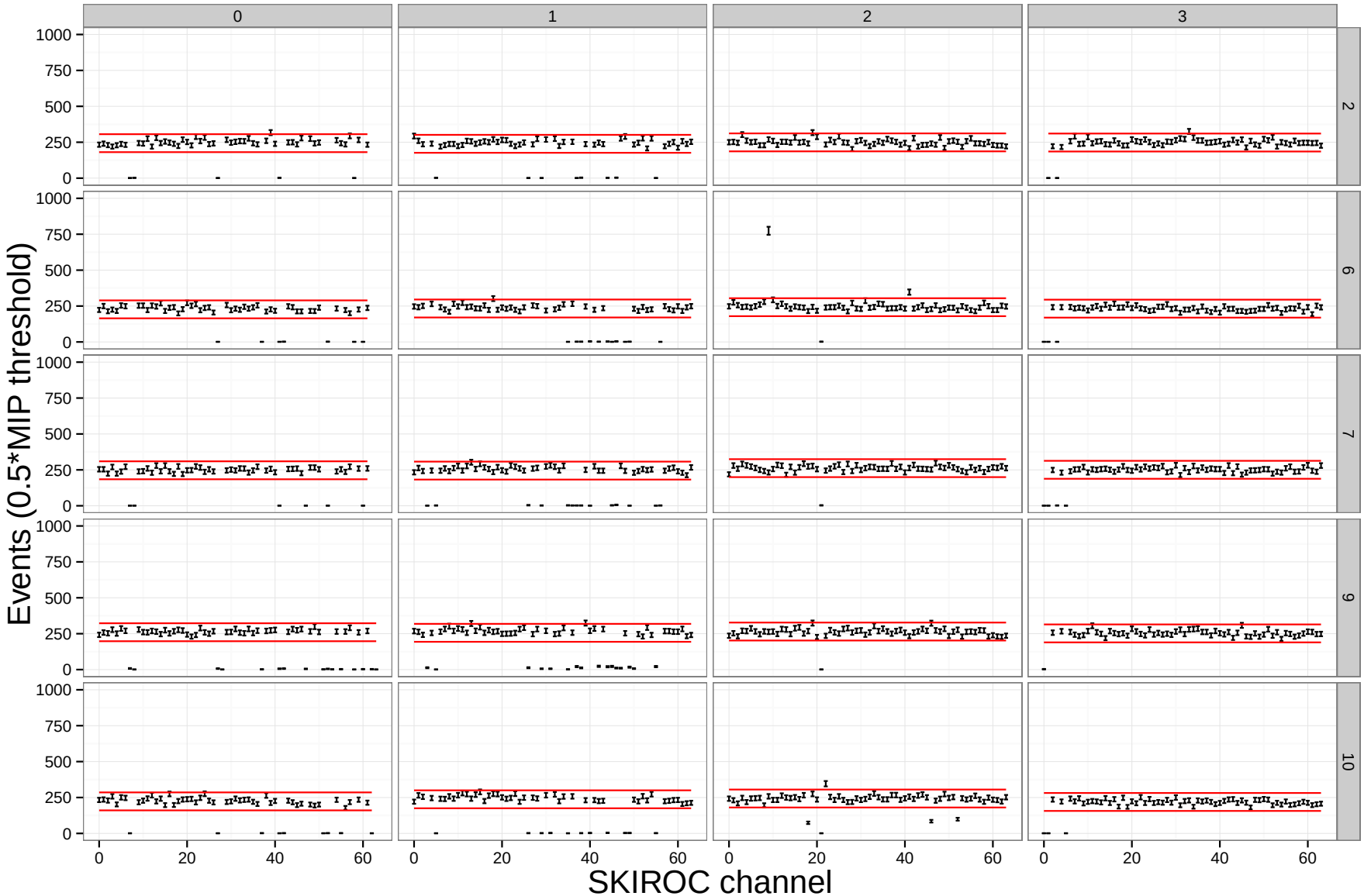
Sum over channels for 4 chips X 5 slabs. Threshold $\sim 0.5 \times$MIP = 35 ADC (1.2 pF gain). Low rate; contrary to ILC, duty cycle $\approx$ 100%.

4 slabs with decoupling C and one without (#9) but with corrected PCB bug (worse).



Channels connected to 2 or 4 cells are masked plus $\sim$5% of channels, probably picking up digital signals. Without decoupling C no good cosmic signals: power line noise fills up SKIROC memory before first muon arrives.

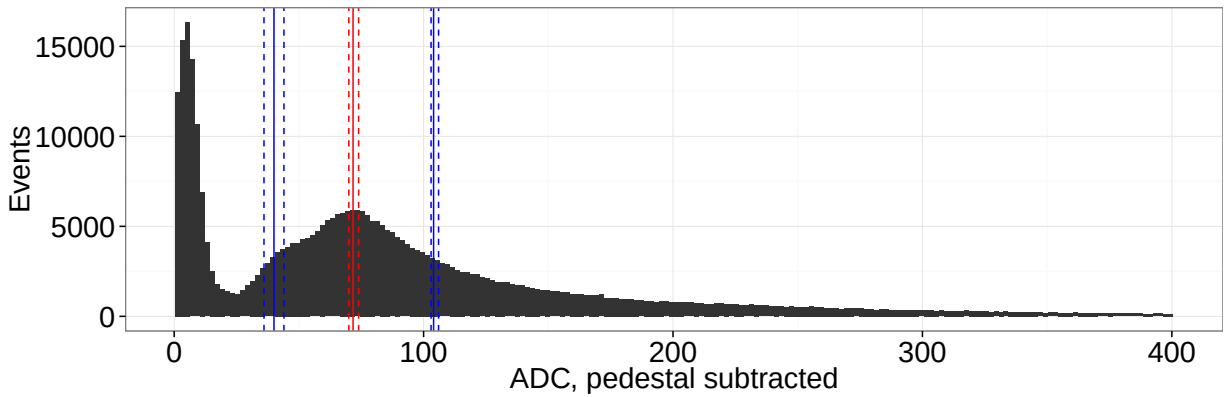
About 250 muons per cell above 0.5×MIP



Exclude channels with number of events N outside $\pm 4\sqrt{<N>}$ band

Muons, most probable signal

For simplicity, take truncated mean over 55% of lower data in ADC>40 range (red line = mean over band within blue lines). Fit to Landau distribution convolved with resolution is more precise, but sometimes may fail to converge (with >1000 channels). Also note effect of "S-curve" trigger efficiency at the left tail.

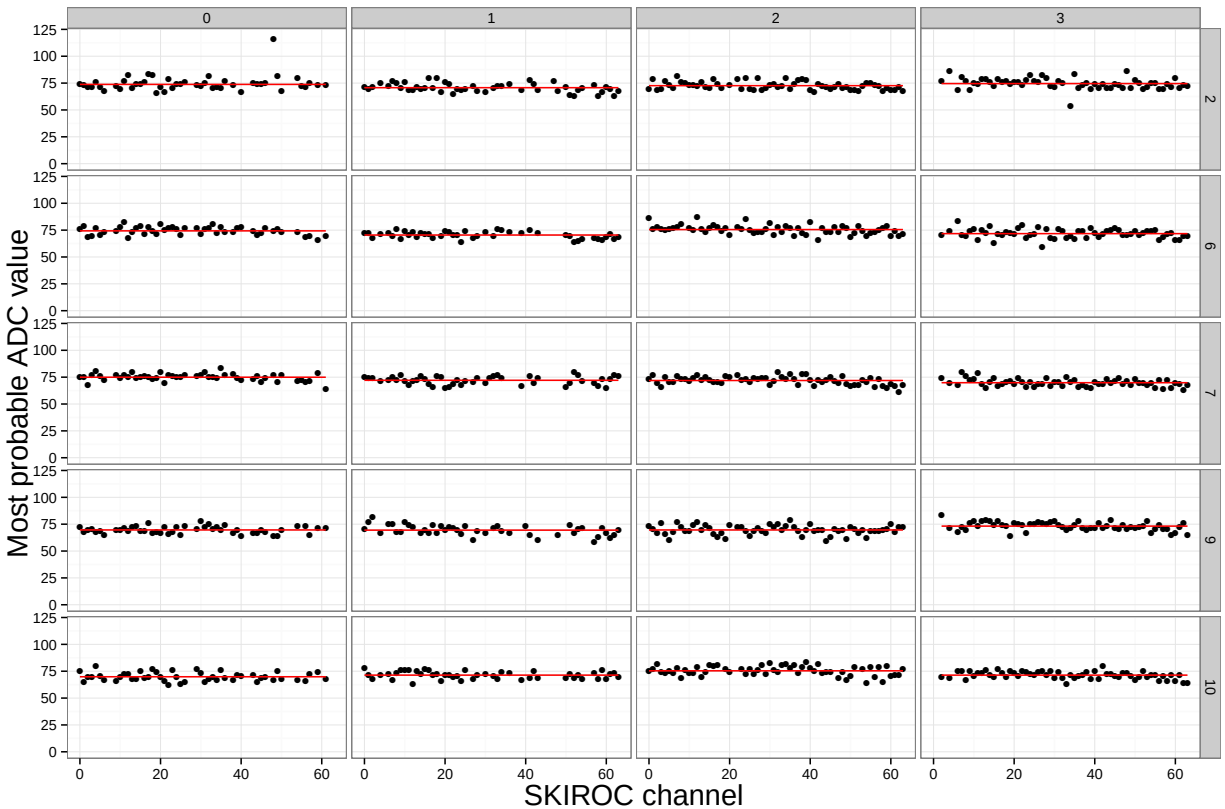


55% truncation is chosen to get the most probable value (MPV) at the right position.
Ideally, the lower threshold ADC>40 should cut a fixed fraction of the lower signal, then truncated mean = MPV. If position is fixed at 40, the fraction varies and there is a bias. ADC>40 cuts more for lower gain channels, effectively increasing truncated mean. The effect for 10% lower gain is equivalent to setting 10% higher threshold (right blue dashed lines on picture) for average gain. Truncated mean is then found to be shifted by 2.7%. Squeezing this picture by 10% lowers MPV by 10% (as assumed), sets threshold back to 40, but lowers truncated mean only by 7.3%. In the following, the bias of truncated mean is thus compensated by enhancing its variations by 1/0.73. The picture above is assumed to be one channel spectrum, ie. we neglected a smearing caused by summing up many channels with slightly different gains.
"S-curve" trigger efficiency is difficult to measure. If it is the same for all channels, for lower gains the left tail is more suppressed and the truncated mean is shifted to the right (again "compensation"). Our estimation of MPV spread is thus a little "optimistic".

Muons, most probable signal

In %	spread	stat. error	above stat.	physical prototype
All	6.1	∼5.1	∼3.3	∼5
Within chip	5.5	∼5.1	∼2.1	
Between chips	2.9	∼0.7	∼2.8	

Stat. error estimation: randomly assign slabs/chips/channels to events and repeat procedure. Not calibrated channels - 15.6% (1.1% without reasonable MIP, 14.5% masked channels, out of which 9.4% with multiple cells)



1.1% of channels with number of events N outside $\pm 4\sqrt{<N>}$ band or with MPV above 100.

Short summary of DESY Jul'13 TB

Improvements:

- Previous test beams suffered from retriggerings / plane events / high trigger thresholds. LLR electronics team found the reason: noise in the power lines. Decoupling capacitors significantly reduced noises in all slabs and improved the performance (many thanks to Remi Cornat and Sebastian Rateau). All slabs can now be power pulsed.
- Many thanks to Gastaldi Franck (LLR), GDCC is in operation instead of LDA. Two GDCC were used in the test beam (and no LDA). Two LDA firmware bugs discovered, rate of lost packets reduced to $\leq 10^{-3}$ (a few % in LDA).

Difficulties with LDAs:
– no possibility to maintain firmware (Xilinx licence is needed for Ethernet interface, current version is obsolete; understanidng of packet management requires reverse engineering)
– not sufficiently reliable (grounding, shielding, connections)

Problems:

- two power supplies (LAMBDA + CAEN) damaged during transportation
- difficult (re)configuration. 0.5 slabs out of 7 were excluded, trigger threshold scans with lots of reconfigs impossible after CAEN failure and power cut
- No beam during 1 + 1.5 days (out of 6 planned, DESY problems)
- production of 2 new slabs started before TB (in LLR, LPNHE, LAL). At the very last step of assembly in LAL in connecting HV Kapton cable to silicon wafer too much glue was deposited which caused a short circuit. Both slabs became not operational. Probably one can be recovered.

What has been done (only the lowest gain)

with 6 slabs
(nobody beleived 7th was "configurable", start with 6 slabs, bad consequence of democracy)
everything in power pulsed and continuous modes:

- MIP position scan (9 points)
- showers with 5 x 4.2 mm W (first layer without W) at 1,2,3,4,5 GeV

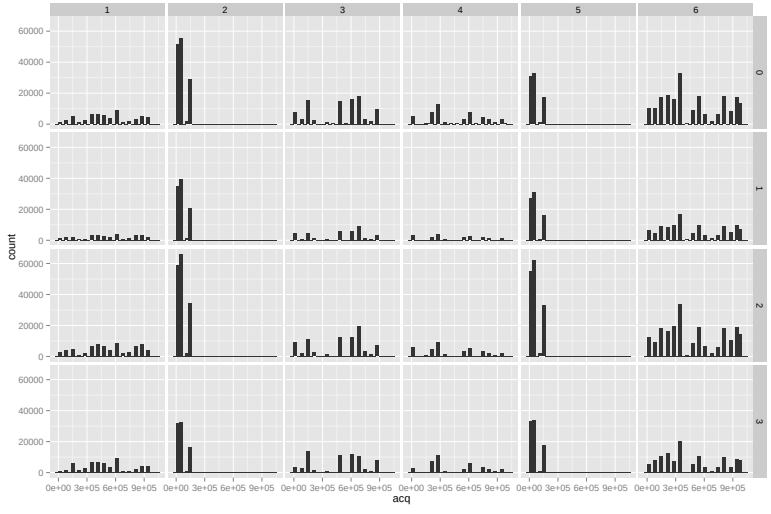
with 7 slabs

- MIPs (center point only)
- 6.3x3 mm (in front) + 6x4.2 mm W (between layers) only at 2 GeV
- 6.3x3 mm (in front) at 2 GeV
- spill frequency scan 5-100 Hz (nominal point - 10 Hz)
- combined Si-Sc run at 2 Hz, only spill synchronization (not BX)

No trigger delay scan (delay=130 as in Feb'13)

Problems in DESY Jul'13 TB

- (Re)configuration: random faults, 5 tries in the standard procedure, sometimes not enough. Contrary to expectations, ARDUINO resets of GDCC/LDA are necessary before every configuration. Trigger threshold scans with many reconfigurations not possible after power cut on Jul 5
- Data taking at 10 Hz spill rate. At higher rate: spill number is not continuous (bug), eg. 25 Hz, CC mode



Except spill number, **no degradation is observed at higher rate, eg. fraction of lost packets in GDCC even decreases**

spill rate	10 Hz	25 Hz	50 Hz
lost packets rate, in 1e-3	1.0515184	0.1722125	0.1563151

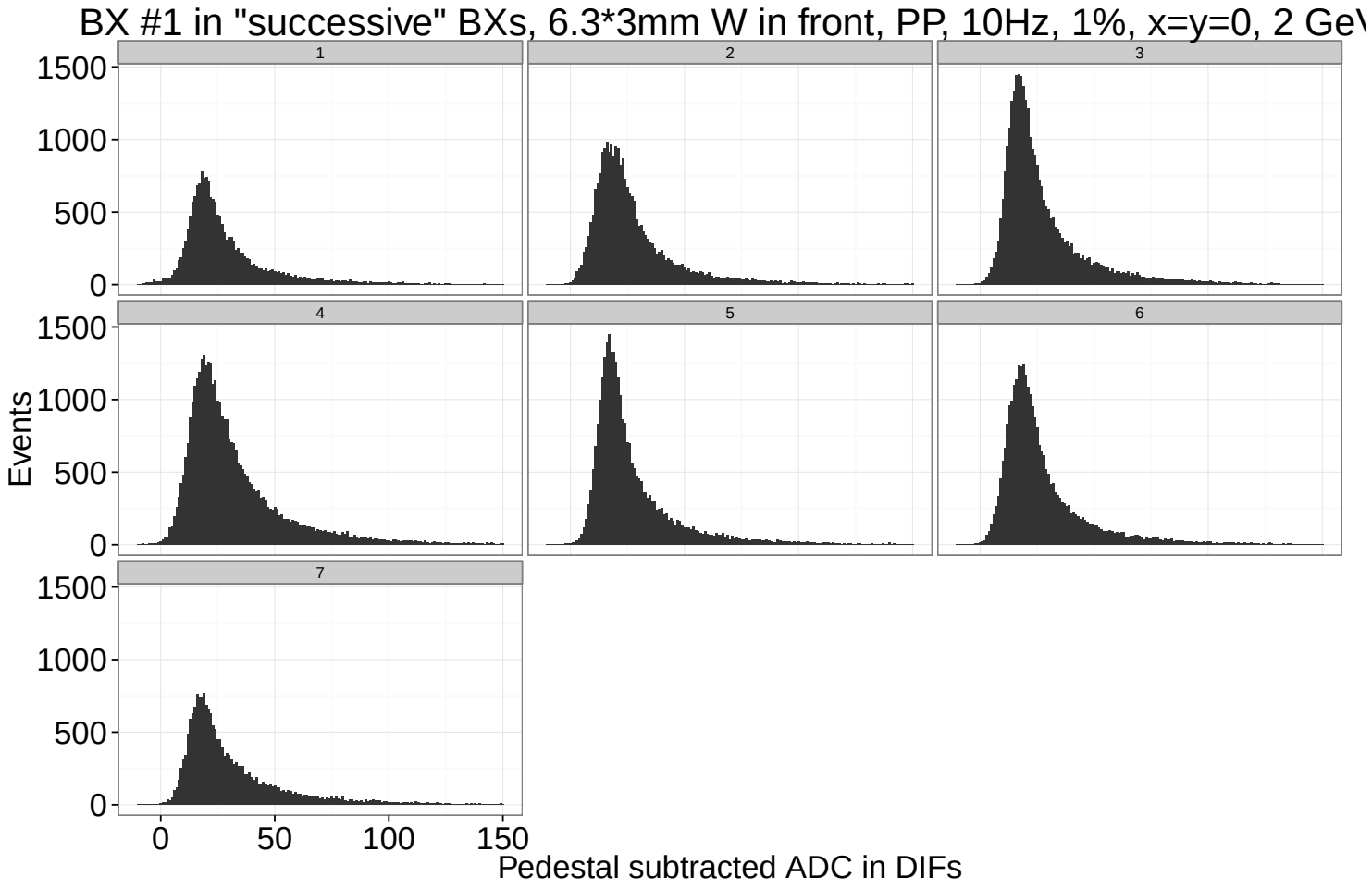
Slabs availability

- 10 slabs after TB Feb'13, two are bad
- 2 new slabs have been produced, but not operational because of HV shorts
- One slab was not taken to DESY (not "configurable", it was working in mid. June: should be rechecked!) $\rightarrow$ 7 slabs in DESY

3 out of 7 slabs with different firmware (test of twice shorter delay after powering ON in power pulsed mode to allow all transitional processes to finish), different timing should be compensated offline

Plan to repare as many slabs as possible and produce new ones to fill 15 alveolars in big mechanical prototype (3/5 of full scale module) for tests in CERN next year. If there will be spares: one slab for tests to LAL, Kyushu and Tokyo (the latter two will need also CCC and LDA or GDCC).

MIPs



Next step: build full event out of independent slabs (never in the past). Spill number at 10 Hz is (almost always) synchronized, BX number - within ± 1.