# Test of Power Pulsing with the HBU-LED System





Shion Chen

DESY FLC AHCAL group Calice Meeting 10. Sep. 2013





# **Challenges of Engineering prototype**

Front-end electronics readout
 Integrated design of active layer and electronics

induce another problem

Heat

Power pulsing!!





WLS guide

# **Concept of AHCAL Power pulsing**



(B. Hermberg, M. Reinecke, M. Terwort (2012))

- ILC beam bunch structure: Ims beam-on / 199ms off
- Turn off the power not in use
- The power of SPIROC is delivered by 4 different power supplies
- pw\_a, pw\_adc, pw\_d, p\_dac:

Power control signal for analog/ADC/digital/others part of SPIROCs

Activation time T\_on: How short can we make it? / what effect will limit T\_on?

# Previous study with charge injection with IHBU

by B. Hermberg



- Shoot charge pulse directly into SPIROCs Checked the output signal
- Amplitude drops in the beginning
- Need ~Ims to stabilize
  Many discussions, but not understood
  Measurements with different setup might give clues
- Data quality after Ims looks nice Test with more realistic setup
- $\Rightarrow$  Scintillator + SiPM system / multi-HBUs !!

### Setup

Calibration LED on each channel



#### **(1)** LED light $\rightarrow$ Scintillator $\rightarrow$ SiPM raw signal

- ② Goes to ASICs via wires (same as charge injection)
- ③ ASICs process trigger, shaping, digitizing etc.
- ④ Stored in the memory in ASICs
- (5) When one memory of channel becomes full, signals are readout to DIF board then outside



### Setup

#### Calibration LED on each channel



- IHBU setup
- 3HBU setup
- 6HBU setup (ILD model)



#### Analysis

- $\cdot$  Shape
- Amplitude, Gain
- External trigger mode

Clocked by DIF

Varying T\_on, trigger distance, number of HBUs (1,3)



### 1**HBU - noPP mode**

T\_on: | | µs trigger distance: 60µs

(Chip 213, channel 10)



# 1HBU - PP mode

T\_on: | | µs trigger distance: 60µs

# Crazy shortly after power-on, gradually come to normal



### **Gain** Peak distance between pedestal and I.p.e



# Gain IHBU

Gain drops restore with T~Ims

(noPP) (PP) T\_on: I I µs, trigger distance 330µs (PP) T\_on: 22µs, trigger distance 63µs (PP) T\_on: 22µs, trigger distance 330µs



Gain ratio of w/ to w/o PP mode





# Gain IHBU

Gain drops restore with T~Ims

#### Comparison with charge injection

Consistent behavior



Charge injection





### 3HBU - PP mode

T\_on: 24µs trigger distance: 190µs

(Chip 213, channel 10)

#### signal quality is fine after the duration









3ms after power-on

Gain 3HBU setup



# Discussion

Why does gain drop?

Not the problem of SiPM
 Same effect (quantitatively) in charge injection
 Pre-amp gain looks actually drops

■ Stabilization time depends on #HBUs
 ⇒ At least not only the problem of SPIROCs

The power supply to the analog part of the SPIROC (VDDA) is directly checked via oscilloscope.

#### IHBU:

VDDA shows a drop (~25mV) after poweron. T~1ms

3HBU:
 Voltage drop ~100mV, τ~2ms

Clue?  $\rightarrow$  VDDA should not affect gain



3HBU





# Summary

- Power pulsing measurement with HBU-LED setup is on going
- Good quality data can be acquired with power pulsing operation after 1~2ms, even with 3HBU setup
- Gain drop is confirmed quite consistently with the result of charge injection study
- But the reason is still not clear, need further investigation

# Outlook

- Further analysis on gain / pedestal
- 6HBU setups measurement are ongoing

# Acknowledgement

Many thanks for Katja, Mathias, Ali, Coralie, Oskar



### Thank you for the attention





# Backup

### Amplitude



#### **1HBU** amplitude curve



19



#### Comparison with IHBU

Need more time to stabilized (~2ms)



### **Geometrical Optimization in terms of PFA**



#### **Pedesta** ADC dist. of channels without scintillator/SiPM attached

red: no PP blue: with PP



# SPIROC2b



#### **IHBU** noPP



chip:214 chn7

#### **3HBU** noPP amplitude curve



26

### **RC** component between VDDA - Preamp



 $\tau = R \cdot C$  VI=V2 (off) VI=V2-0.2V (on)

### Gain drops in charge injection study

10Ω



### Gain drops in charge injection study



#### Power consumption estimation in current chip design



time window	$I_{VDDA}$ [mA]	$I_{VDDD}$ [mA]	time [ms]
t1	498.47	30.33	0.9
t2	519.47	37.56	0.1
t3	245.20	36.79	3.2
t4	0.71	29.31	150
t5	0.56	0.01	45.8

TABLE 1: Table with the different currents and times.

Power	$P_{VDDA}$ [mW]	$P_{VDDD}$ [mW]	P [mW]
P1	7.40	0.45	-
P2	0.86	0.06	-
P3	12.95	1.94	-
P4	1.76	72.54	-
P5	0.42	$7.56 \cdot 10^{-3}$	-
$P_{VDAC}$	-	-	0.05
$P_{VRef}$	_	_	1.89
$\sum \mathbf{P}$	$100.32 \mathrm{~mW}$		

TABLE 2: Table with the different power consumptions.