First layers of the Si-W ECAL technological prototype in test beam

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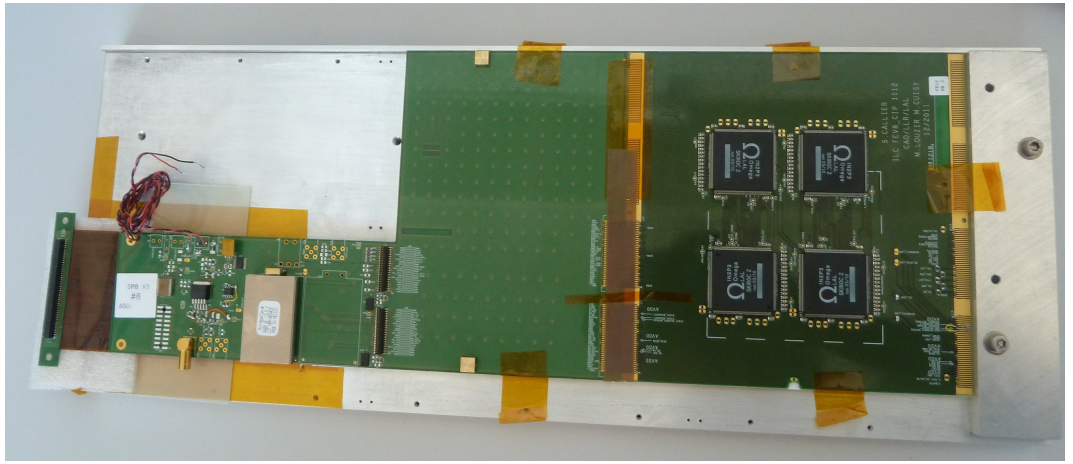
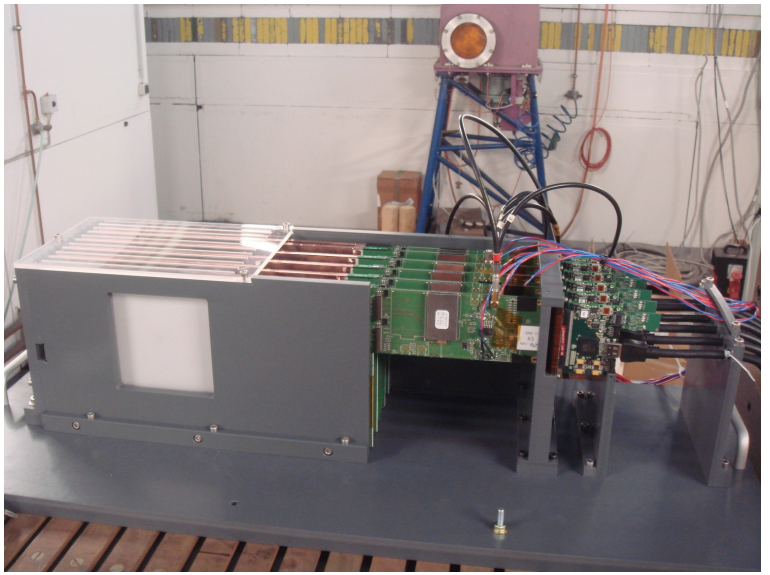
The road to the Si-W ECAL technological prototype

Intermediate step: Conservative layer design for beam tests

- First test in beam
- Benchmark to go further





- Single detection layer per slab (U structure)
- Si wafer:
  9x9 cm^2 – Thickness = 320 μm
  pixel size: 5x5 mm^2 :lateral granularity = 4 x better than physics prototype
- SKIROC2 ASICs
- 4 ASICs per slab (1⁄4 final design) - conservative design (chip in package)
  4 SKIROCs x 64 channels = 256 channels/slab

Beam tests @DESY - summary

Summer 2012

- 6 layers
- 1 LDA
- DAQ soft v0

- Debugging electronics (SKIROC2, PCB...)
- Establishment of calibration procedures
- Measure of S/N

Winter 2013

- 8 layers
- 2 LDA
- DAQ soft v1

- Power Pulsing

Summer 2013

- 6 layers
- 2 GDCC
- DAQ soft v1

- Power Pulsing
- Showers

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Main results shown by Nathalie and Yuji @ previous CALICE meeting

Summer 2013
- 6 layers
- 2 GDCC
- DAQ soft v1

- Power Pulsing
- Showers

Beam tests @DESY - summary

Summer 2012

- Debugging electronics (SKIROC2, PCB...)
  - plane events
  - BCID+1
  - Noise
- Establishment of calibration procedures
  - Trigger Threshold calib ~ OK
  - Trigger delay calib ~ OK
  - Energy calibration

- MIPs and showers
- no power pulsing
- Position scan
- Several gains (main Cf = 1,2pF)

Summer 2013

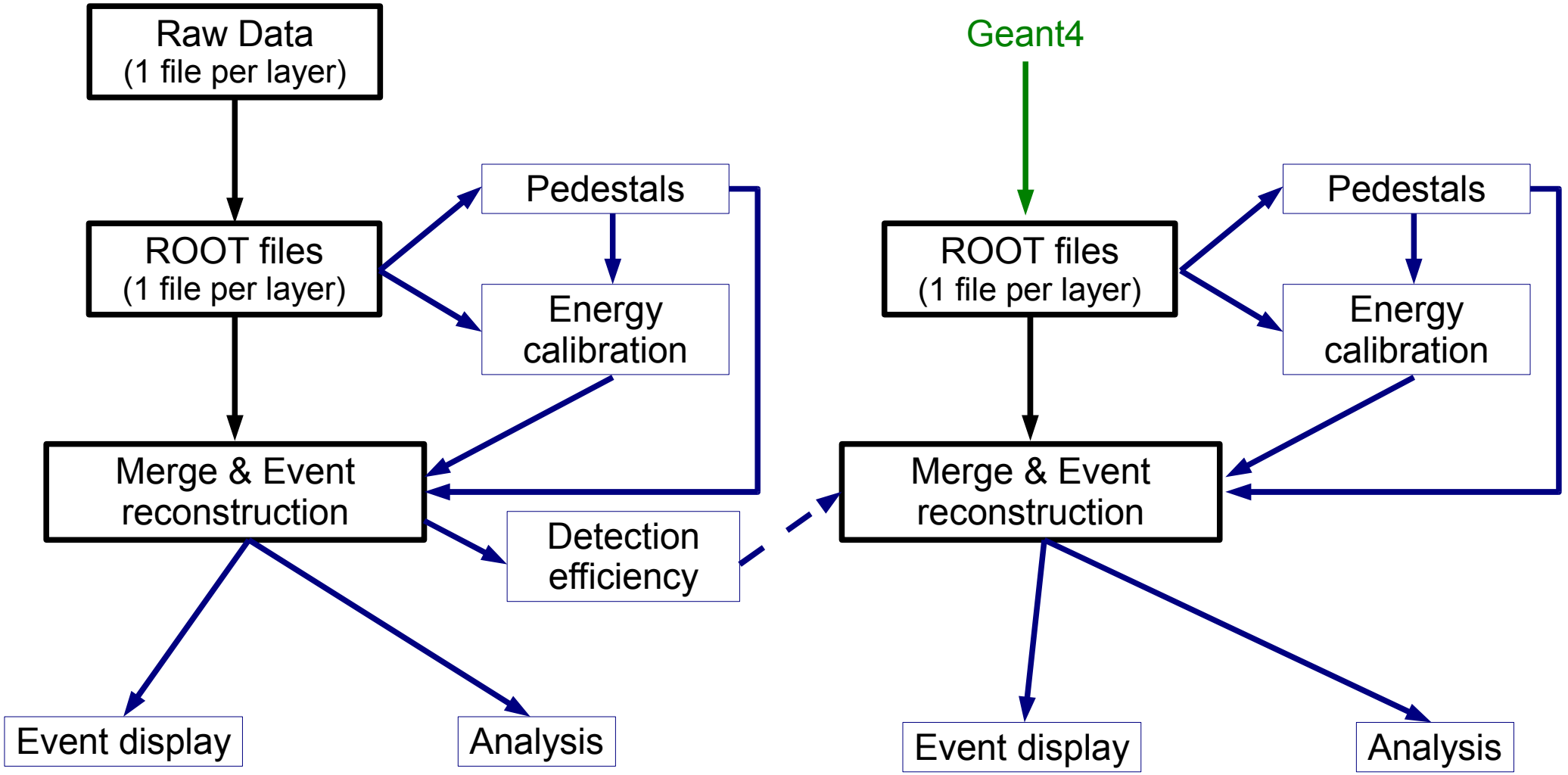
- Power cycling, GDCC
  - heavy debugging (5 days) → quick and dirty procedure to switch on the setup
  - Blind detector:
    - No trigger threshold calibration
    - No trigger delay calibration

→ Thanks to Franck, Frédéric, JB, Jérémy, Mickael, Rémi

- MIPs and showers
- power pulsing mode (PP) and no power pulsing mode (CC)
- Position scan
- 1 gain (Cf = 6pF)

Software / Simulation

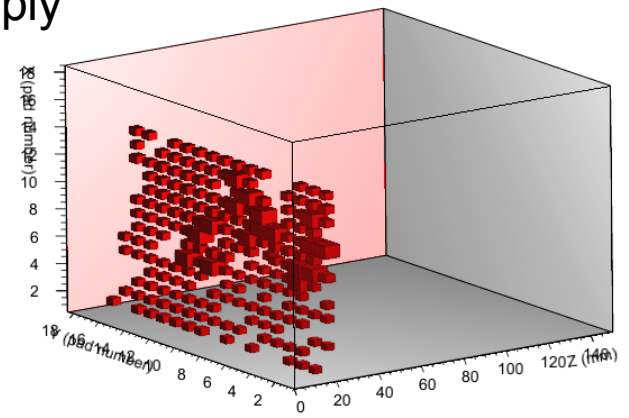
Same tools as previous TB (few improvements)
MC used same data structure with additional information



Data quality - Plane events (Summer 2013)

Instabilities of power supply level → fake events

- All layers with additional capacitors to stabilize power supply



Ratio (plane events) / (good events) in Summer 2013

MIPs:

CC: ~20-40% (winter TB modified slabs: ~10%)

PP: ~60-200 %

(For BCID+1: ~20-40%)

* difficult to compare winter TB and summer TB: not the same gain, trigger threshold...

* As expected, capa reduce frequency of plane events BUT also the number of hits in a plane event ==> difficult to separate plane events and good events

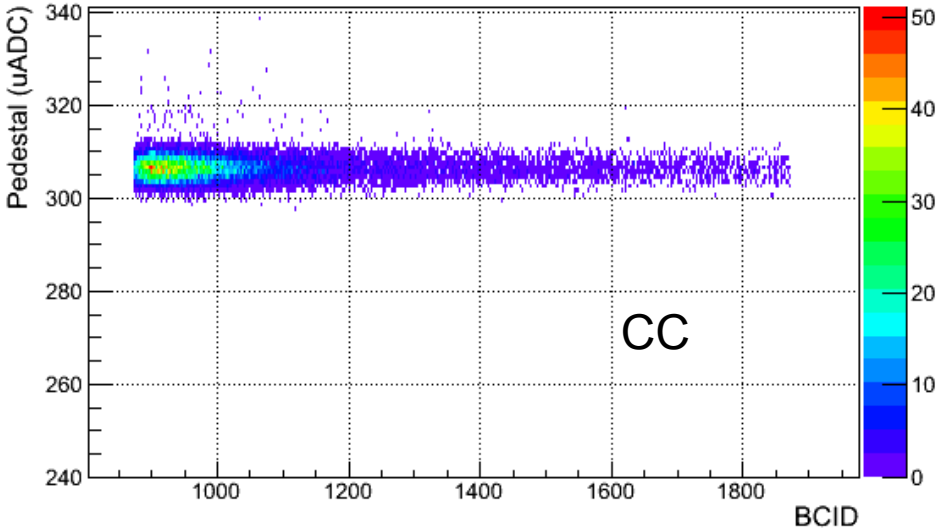
Data quality - BCID synchronization (Summer 2013)

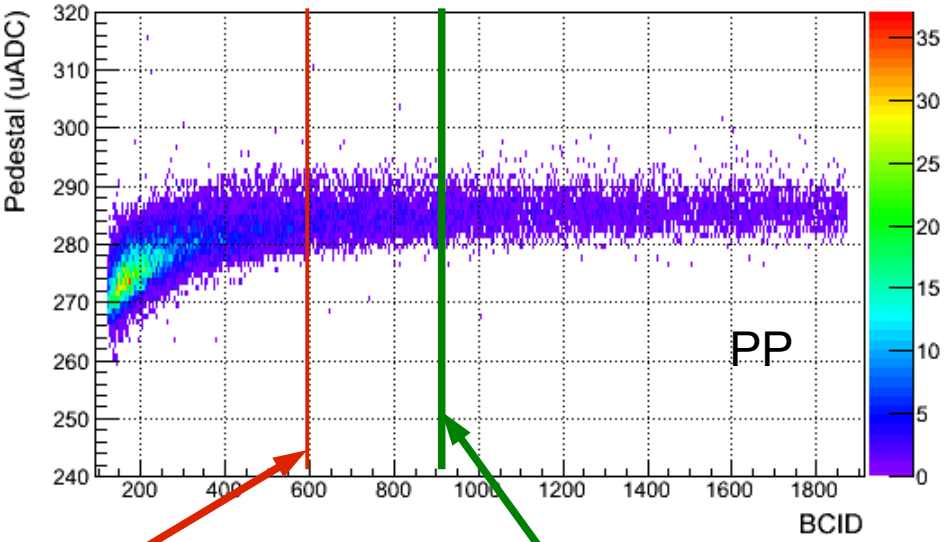
2 DIF with bad firmware version (dif 2 and 5):

1/ not the same BCID counter reference (easy to patch)

2/ start to take data earlier:

- CC mode: first data lost for reconstruction of MIPs or showers
- PP mode: electronics are not stabilized before 600 BCID (see figures)
  - * data lost for all analysis
- all modes: increase the probability to have an ASIC full before other DIFs
  - * reduce efficiency
  - * increase probability to have less than 6 layers in an event



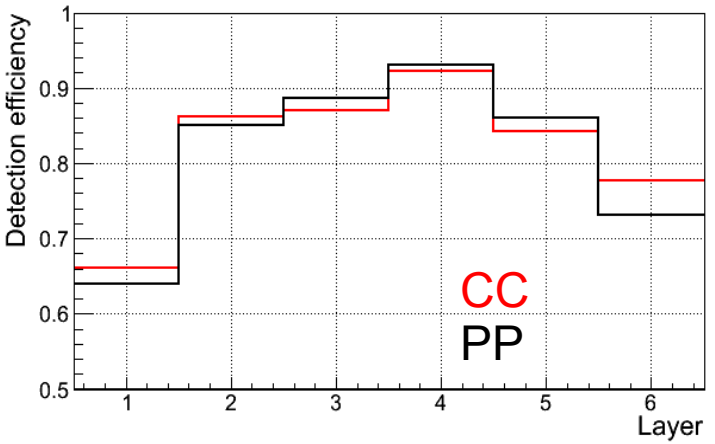


BCID cut for DIFs with bad firmware

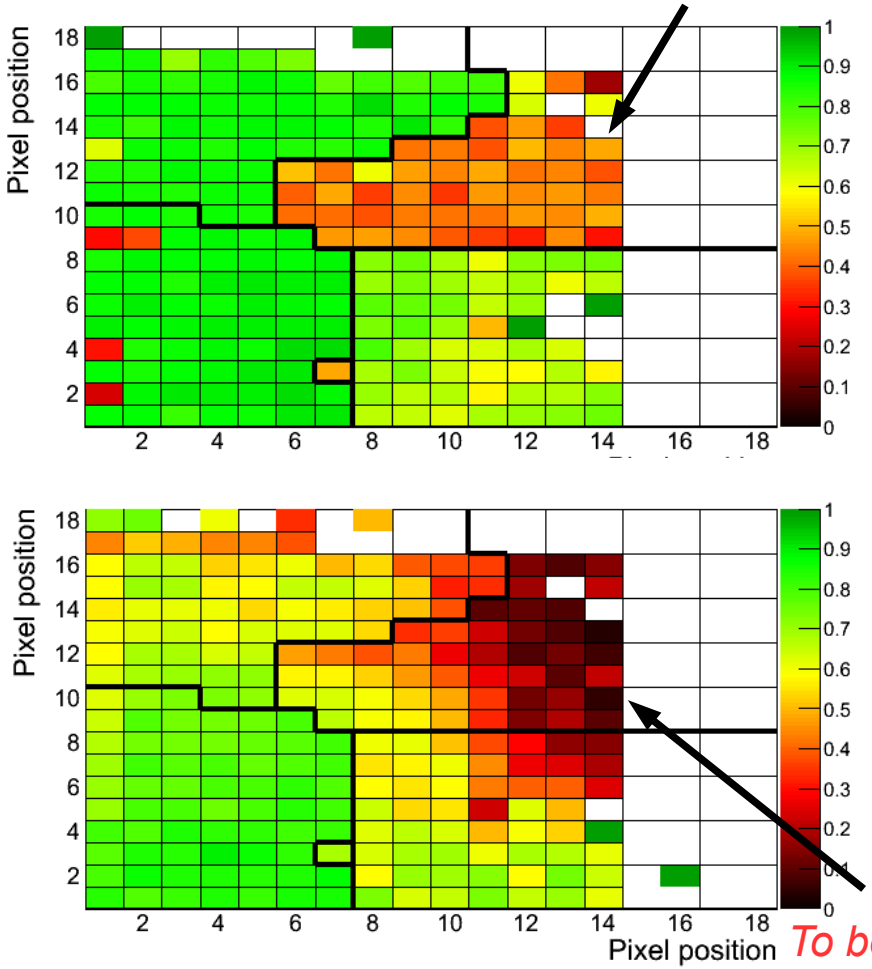
Start of others DIFs

Detection efficiency (Summer 2013)

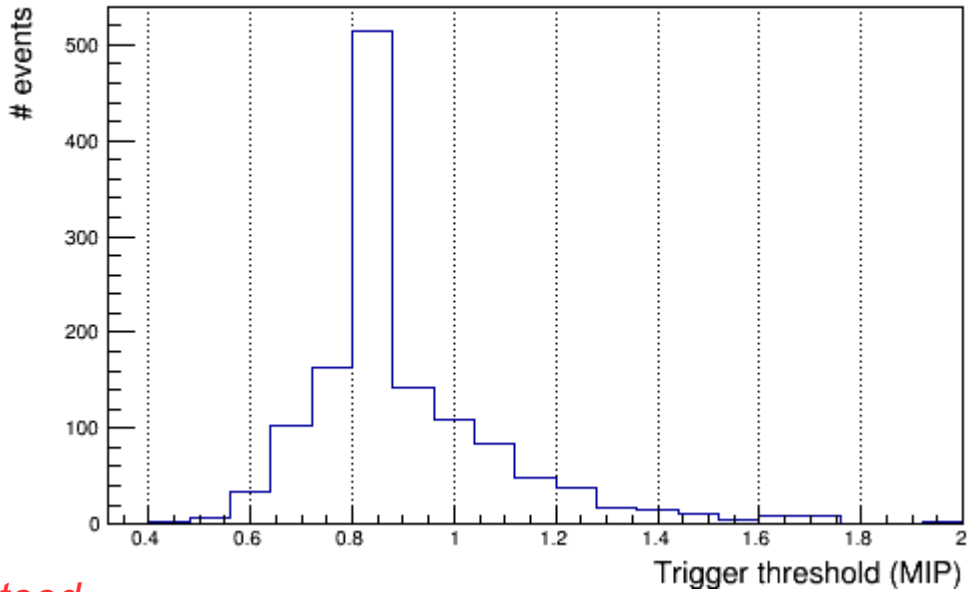
* Same tools as previous TB
* Select events:
  - without inefficiency due to full ASIC
  - without inefficiency due to DIF firmware problem
  - at least 4 layers with hits
  - only 1 incoming particle



Trigger threshold too high

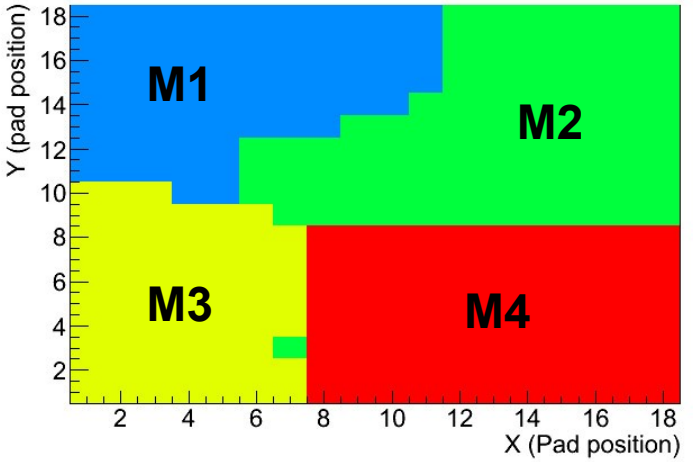


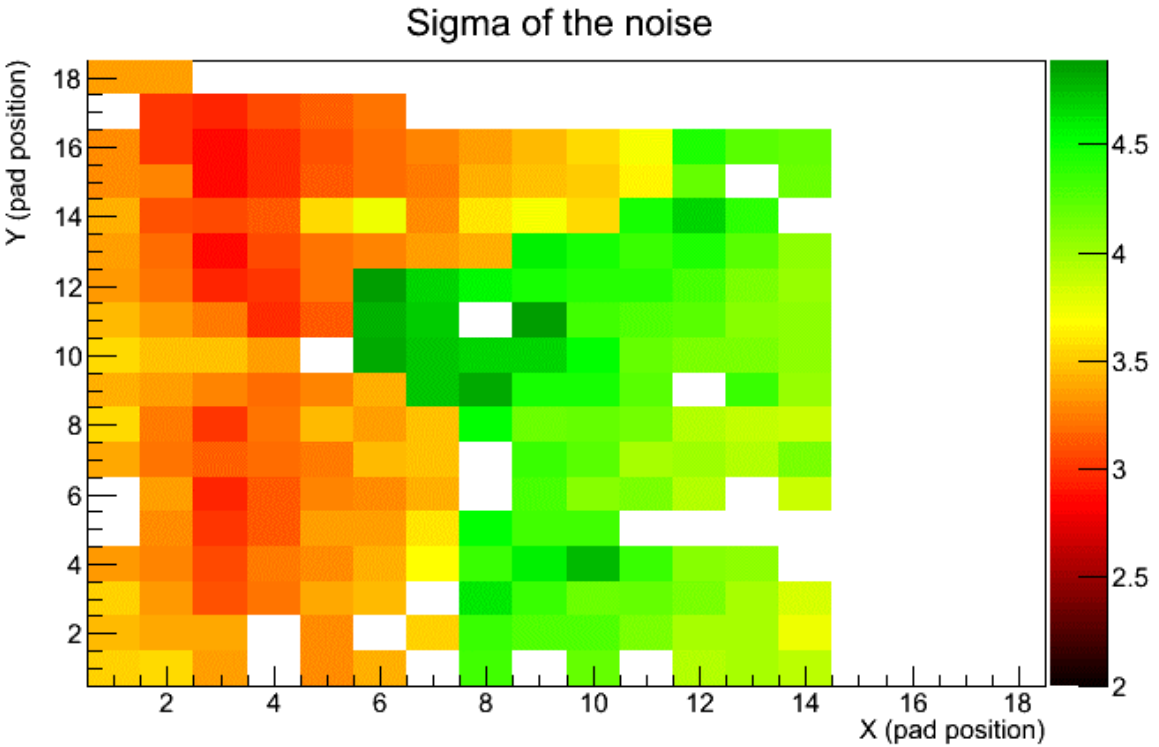
High dispersion in some layers
Used to define trigger threshold in simulation
→ Need trigger threshold per channel in simulation (done)
→ Inefficiency due to plane events (to be done)



To be understood

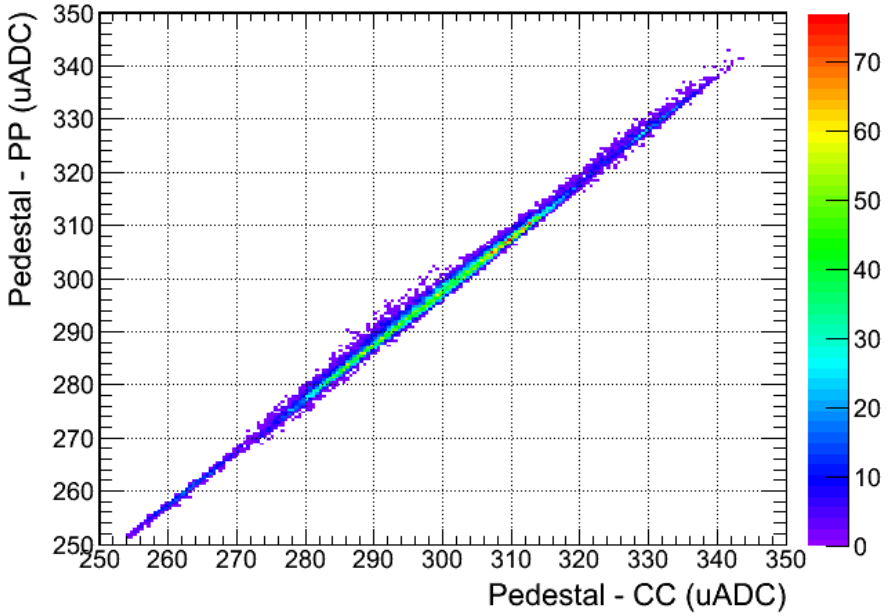
Reminder – Noise in 2012 TB

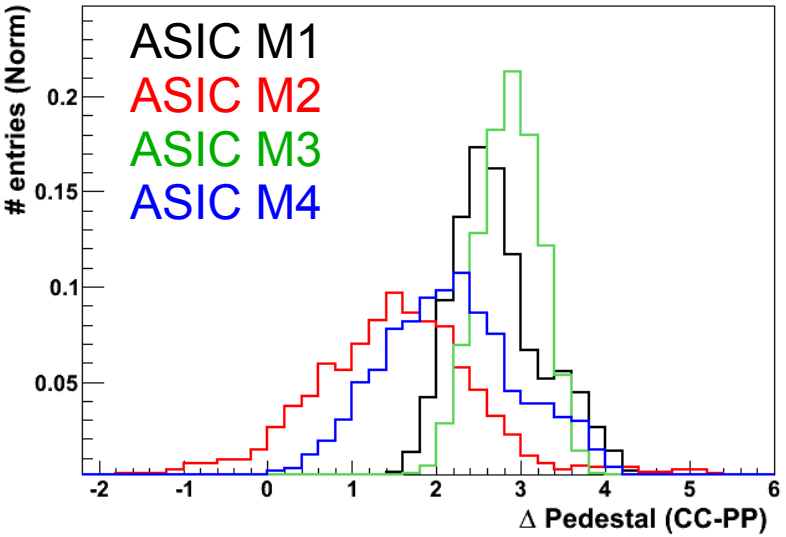


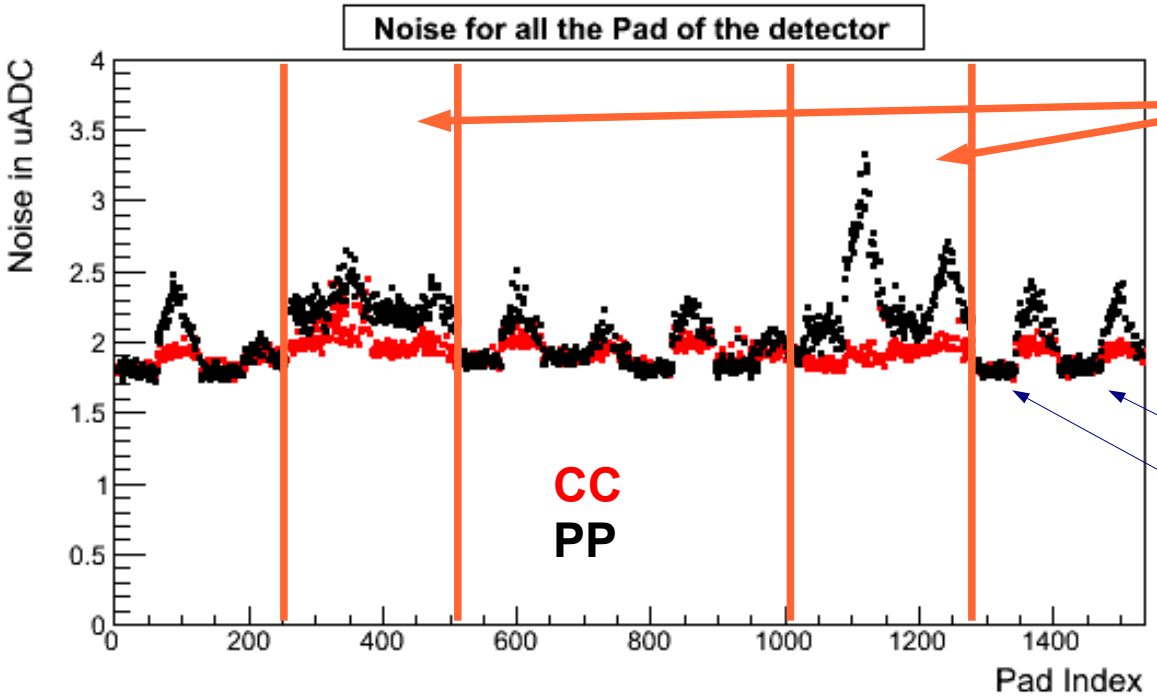


Comparison CC \ PP - Pedestal (2013)

(BCID cut for bad DIFs firmware is applied)







DIFs with bad firmware

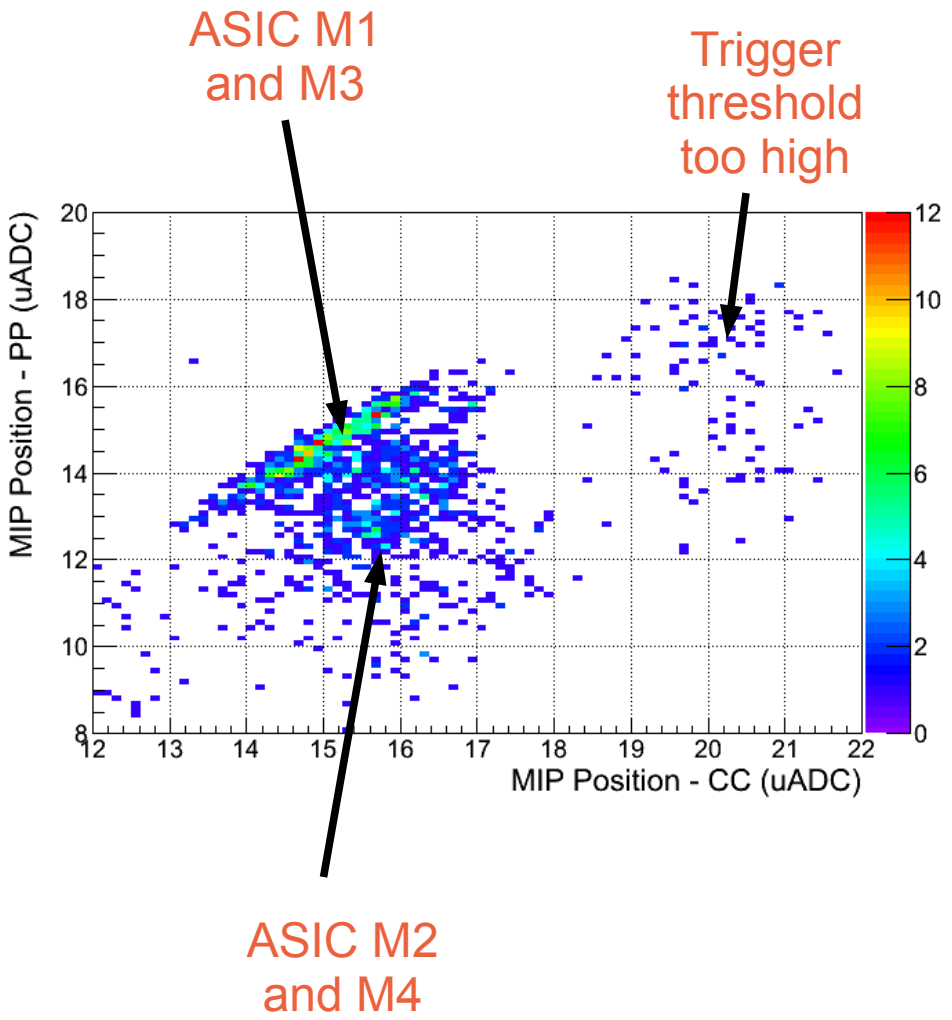
(BCID cut for bad DIFs firmware is not applied)

ASIC M3
ASIC M1

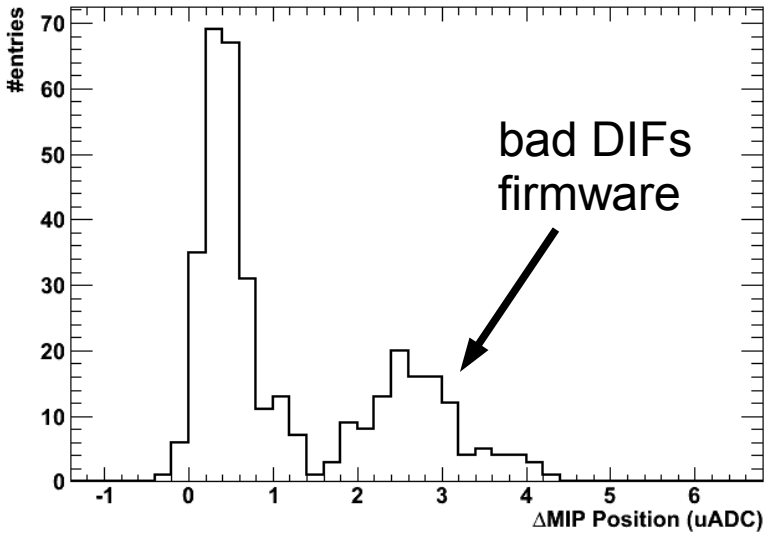
Same noise pattern as 2012 TB
PCB routing has additional effect in PP

Comparison CC \ PP - Energy calibration (2013)

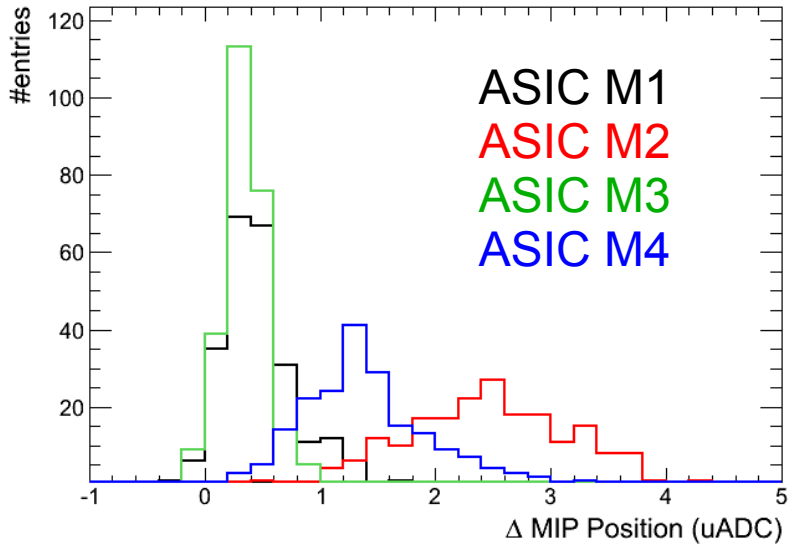
Fit energy distribution: Landau convoluted with a Gaussian
Sigma of the Gaussian is fixed to the noise



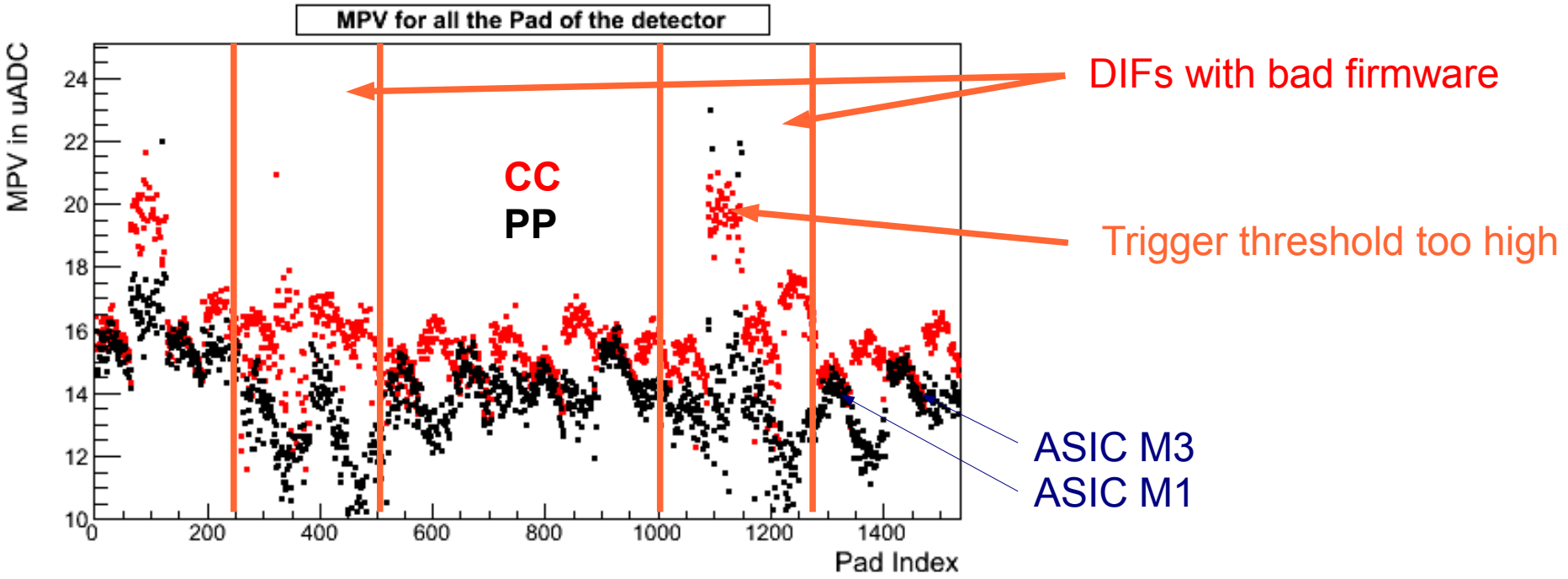
ASIC M1 – all layers



Layer with bad DIF firmware excluded



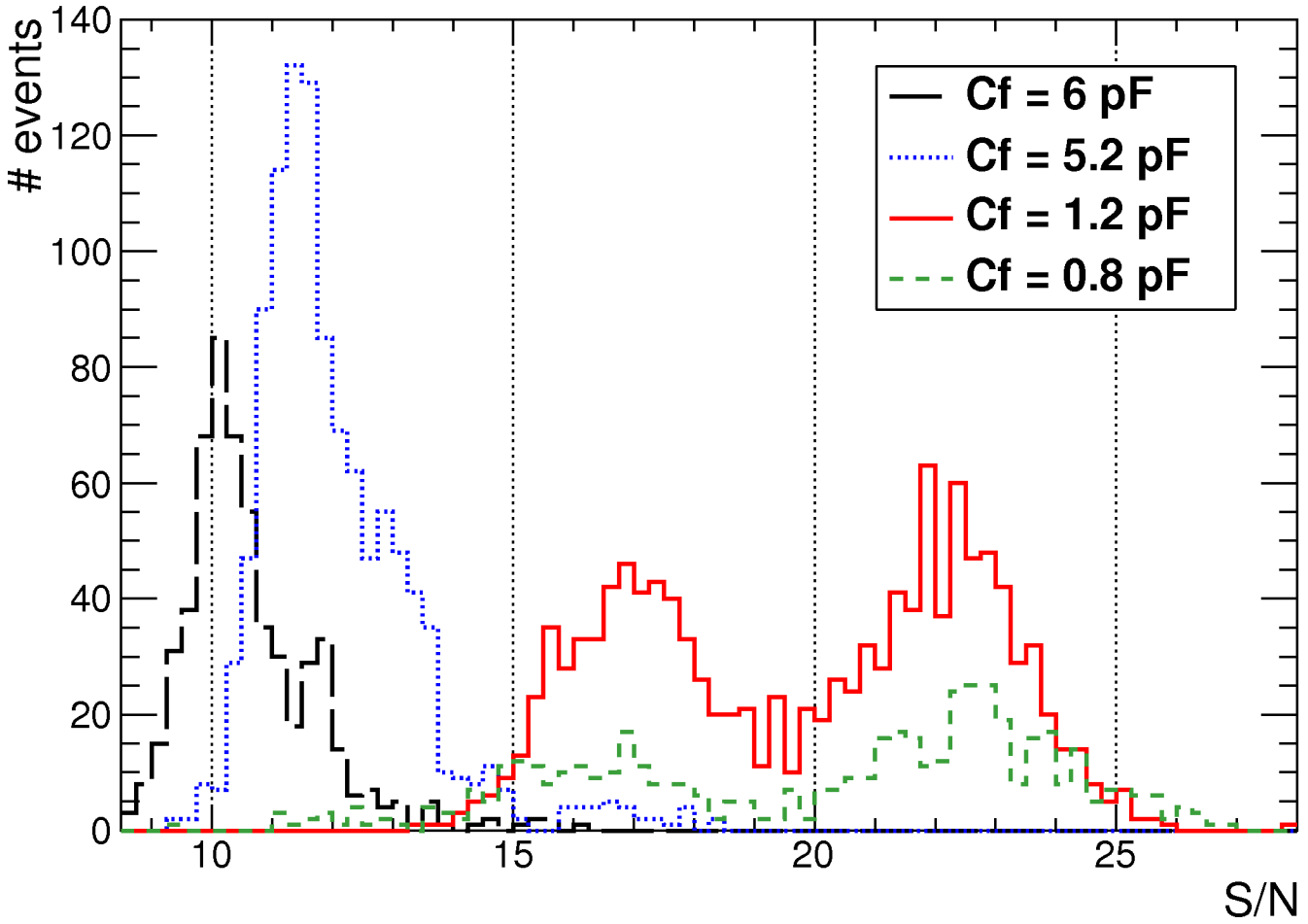
Comparison CC \ PP - Energy calibration (2013)



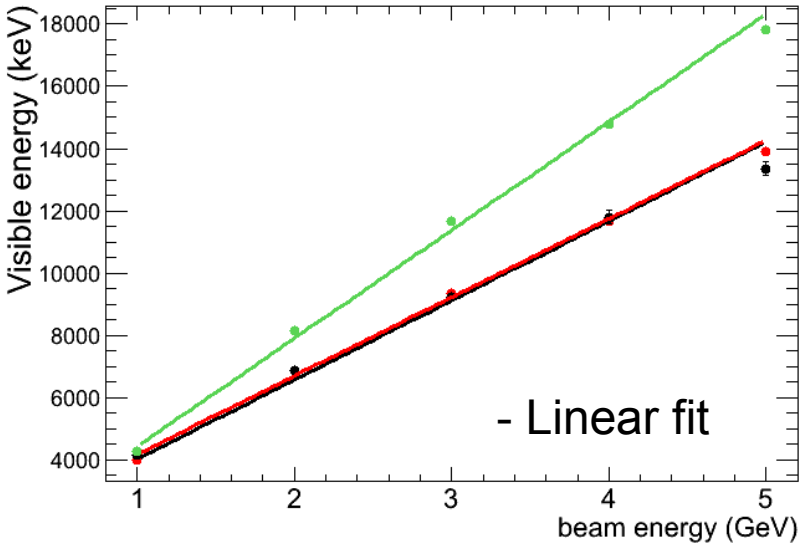
* No trigger delay calibration: response not optimized → bad S/N
* 2012 TB: response flat as a function of the channel number (trigger delay calibration?)
* PCB routing seems to have effect on energy calibration (@ pedestal subtraction step?)

Signal over noise (2012)

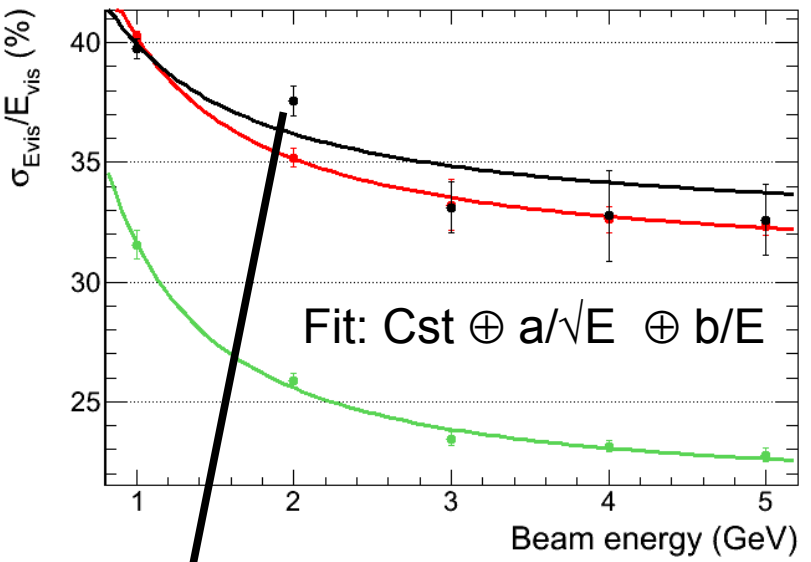
2013: No trigger delay calibration: response not optimized → bad S/N



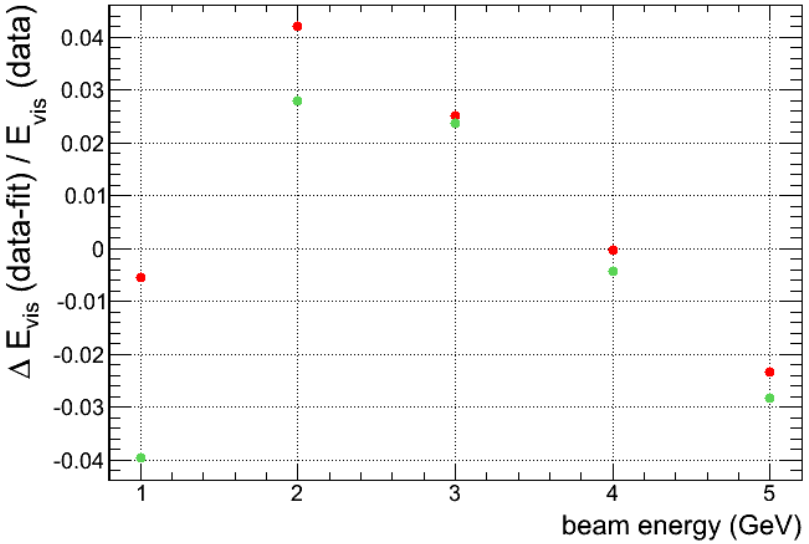
Showers (2013)



CC
PP
MC



The PP fit is disturbed by one bad value.



--> same non linearity effect in MC and data

On going: Inefficiency due to plane events

Conclusion

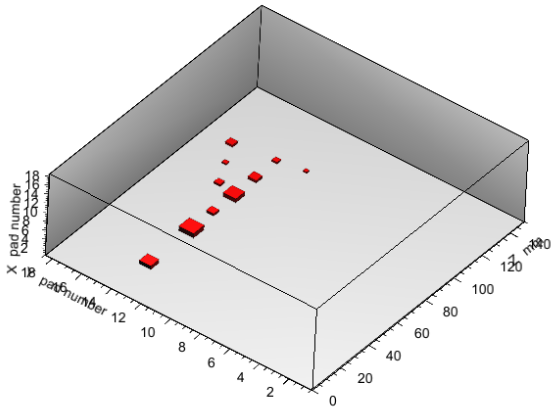
2012 results describe in CALICE Internal Note CIN-023 → Upgrade to publication
==> Successful test beam campaign

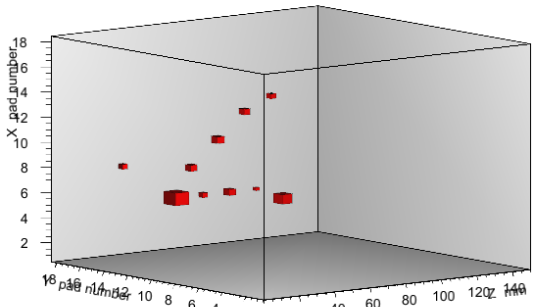
- encouraging results
- identification of open issues

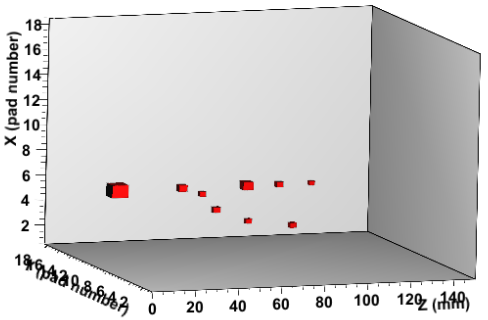
Summer 2013: useful results especially concerning power pulsing studies

- Finalize 2012 / 2013 shower analysis
- Internal Note to summarize power pulsing studies

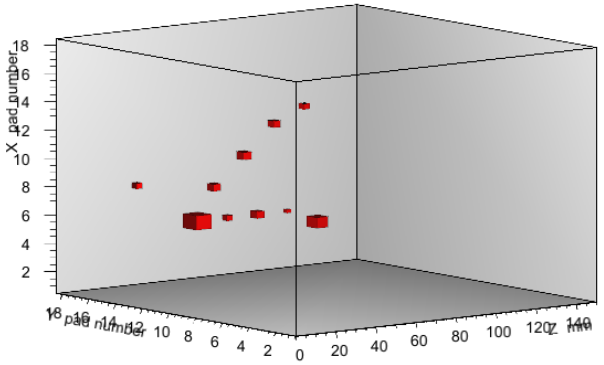
Thanks to all people who have a positive impact on the Si-W ECAL developments



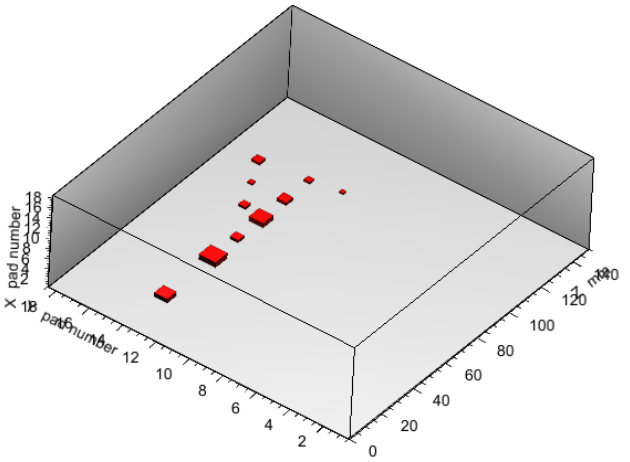




Event display



MIP



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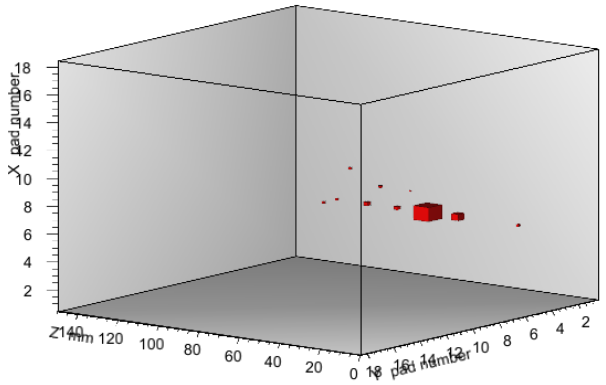

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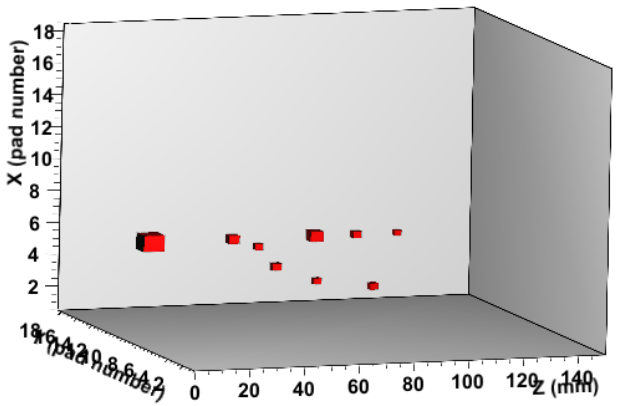

MIP