AHCAL Data Acquisition System

From a single layer towards multi layer DAQ

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HELMHOLTZ ASSOCIATION

Universität Hamburg

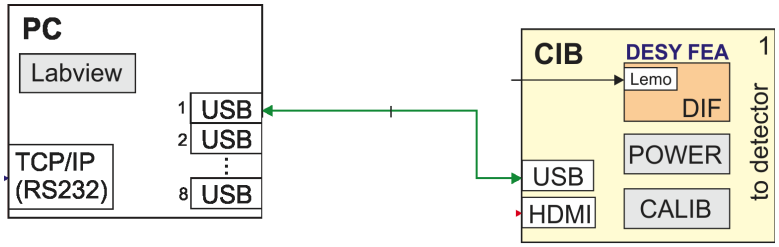
DESY

Overview

- Development roadmap
- Multilayer DAQ
  - DAQ Software
  - Clock and Control Card(CCC)
  - Link and Data Aggregator(LDA)
- Performance of the multilayer DAQ
  - Stability
  - Timing
  - Synchronicity
  - Power cycling
  - Compatibility with other detectors
- Summary and Outlook

Development roadmap

- Single layer DAQ system
  - Operated with LabView on a PC
  - USB interface to front-end
  - Local clock generated on the Central Interface Board (CIB)
  - Readout frequency of ~1.5 Hz



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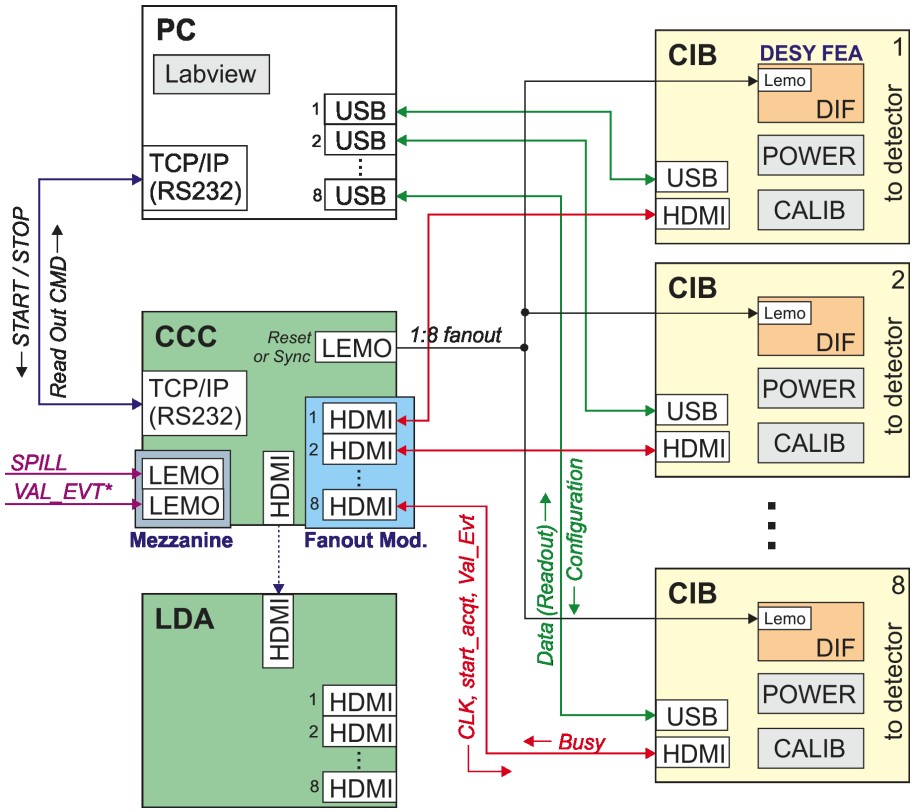
- A multilayer DAQ requires
  - Hardware/Firmware modifications
    - New hardware
    - Global clock Generation
    - HDMI implementation
  - Software modifications
    - Multithreaded software
    - Multiple-DIF configuration
    - Parallel readout



AHCAL multilayer DAQ design concept

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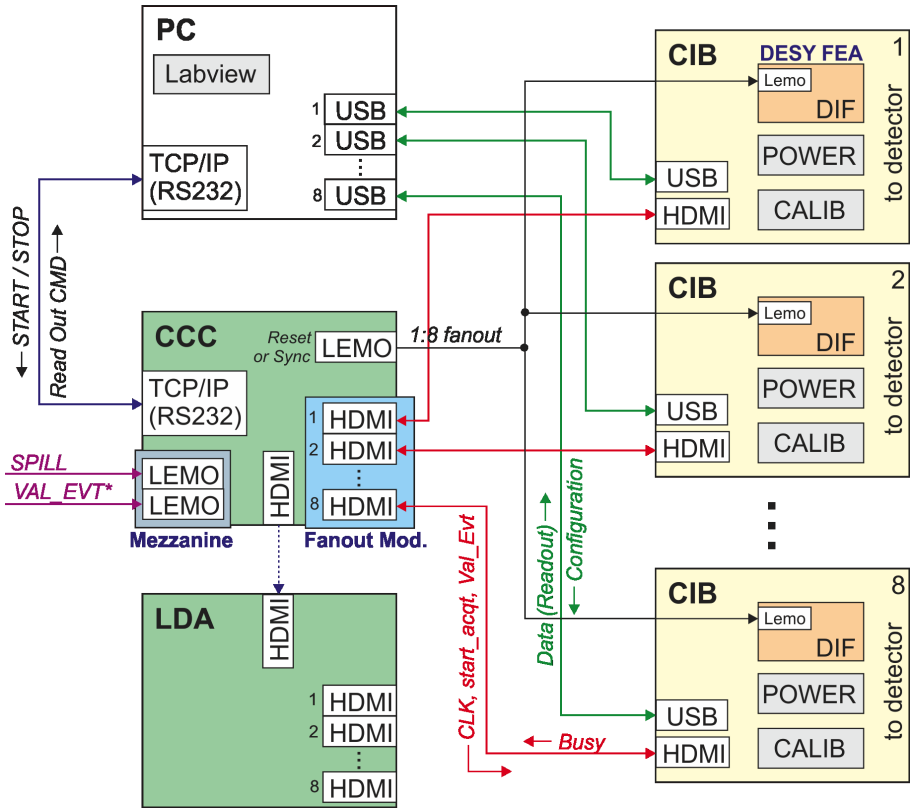
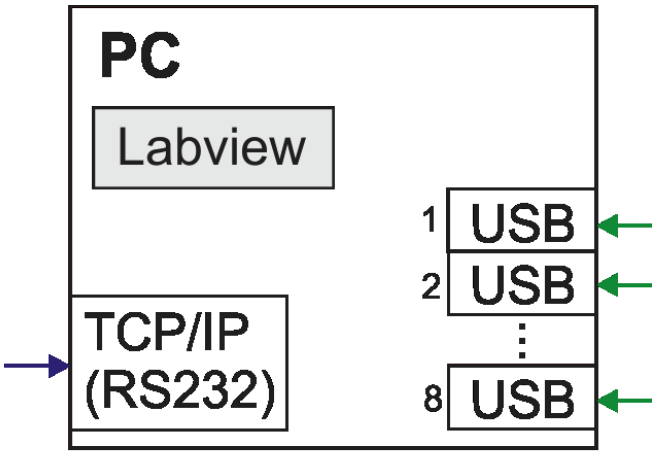
- Our development strategy
  - Building up on the single layer DAQ system
  - Follow a stepwise approach towards a multilayer DAQ system

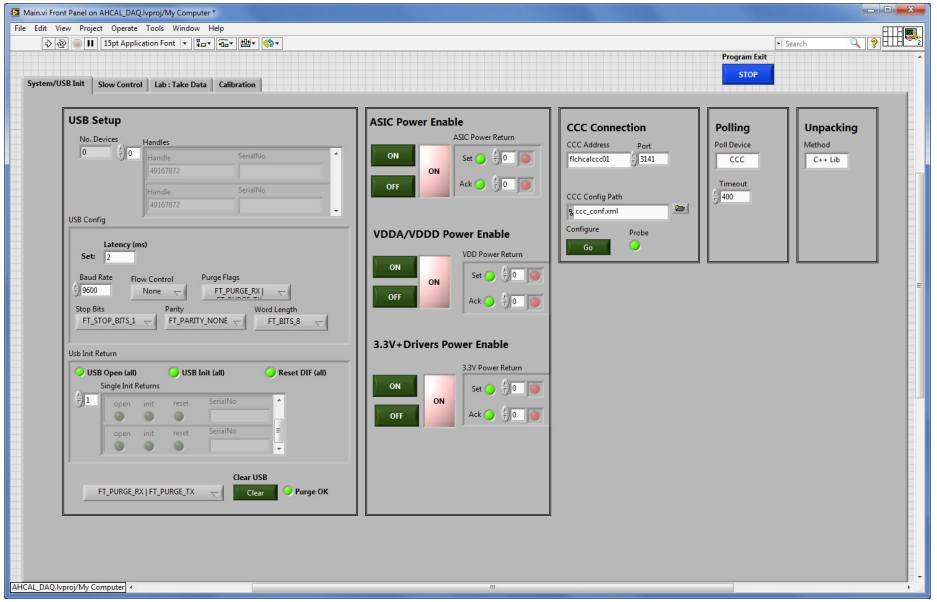


PC / Software

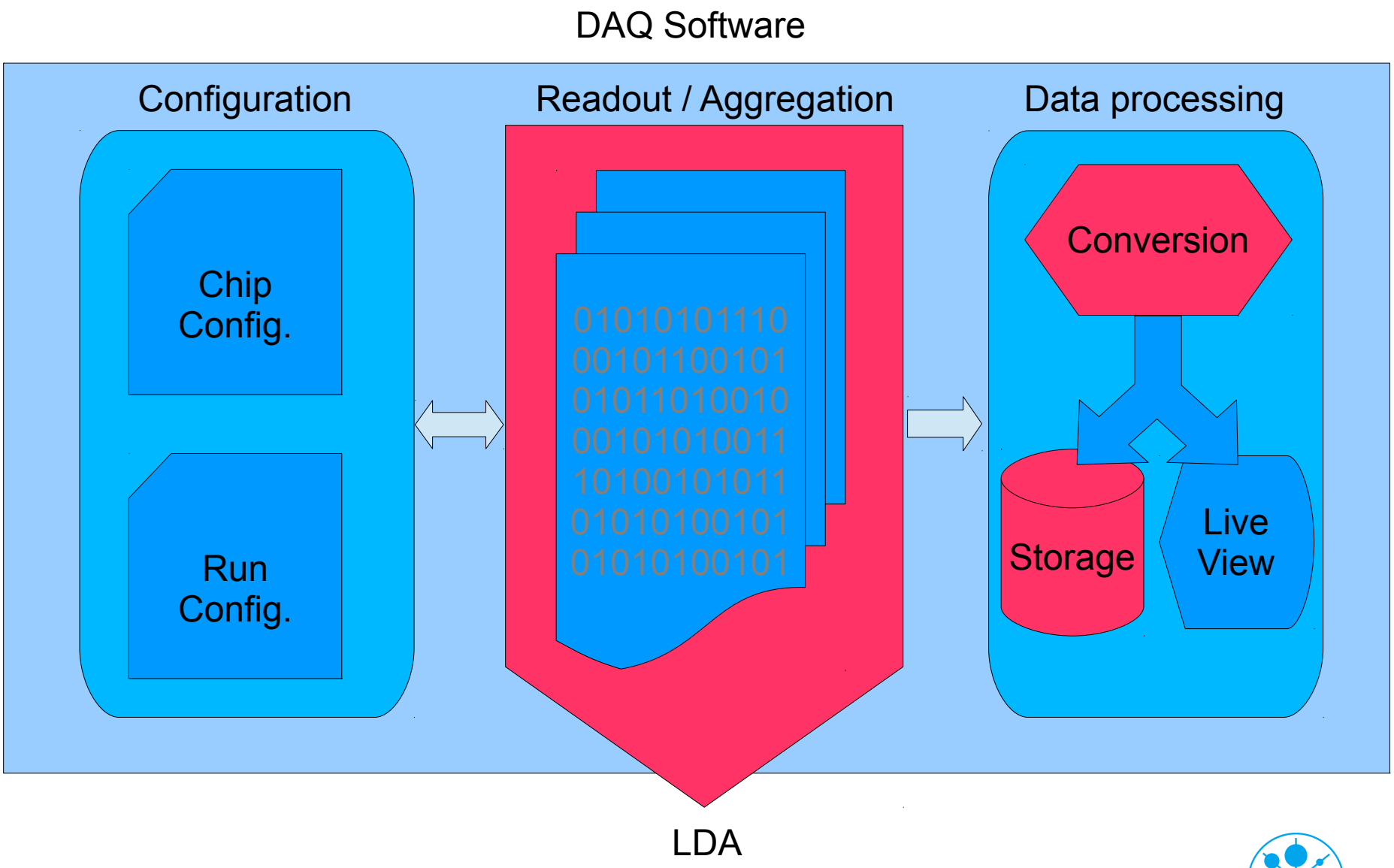
- PC specification
  - Intel quad core processor
  - 8 GB of RAM
  - Windows operating system



- DAQ Software
  - Based on LabVIEW
    - Flexible
    - Easy to create GUI
    - Easy and fast modification/debugging
  - 50% rewritten
  - Fully multithreaded
  - Now is Modular
  - Some tasks are done using C++ libraries added to the LabVIEW

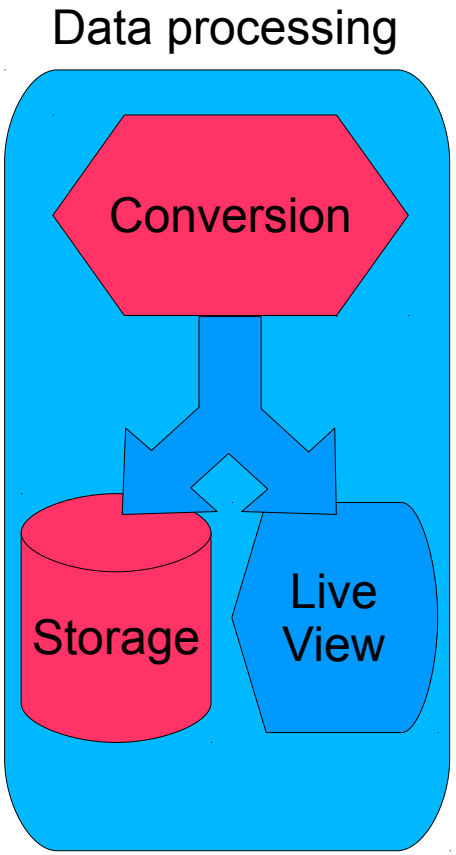


AHCAL DAQ Software



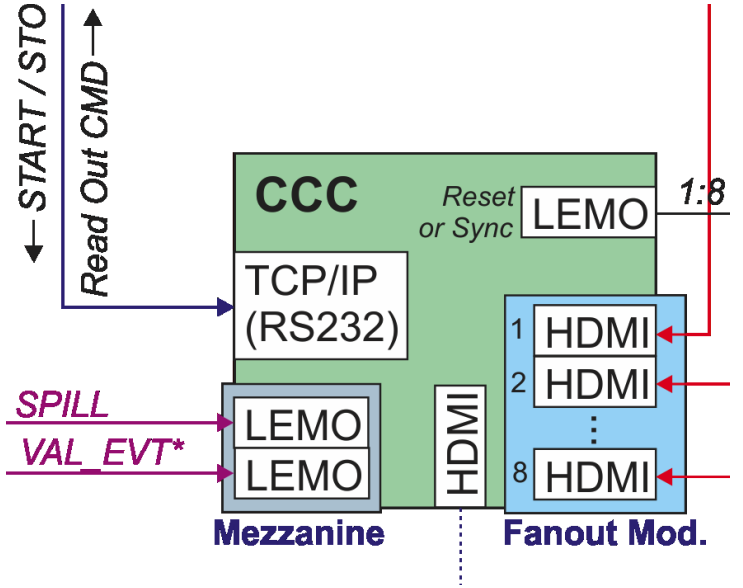
Using C++ library for conversion

- A C++ windows library (DLL) is developed to replace native LabVIEW “Conversion”
- Conversion using standalone library is a factor of 5 faster
- Conversion by calling the C++ DLL from LabVIEW is ~20% faster
- It can write out ASCII files for storage
  - This feature is not used in current version and LabVIEW handles the storage
- A LCIO converter function is developed and is tested in Linux environment
  - Not implemented in LabVIEW software as of yet because of windows compiler problems
- The conversion algorithm will be optimized to make readout even faster

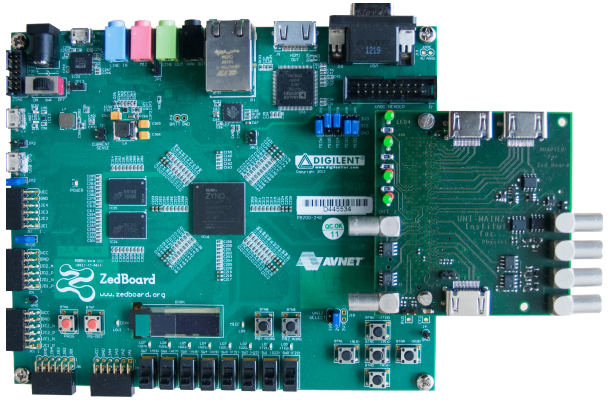


Clock and Control Card (CCC)

- New CCC design by university of Mainz
  - Compatible with CALICE DAQ
- Based on Xilinx Zynq FPGA/SoC
  - Very flexible
  - Powerful on-board processing
  - There are two options
    - ZedBoard
    - MarsBoard



- Ethernet connection to PC for Start/Stop/Readout
- In temporary setup while LDA is being developed
  - 8 layers can be controlled using an 1:8 HDMI fanout
  - Reset/Sync command is sent via an 1:8 LEMO fanout
- Parallel data path thorough HDMI is tested successfully

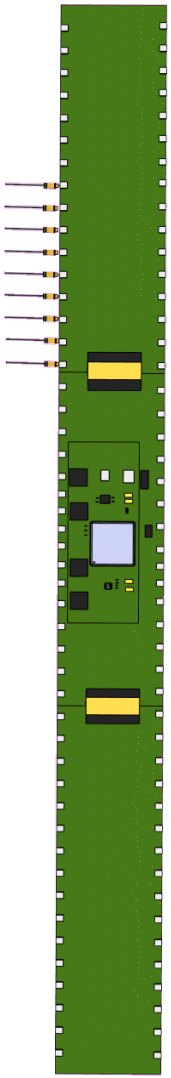


ZedBoard and Mezzanine

DESY

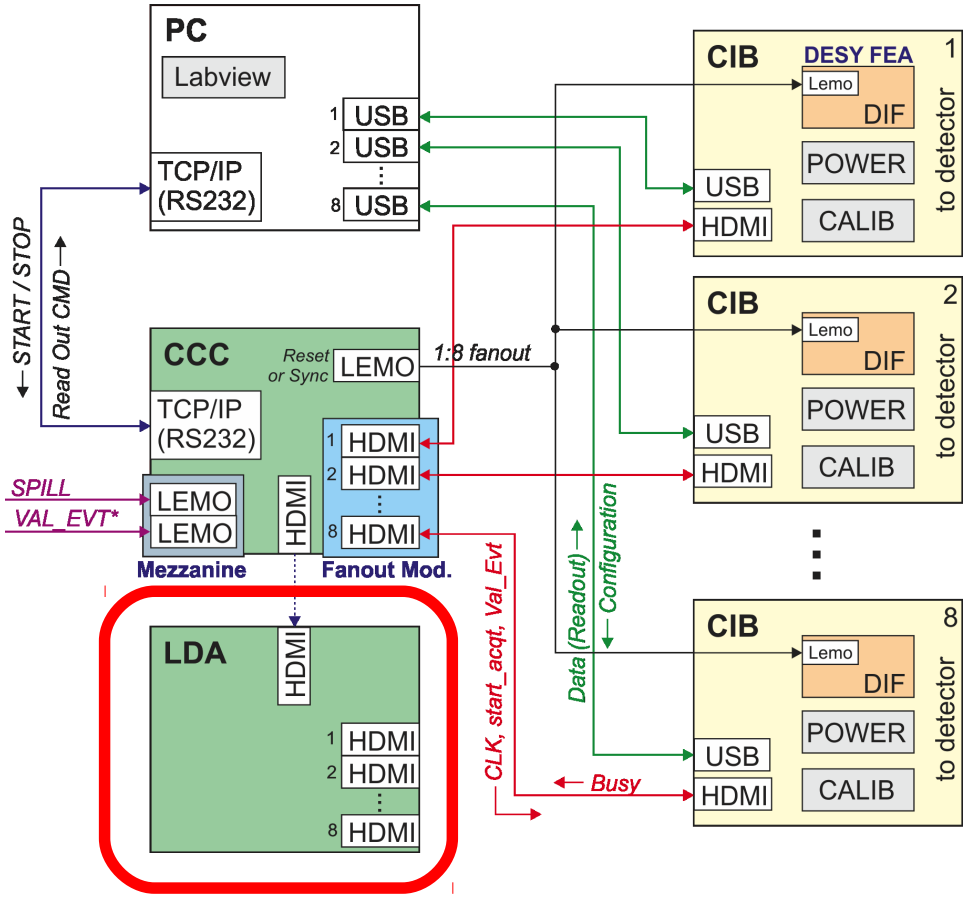
Link and Data Aggregator (LDA)

- New LDA design by university of Mainz
  - Compatible with CALICE DAQ
- Based on Xilinx Zynq FPGA/SoC
  - ZedBoard or MarsBoard
- There are two options
  - Wing LDA → AHCAL geometry specific
  - ZedBoard + Mezzanine → Generic
- Interfaces
  - 1 ethernet connection to PC
  - 1 HDMI connection to CCC
  - XX HDMI connection to DIFs
- To be ready for first evaluations in near future



LDA: A. Welker (Mainz)

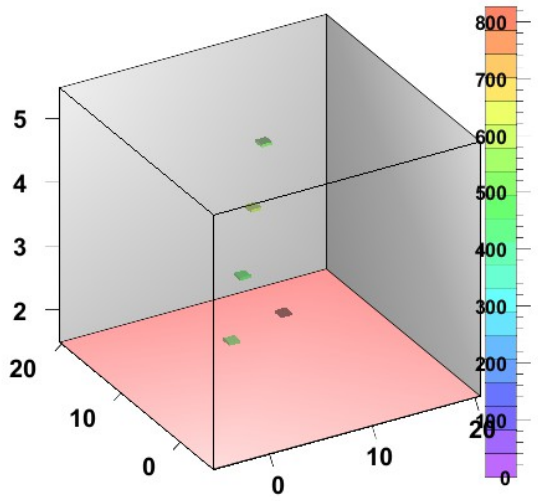
Current status of the DAQ



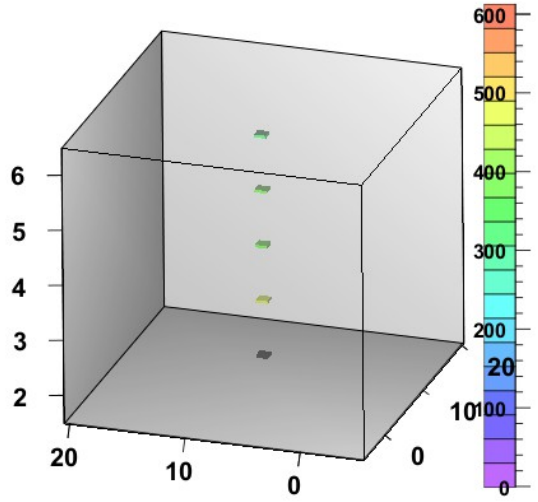
- Software is ready
- CCC is in operation
- Ready for next step to incorporate LDA

Performance of the DAQ system

- Current version of the DAQ tested in different setups
  - Lab Setup
  - Cosmic Muon run
  - Test beams
- Fully functional parallel data readout
- Very stable operation
  - 72+ hours run
- Faster than ever
  - ~9 Hz readout frequency
  - ~150 Hz sustained trigger rate
- Now we were ready to test
  - Specific power-on procedure
  - Detector synchronicity



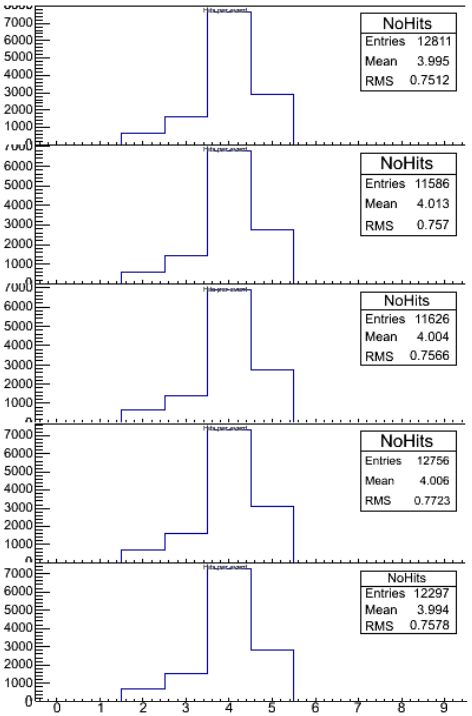
A cosmic Muon track in 4 layers



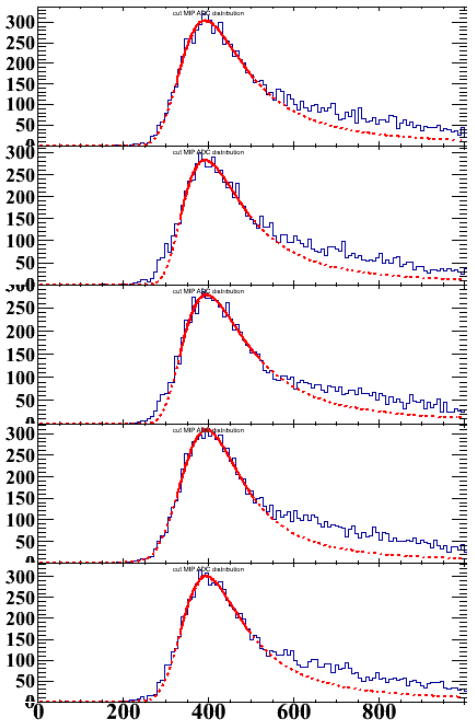
A track in 5 layers at test beam

Specific power-on procedure

- We had a week of DESY test beam in July
- Non-reproducible state after power cycling problem is solved:
  - Switching on power- and signal lines to the SPIROC in a fixed specific order
- This solution was tested in several runs with power cycles in between



Number of Hits

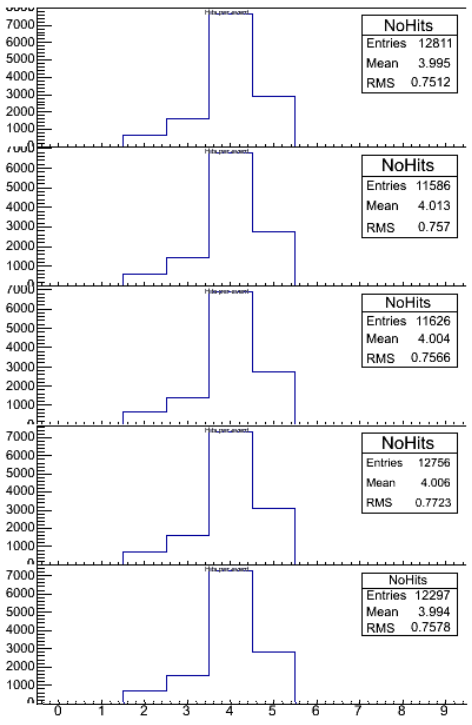


ADC Counts

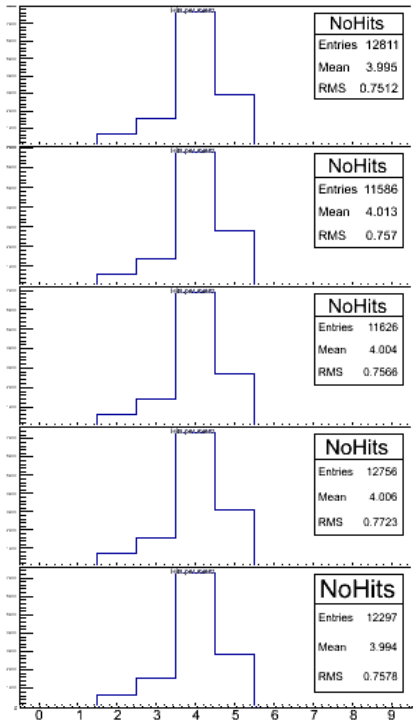
- After applying power-on procedure, MIP position and hit multiplicities/efficiencies seem to be stable

Multilayer Synchronicity

- During July test beam we tested synchronicity
- For the same run, number of hits was checked in two different event builders
  - Accepting only the same bunch crossing IDs
  - Accepting bunch crossing IDs +/- 1
- Absolutely no difference is observed



Same BunchX ID

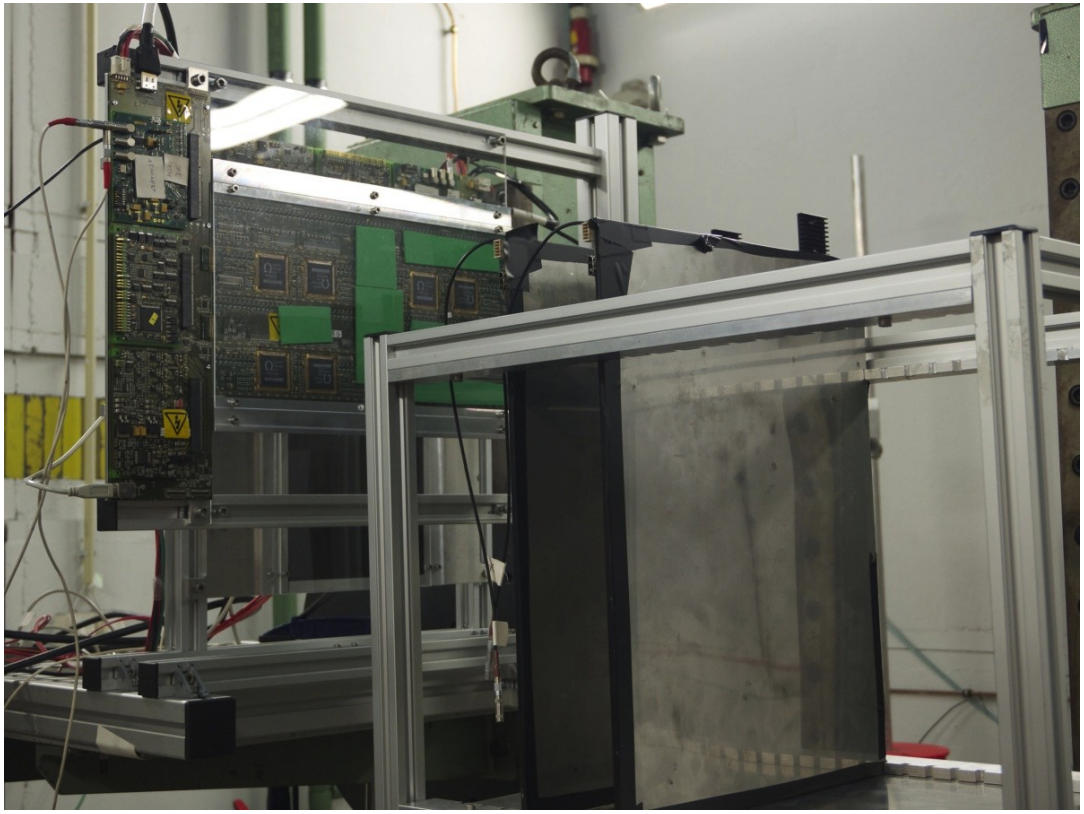


BunchX ID +/- 1

- We have a true synchronous detector 

Compatibility with other detectors

- Beginning of July ScECAL was at DESY 21 test beam
- We had joint runs with 2 HBUs and 2 EBUs
- New multilayer DAQ was used to operate all 4 layers together



- In principle the new multilayer DAQ can be used by other detectors

Summary and outlook

- We have completed the first stage of AHCAL multilayer DAQ
- The multilayer DAQ system is tested
  - It is compatible with CALICE DAQ
  - It is stable
  - It is fast
  - It is synchronous
  - It can be used by other detectors

Outlook

- Ready for the next stage and to incorporate LDA
- Full HDMI readout to be implemented