SiW ECAL Technological Prototype
Long slab and FEV_COB

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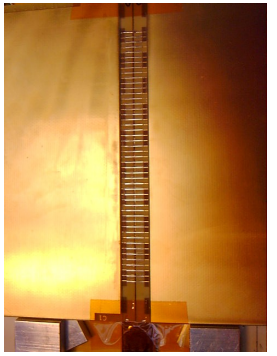
2010 BLANC 0429 01

SiEcal detector layer principle

A layer is composed of several short ASUs:

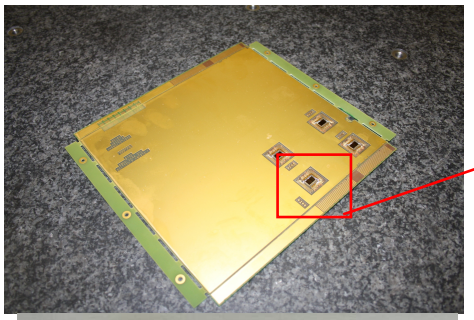
- A.S.U. : Active Sensors Units



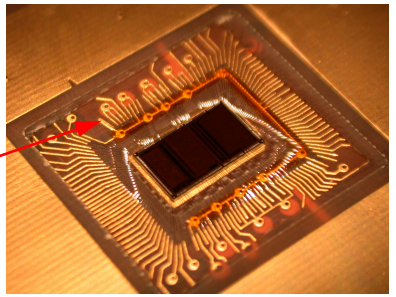
Interconnection work (see later)

Dedicated mechanical 'scaffolding' will be constructed

Chip+PCB+SiWafer =ASU



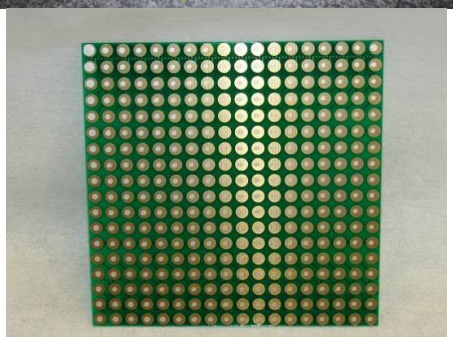
Bonding realised by CERN



Chip embedded

PCB is glued onto SiWafers

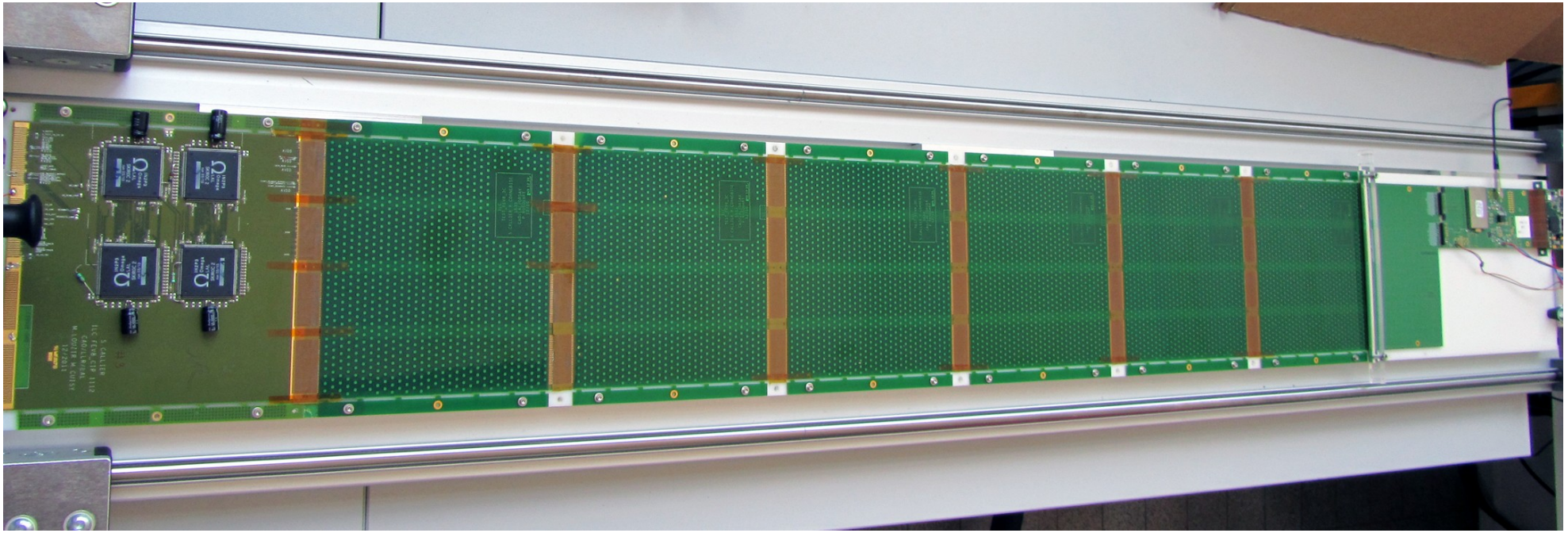
Gluing robot about to be commissioned



Length of layer:

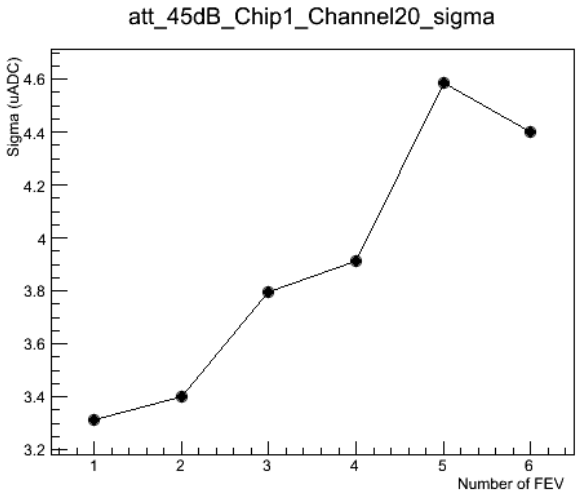
1.5m for barrel
2.5m for endcaps

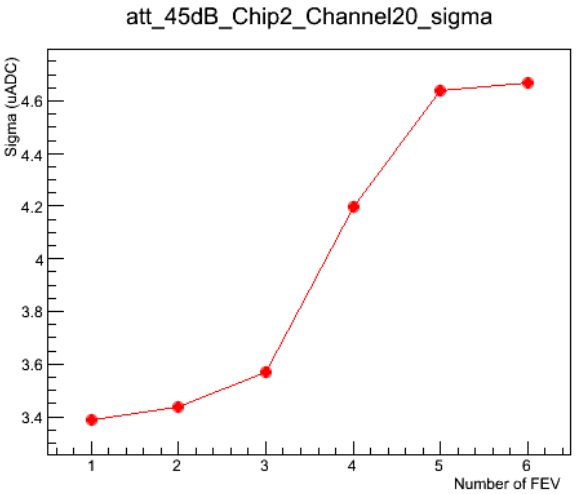
Long Slab

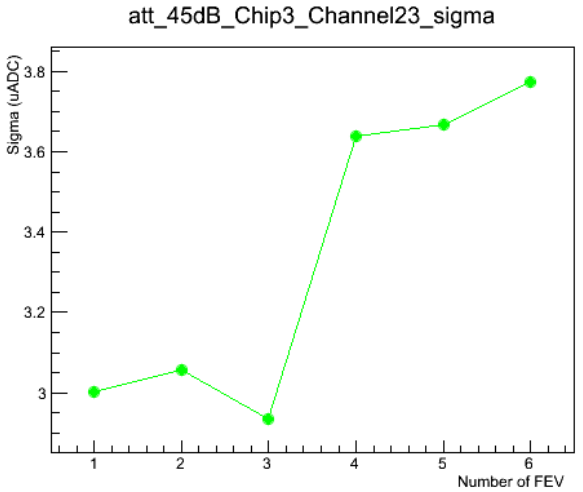


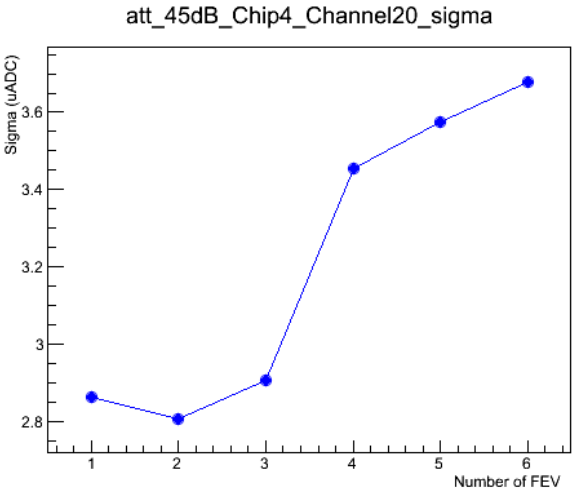
Injection

No stub
Response as a function of number of FEV = RMS of signal increases with nFEV
Big step T° effect (see next slide)

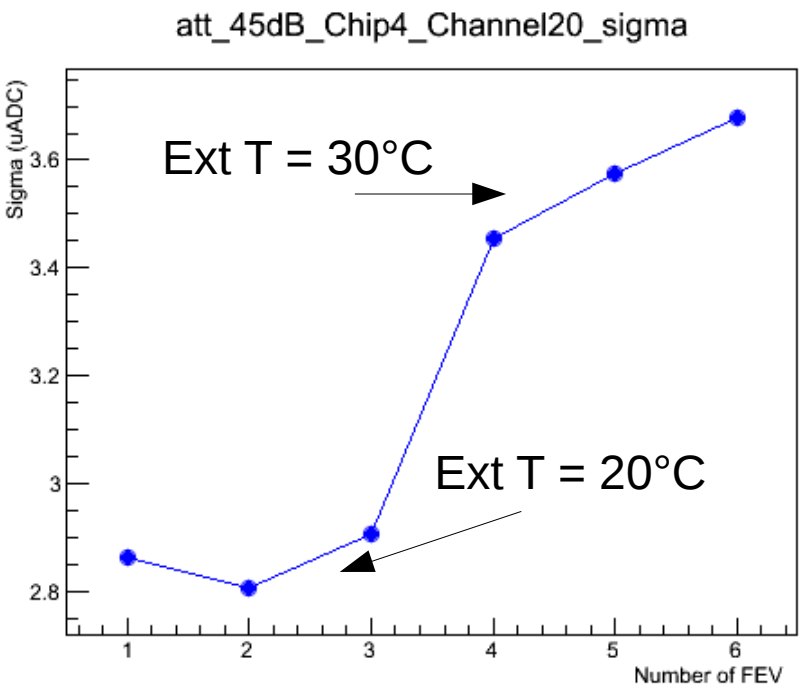


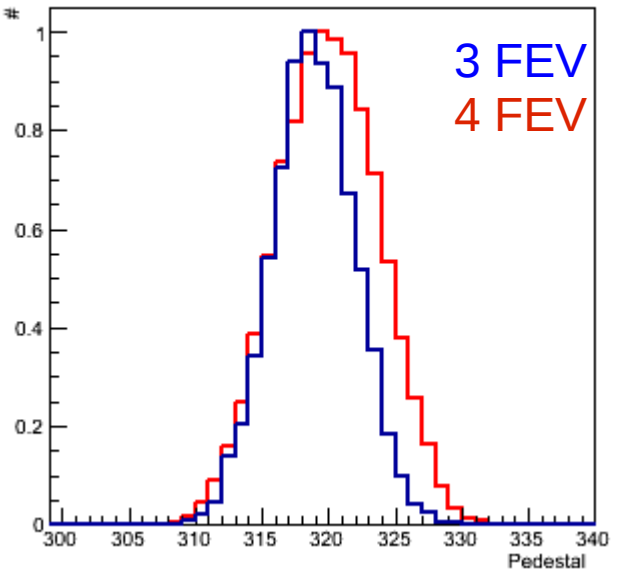


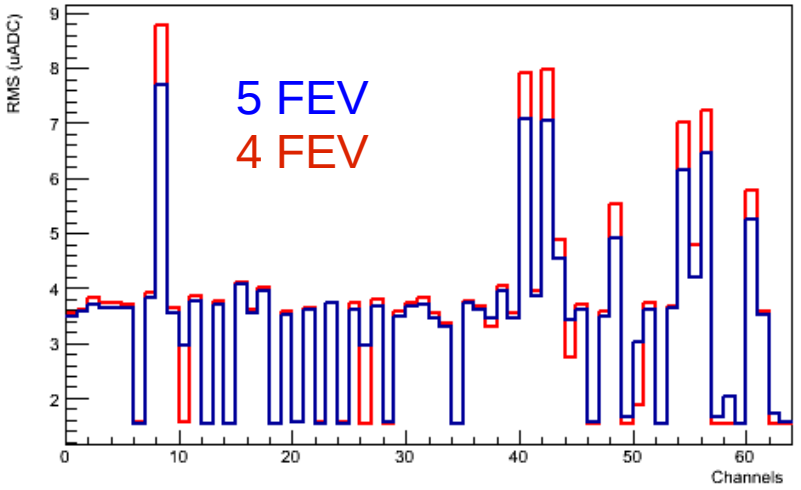


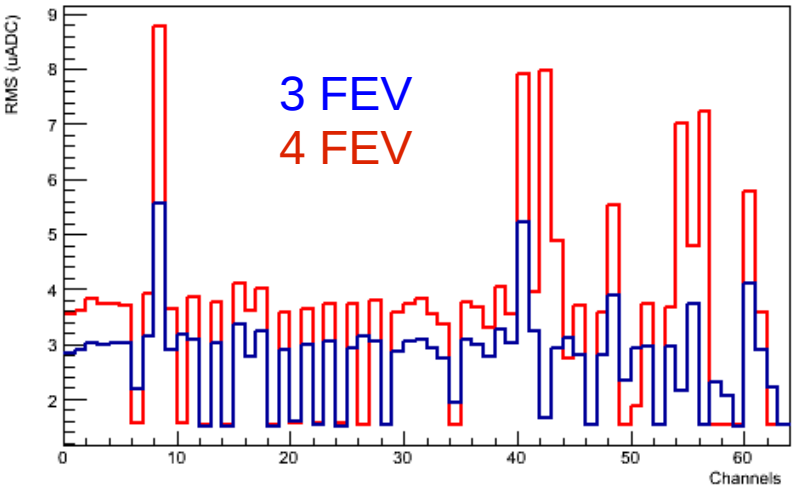


Noise (as a function of ext T°)

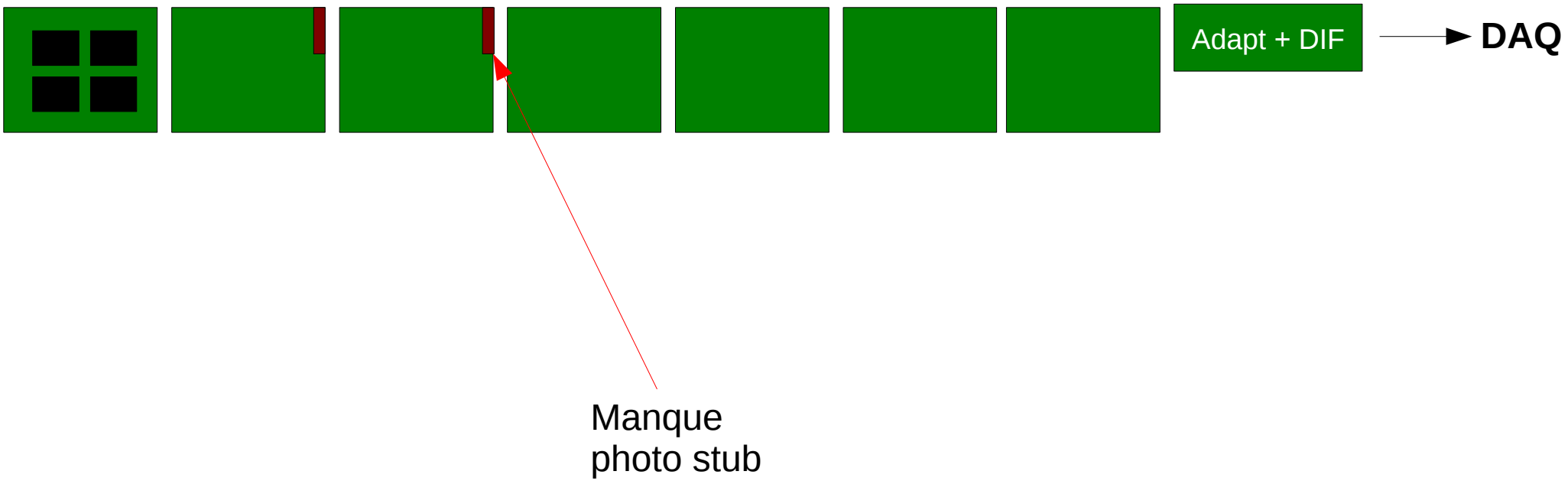




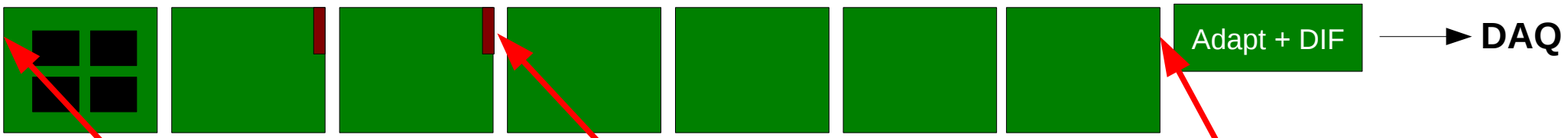




Long Slab + Stubs

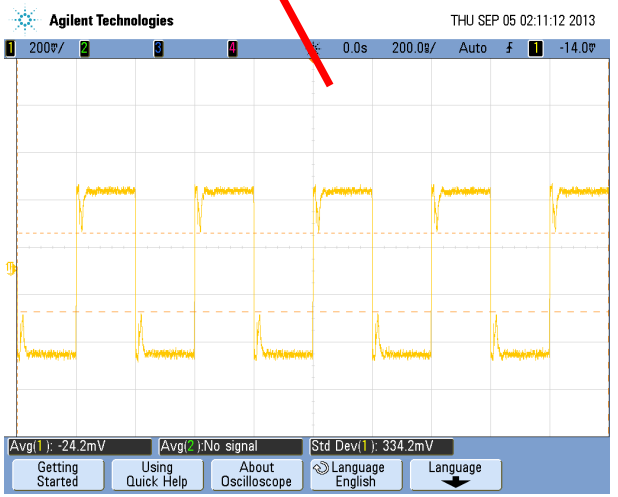


Clock 5 MHz



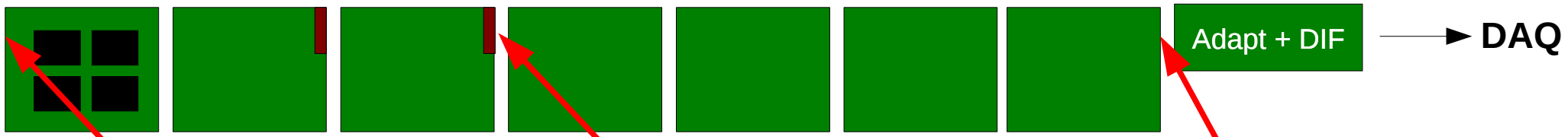
V = 640 mV

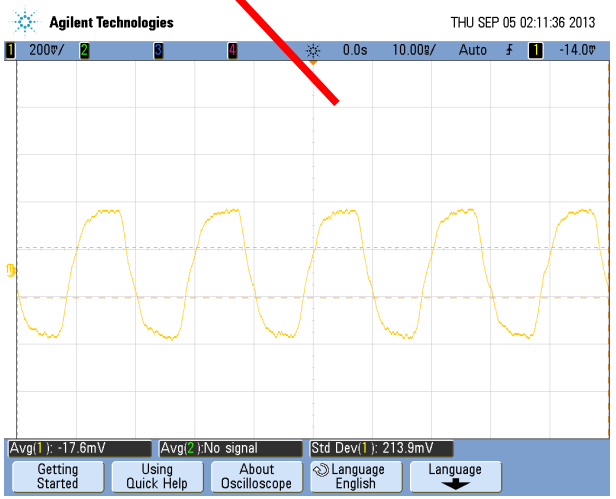
V = 660 mV



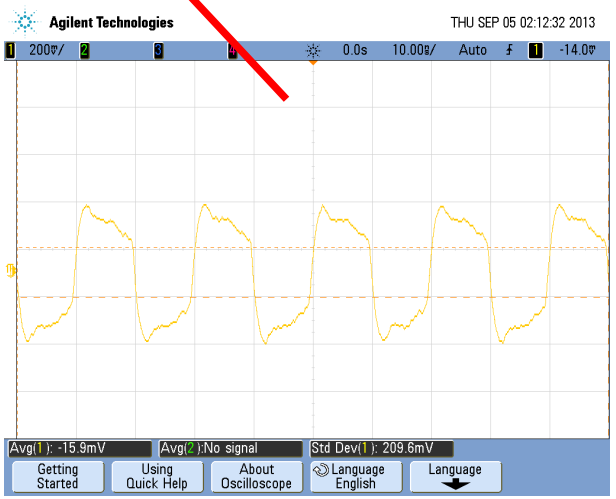
V = 700 mV

Clock 40 MHz

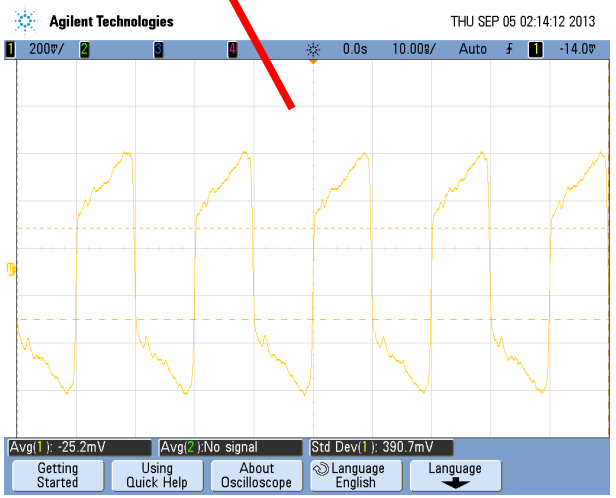




V = 500 mV

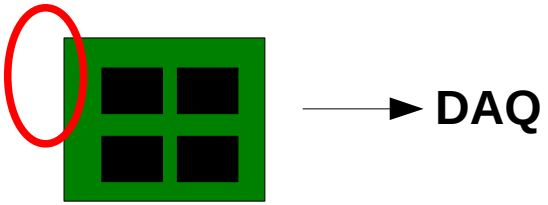


V = 600 mV



V = 800 mV

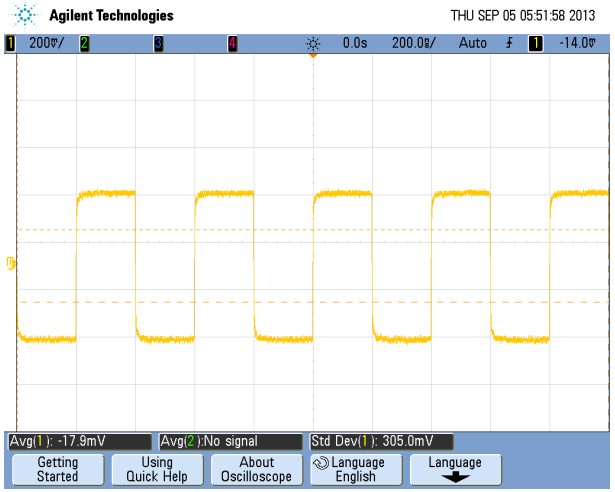
Short / long slab

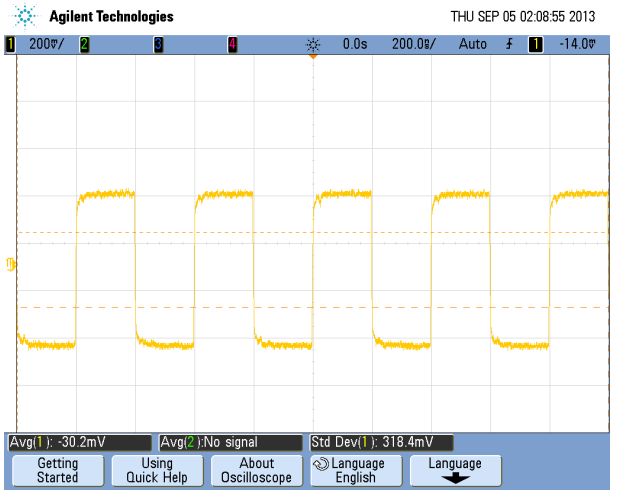


Short slab

Long slab

40 MHz clock

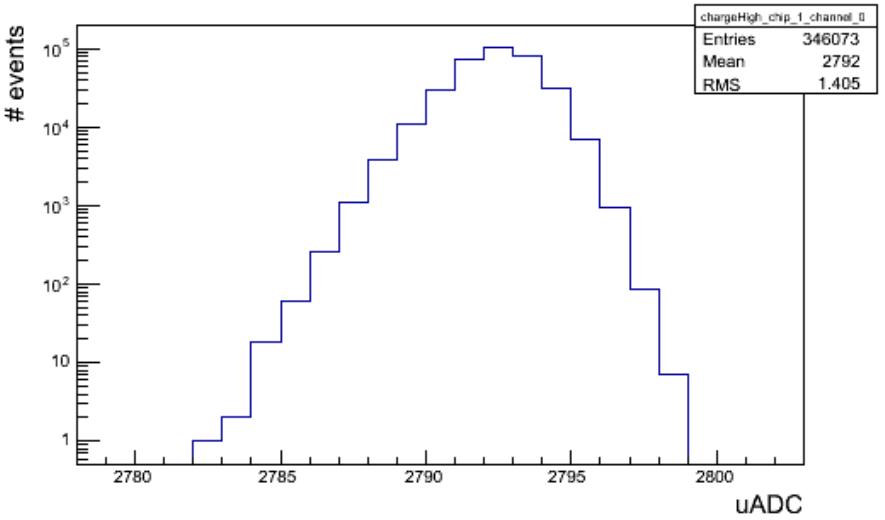


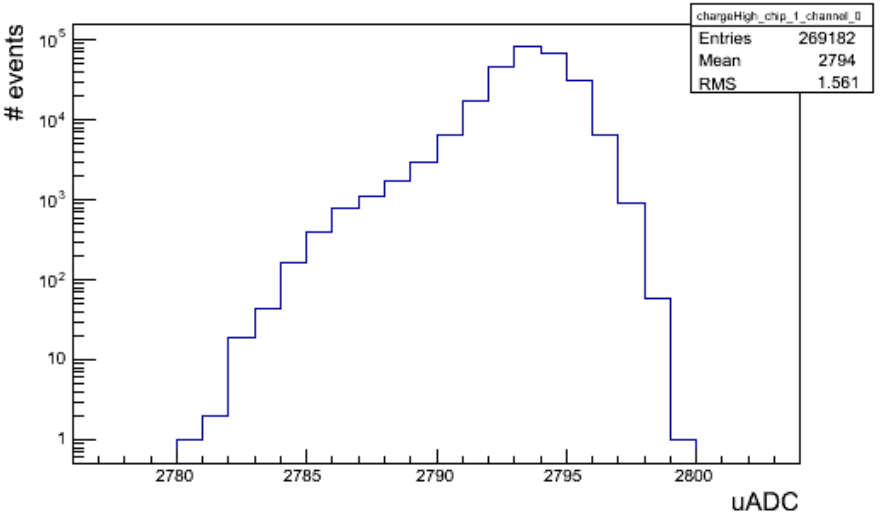


5 MHz clock

Clock 40 MHz

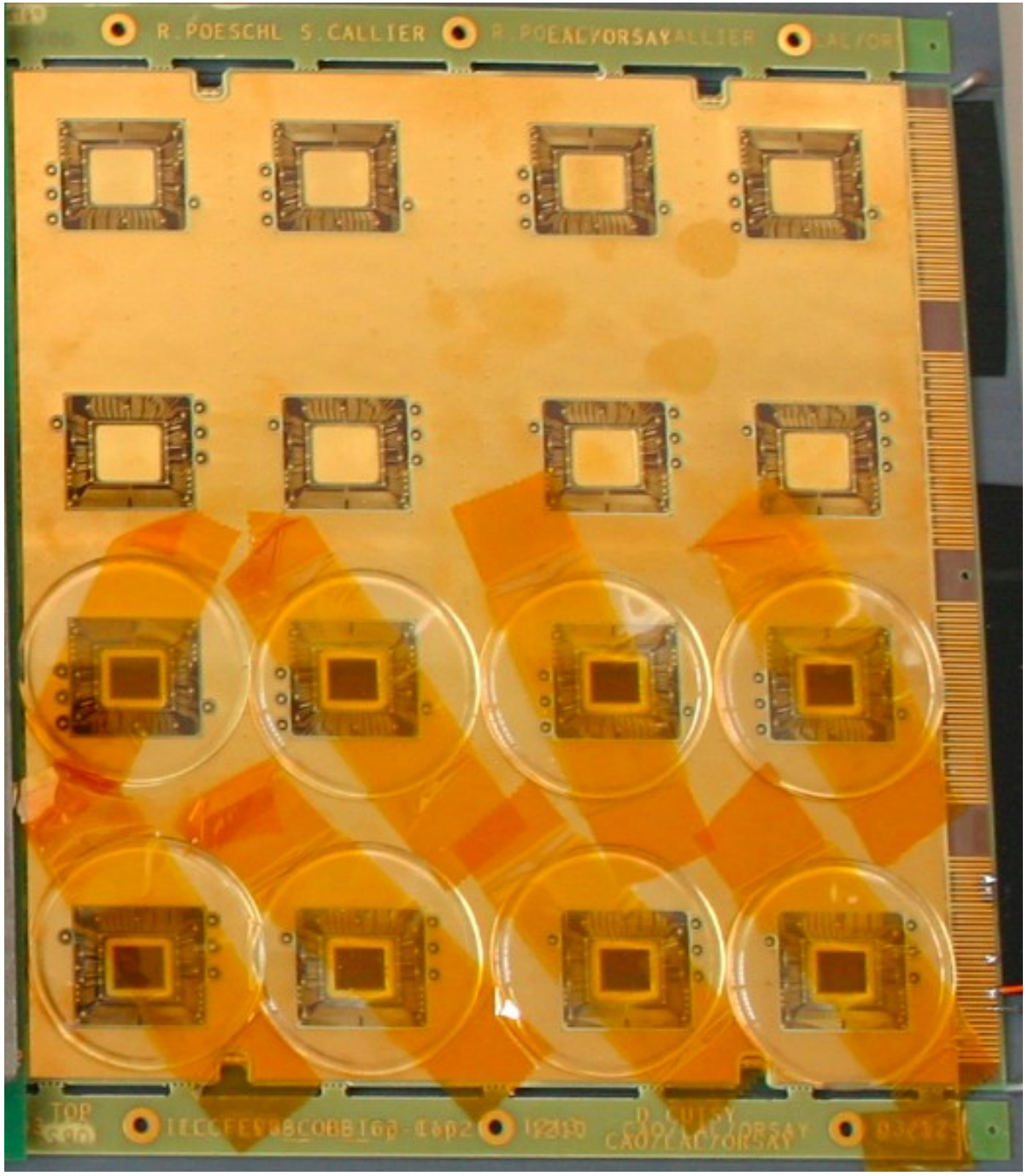
Comparison 1 stub – 2 stubs
Clock 40 MHz : TEST_ADC input -> continuous voltage (Wilkinson : clock used for the ramp)





RMS increases with 2 stubs (bump on the left part of the Gaussian)
==> lost pulse of 40 MHz clock ?

Studies with FEV8_COB



- Interface board with Chip On Board
  - SiW Ecal and ILD baseline design
  - Assures compact calorimeter

- Not trivial specs

  Ultrathin : 9 layers with thickness of about 1.2mm
  Deviation of total planarity of about 0.5 mm (3mm is industrial standard)

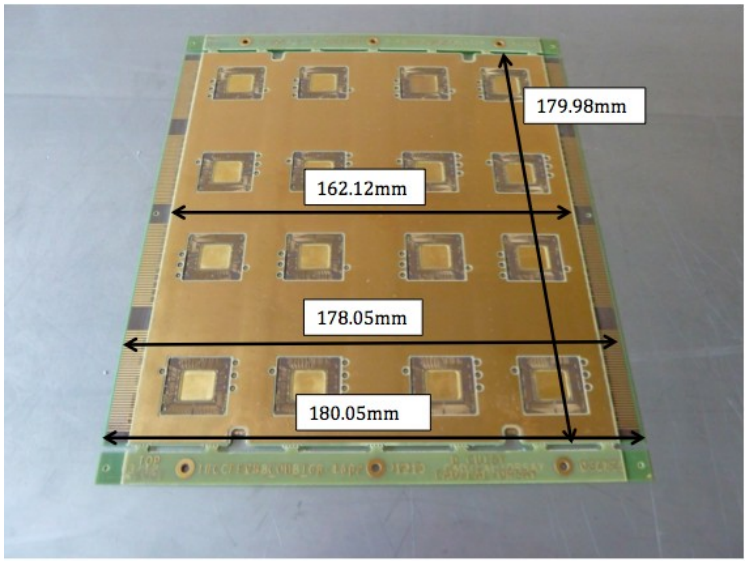
However it's now there in a first version

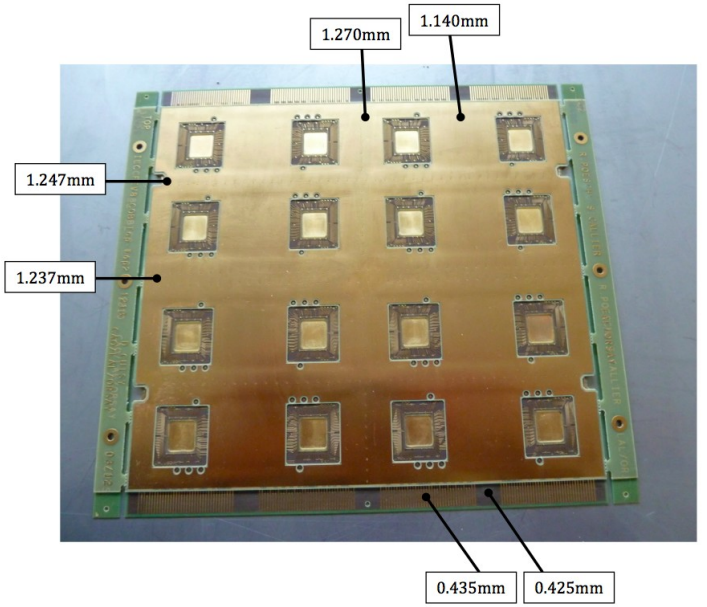
- Design and routing OMEGA/LAL
- Fabrication end of 2012
- Metrology at LAL
- Chips mounted beginning of 2013 by CERN bonding lab

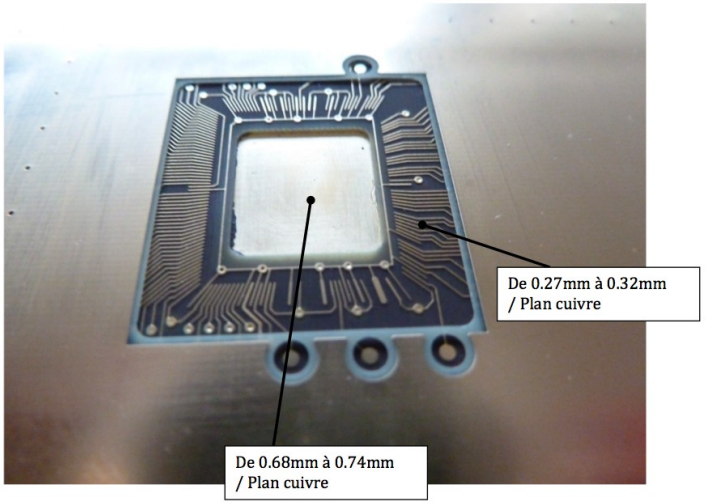
  Personal Intermezzo : I appreciate a lot the Support by the CERN bonding lab !

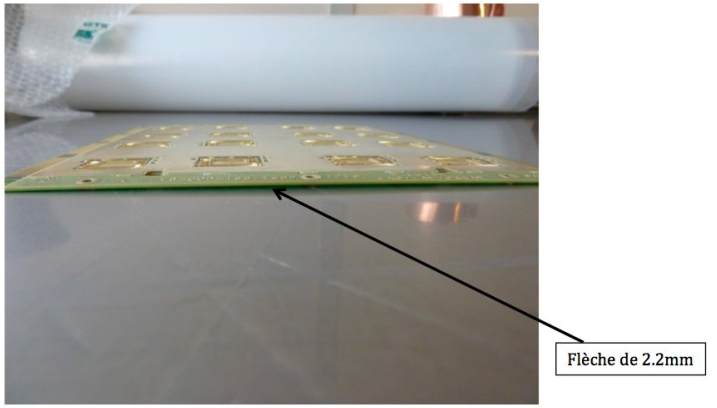
- First tests in summer 2013 at LAL

FEV8_COB – Metrology





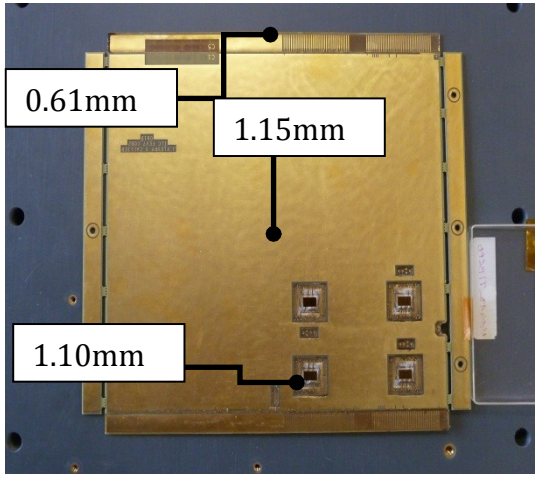


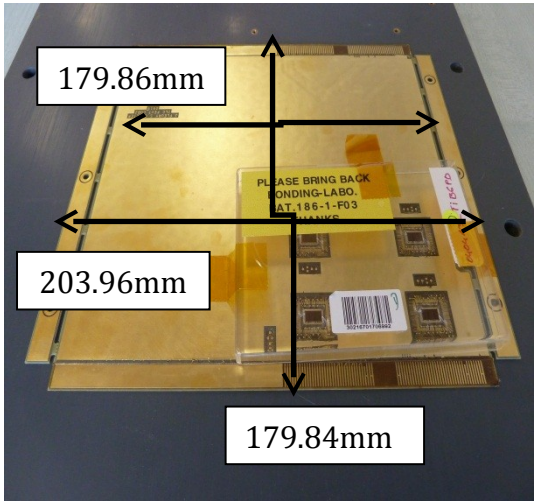


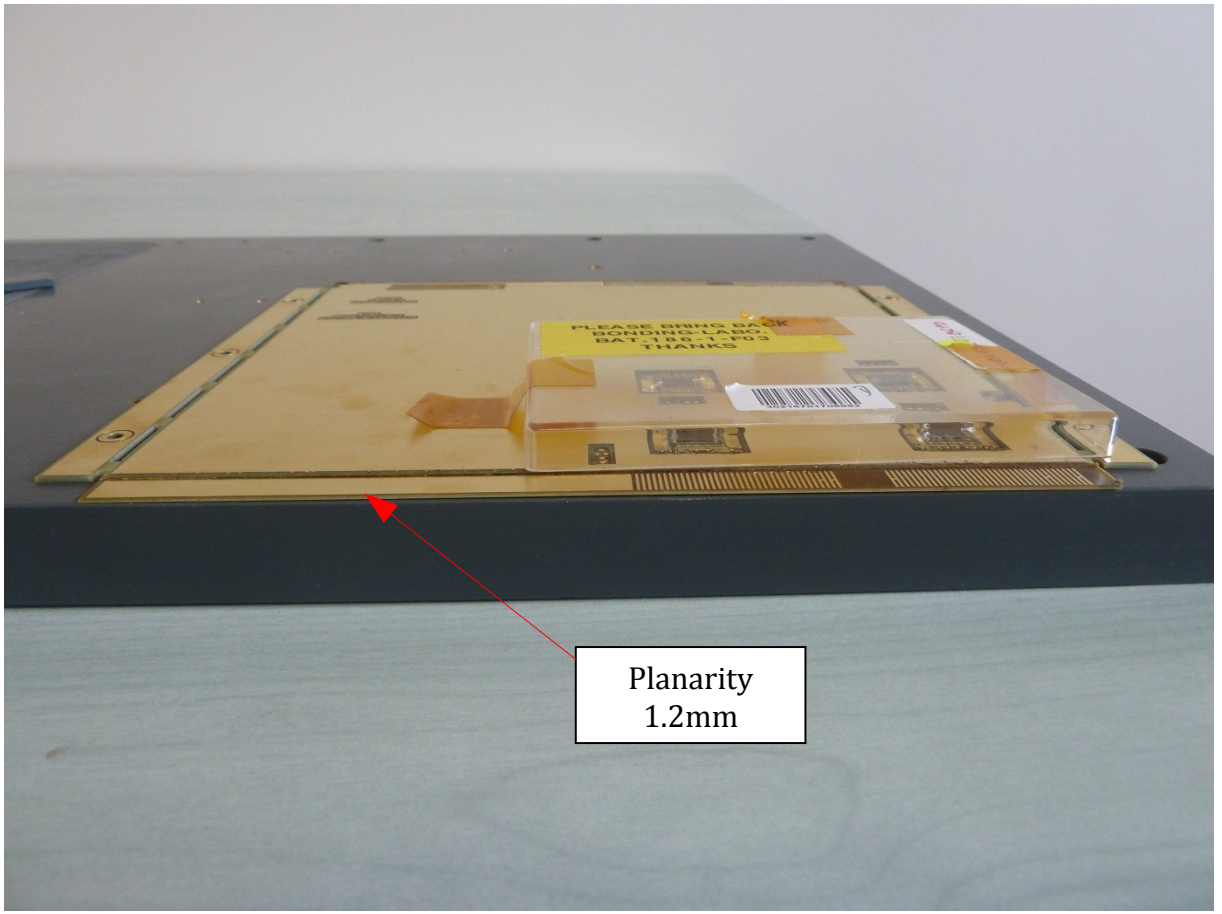
Mechanically tolerances are not met for this board
Also problems with arrangements of bonding pads → Can/will be solved

FEV7_COB – Test production at EOS company

… under supervision of SKKU at Suwon



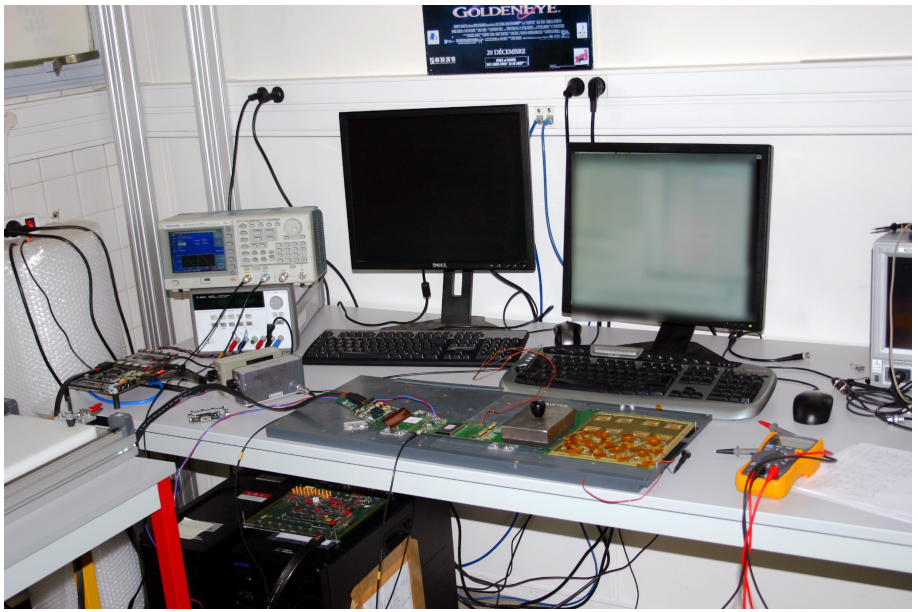


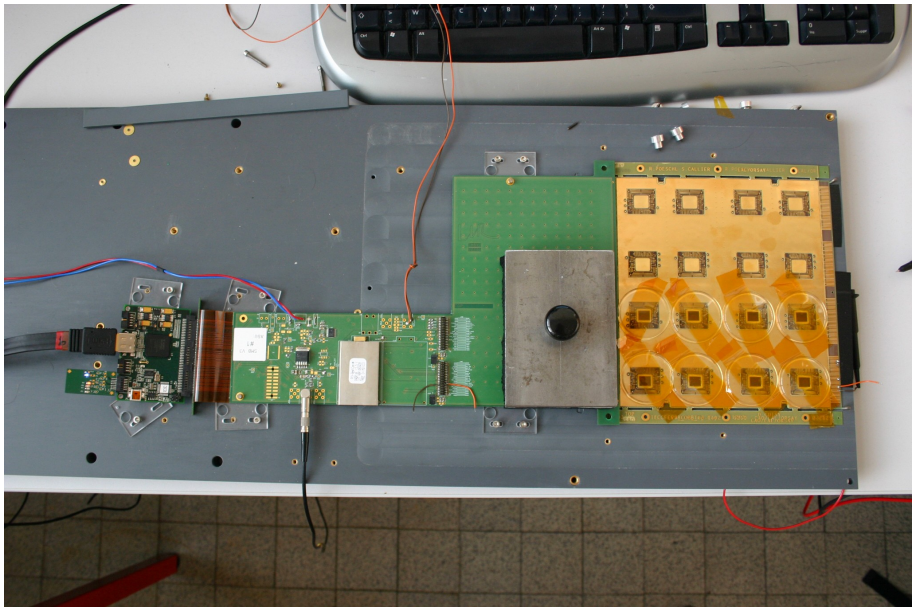


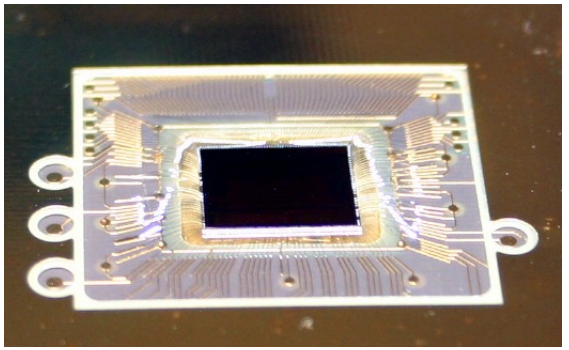
- Very promising from mechanical point of view
  However issues with gluing of wafers
- Could not be tested since it came somewhat late
- Will pick up contact this autumn to arrange FEV8_COB production with SKKU/EOS

Setup at LAL

... to establish first communication with FEV8_COB



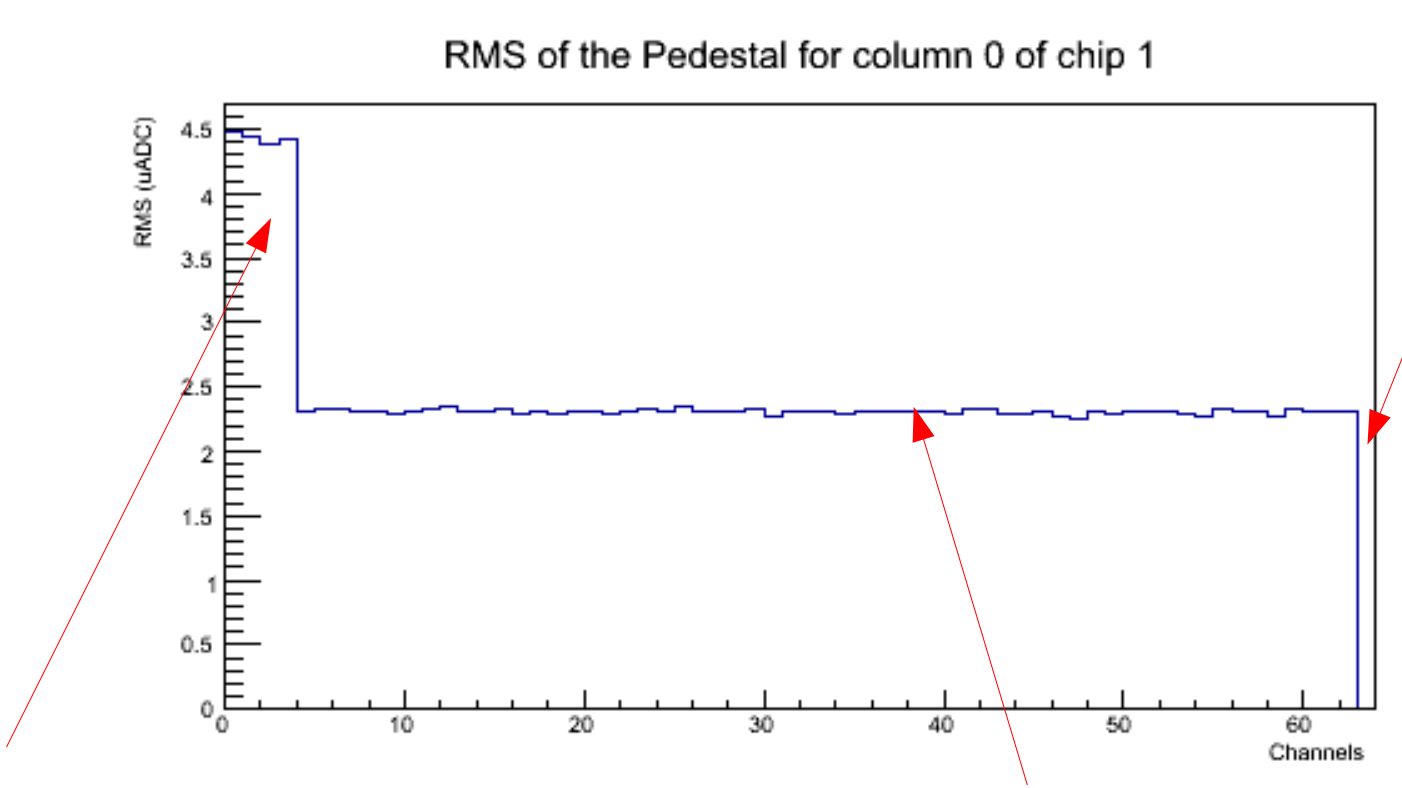




Slow control tests with one ASIC

Study with only one ASIC, all switched on but all but one masked

Channel 63 to trigger ASICs → noise in other channels



Trigger channel

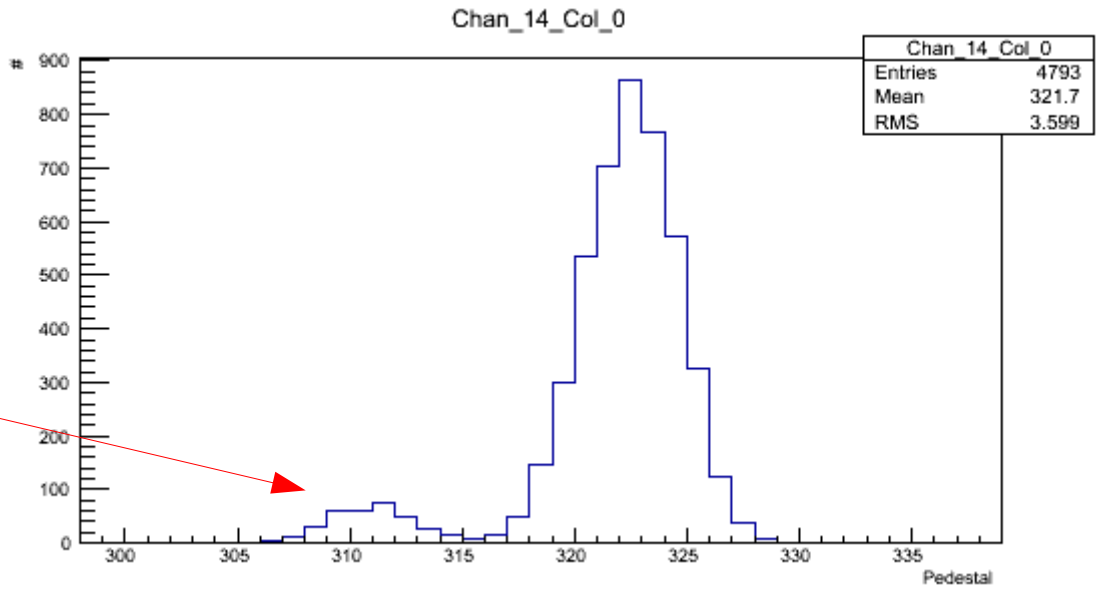
Channels with disable preAmps.
Pedestal distributrion with multi-peaks → already seen in FEV8 CIP

Nice flat distribution → good routing in PCB
(In TB with FEV8_CIP, noise ~ 2 uADC)

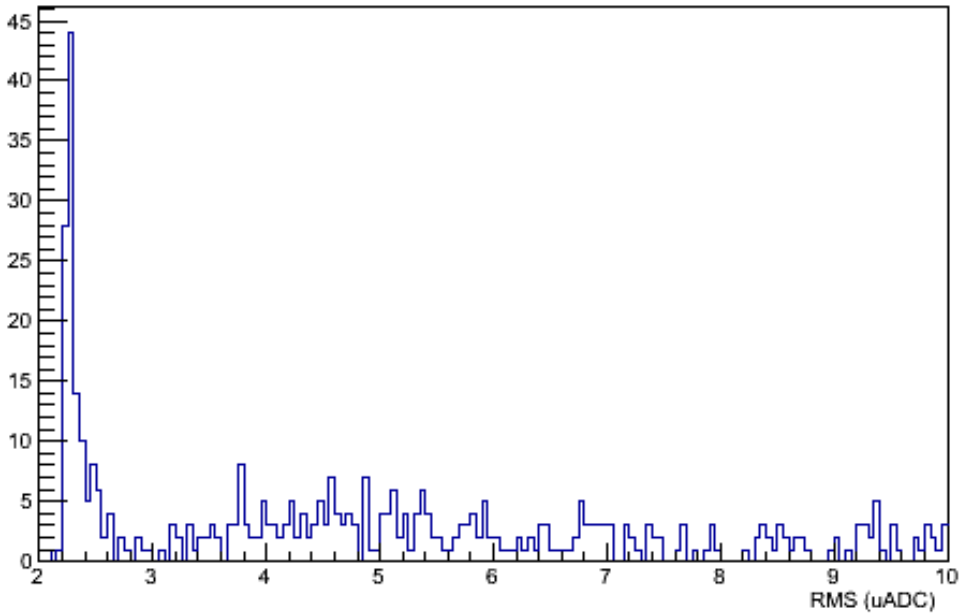
Chip react correctly on change of slow control parameter
Quality of results to be taken with care

Noise measurement with several ASICs (to be studied)

Multi peaks
→ plane events which pass cut?
→ too low threshold ?
→ another effect?



Lots of channels with hits
(Injection on 30 channels per chip, 8 chips)
→ Multi peaks → large RMS



Summary and outlook

- Studies towards realistic Ecal ASUs and layers
  Simplified long layers
  First board for 16 ASICs with SiEcal baseline design

- Studies with stubs reveal some distortion of clock

- Noise rms increase with
  … increasing number of ASUs
  … increasing temperature (side observation in hot summer. Not related to number of ASUs

- FEV8_COB for 16 ASICs
  - out of mechanical tolerances
  - Korean FEV7_COB gives good hope that this issue can be overcome
  - Examination for gluing revealed further shortcomings, however no show stopper

- FEV8_COB initially equipped with 8 ASICs
  First studies prove that we can communicate with **all** eight ASICs on the board
  Understanding of spectra needs to be scrutinised ...
  before gluing of Si wafers and extending to 16 ASICs

- Prepare production of new series of FEV8_COB boards in Korea