Test beam results of small resistive Micromegas prototypes

CALICE Collaboration Meeting
September 09-11th 2013
LAPP, Annecy-le-Vieux

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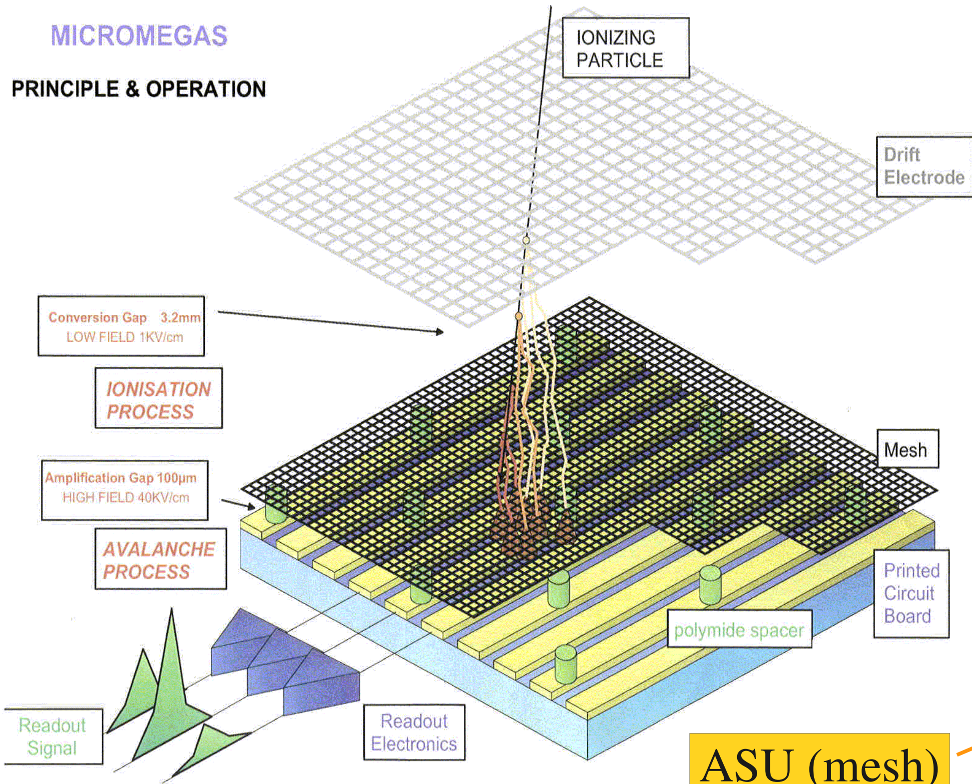
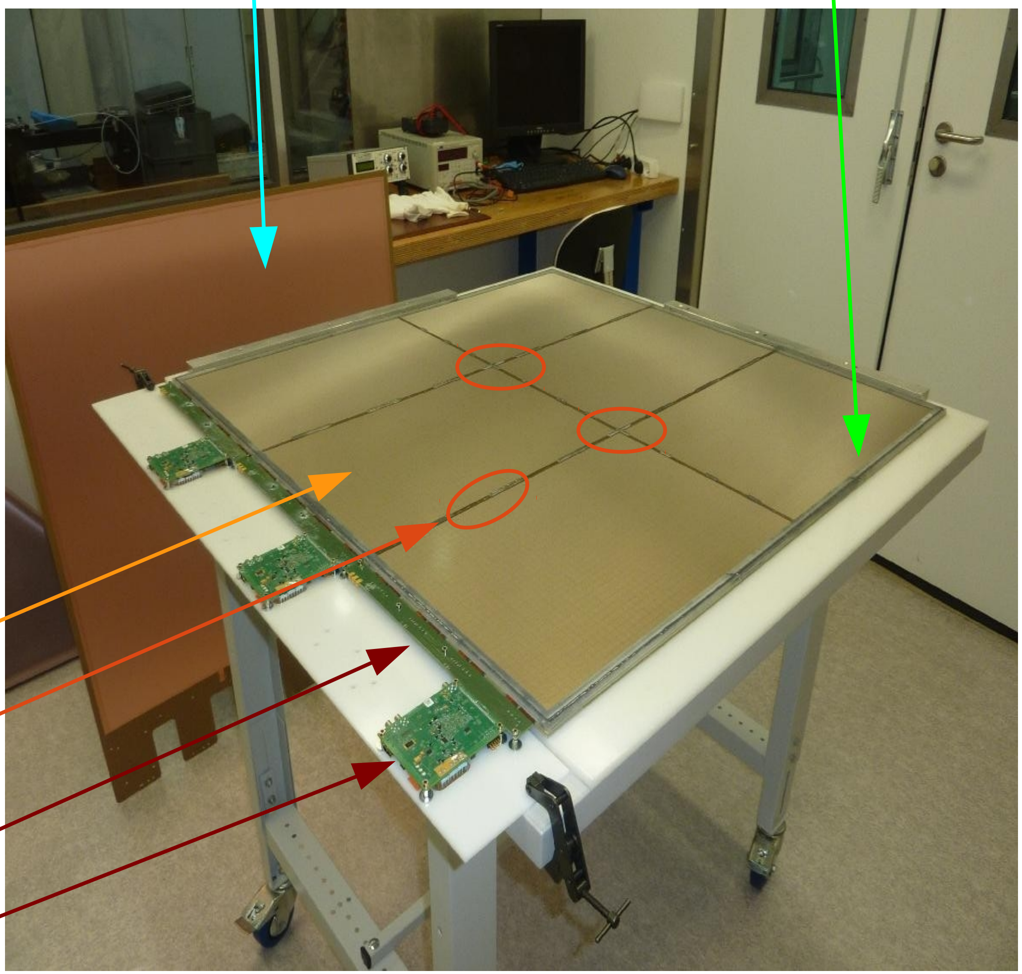
Principle of Micromegas detector



Cathode

Frame with 2 gas pipes (Ar/CO_2)



ASU (mesh)

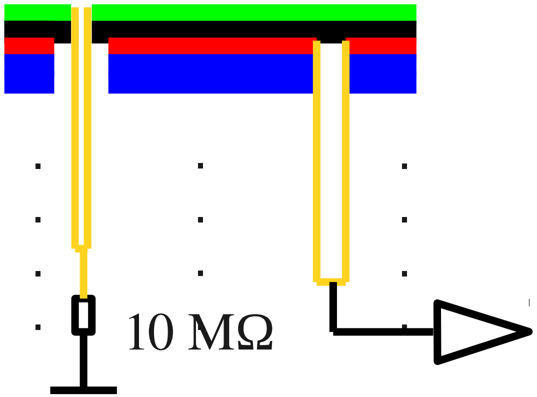
spacers

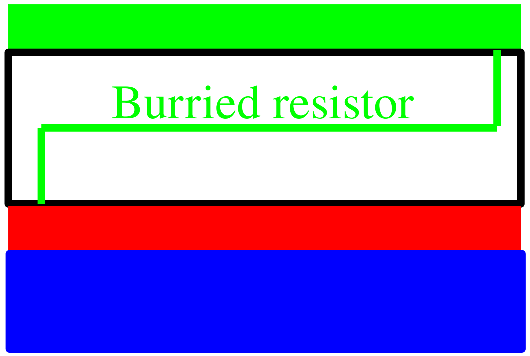
R/O cards (DIF+interDIF)
ASIC LV & mesh HV

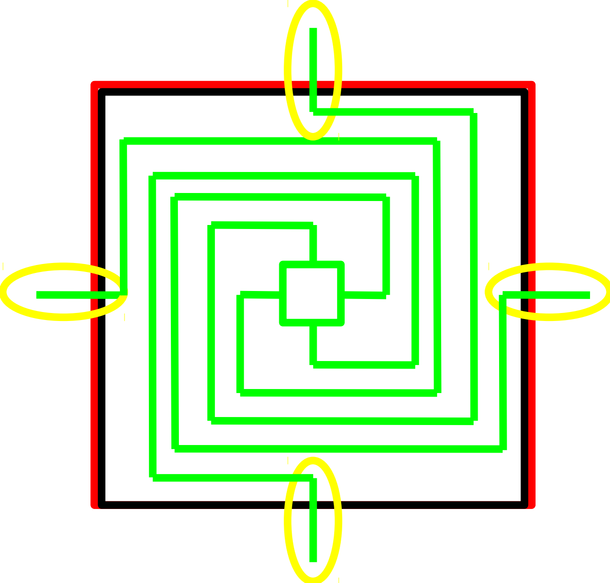
Micromegas → good performances (efficiency, rate capabilities, energy and position resolution)
→ but spark sensitive → introduction of resistive layers

Resistive Micromegas detectors

Beam test goals : Compare performances of 16×16 cm^2 standards and resistive Micromegas (efficiency, multiplicity, rate capabilities, spark rate, threshold...)
Resistive Micromegas : 3 configurations tested







Resistive vias configuration (independent pad)

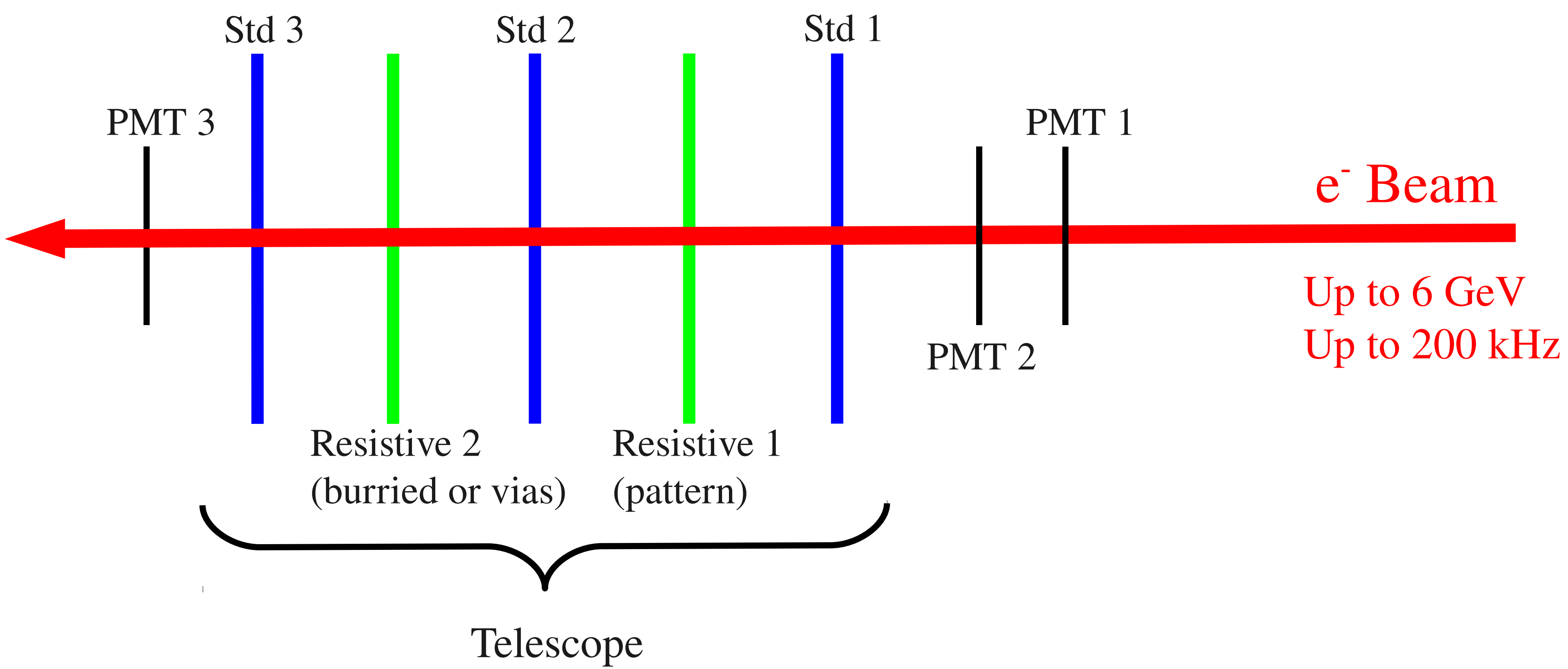
Burried resistors configuration (independent pad)

Resistive lines configuration (connected pads)

Resistive Micromegas : good sparks protection, simpler and cheaper PCB (than with diodes) but rate limitation (charge evacuation)

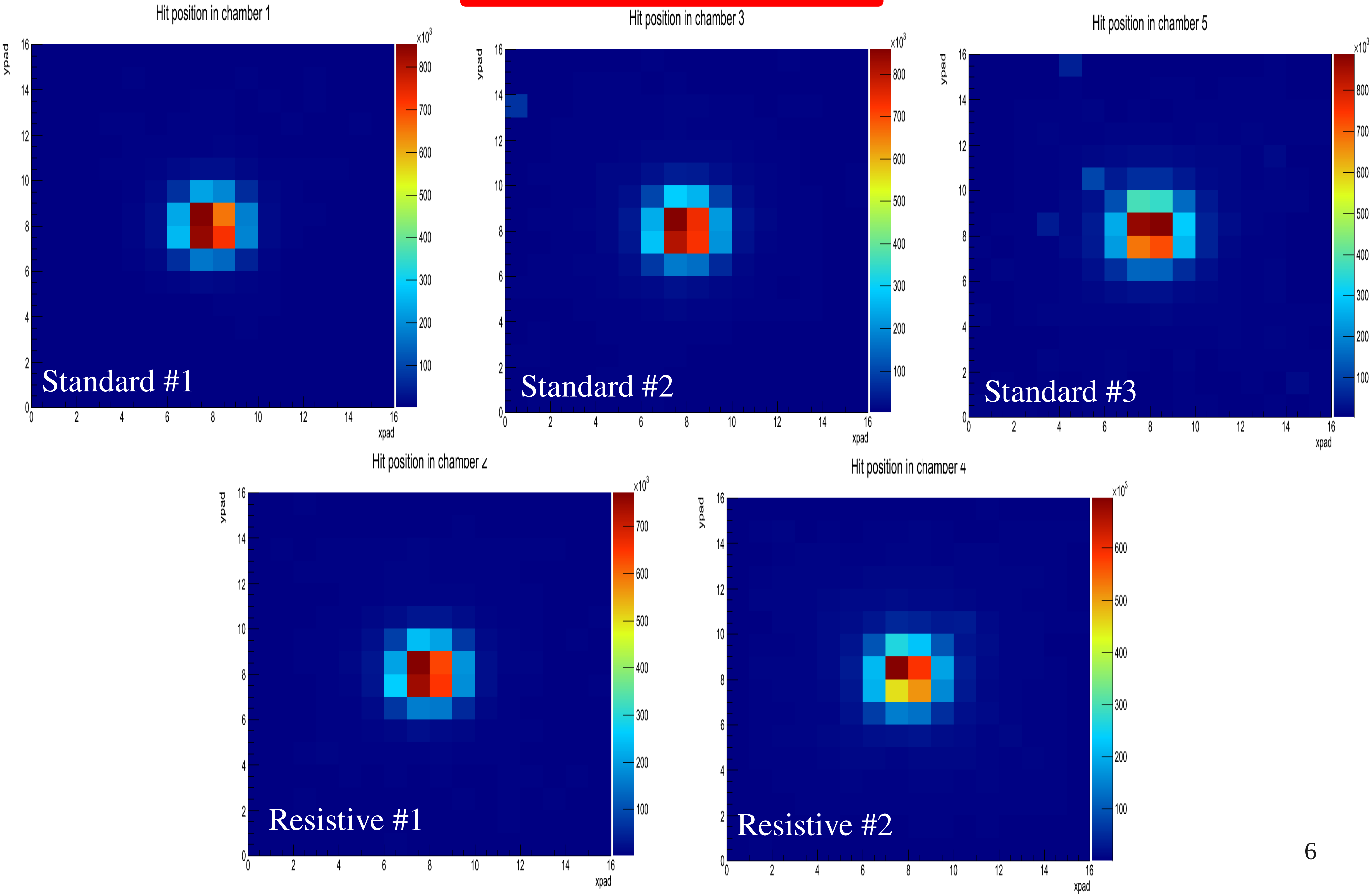
Test beam setup

<u>Setup</u> :
3 standards & 3 resistive chambers
Ar/CO_2 gas mixture
Intermediate CALICE DAQ system
Software : LAPP based (Labview, C++ framework)



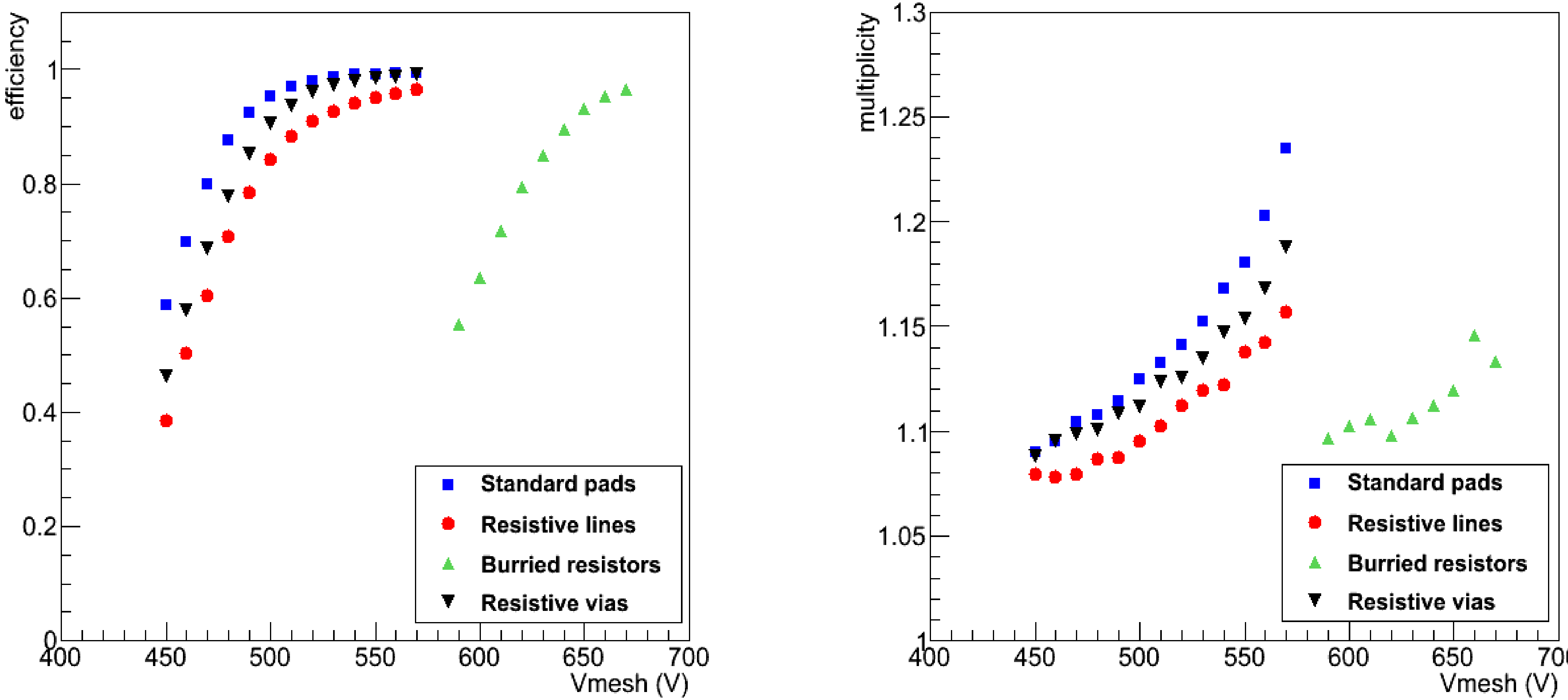
Test beam setup

Beam profile



Good news → chambers worked @ first beam !!!

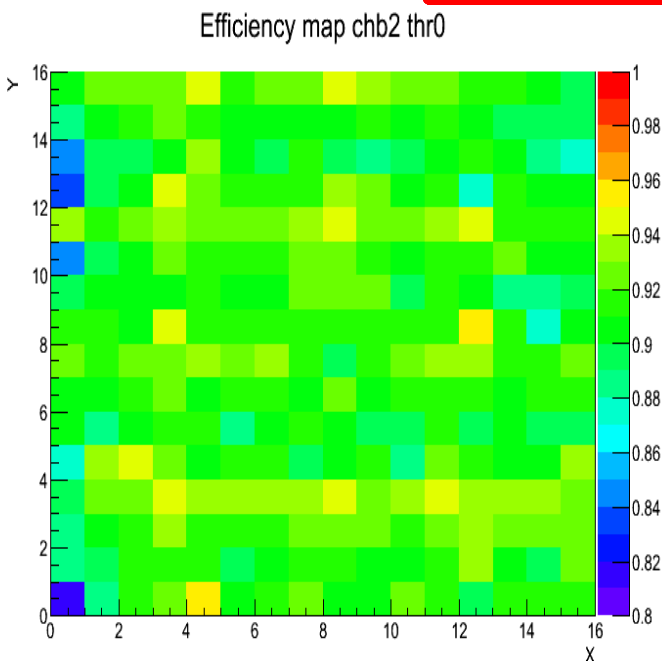
Efficiency and multiplicity vs HV mesh



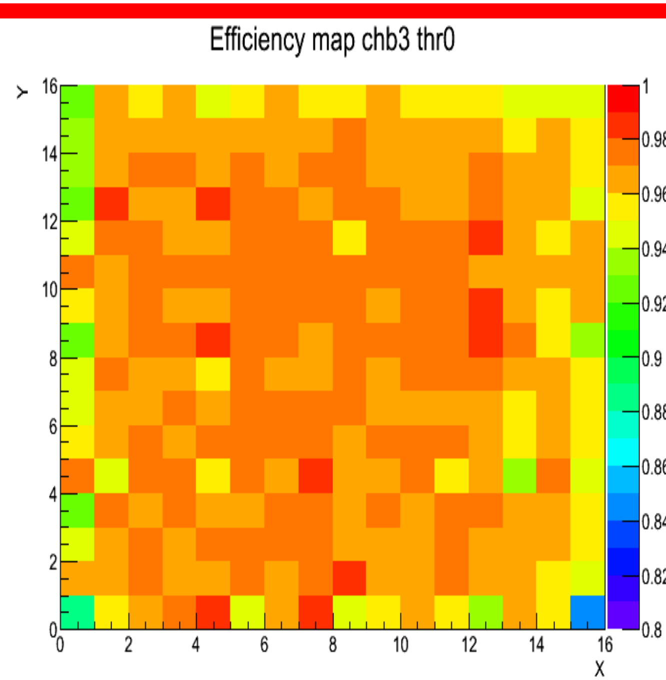
Efficiency ≥ 95 % and multiplicity contains 1.03 ≤ mult ≤ 1.25 pad for all chambers

Chamber with burried resistors needs 100 V more than the others ⇒ problem in the construction (no contact or bad contacts between resistive layer and R/O pad)

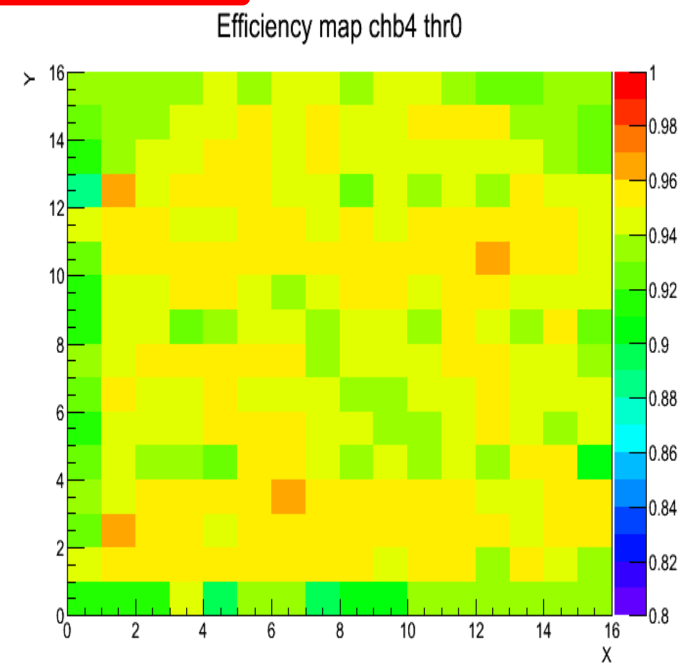
Uniformity of the response



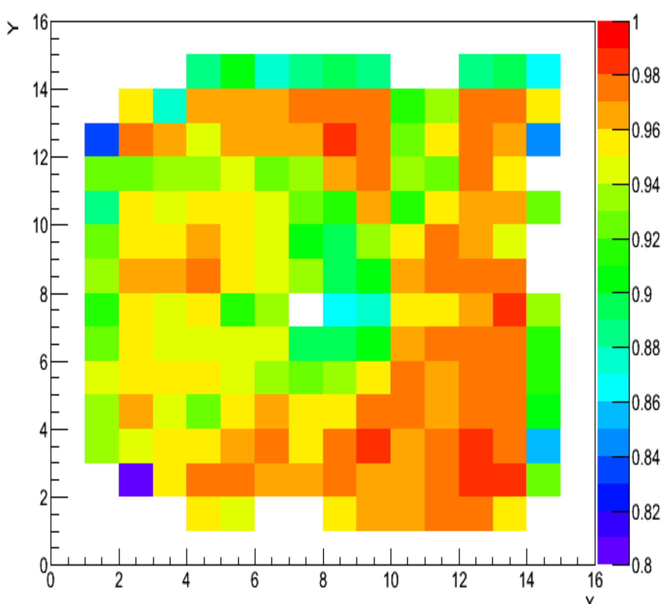
Resistive lines



Standard



Resistive vias

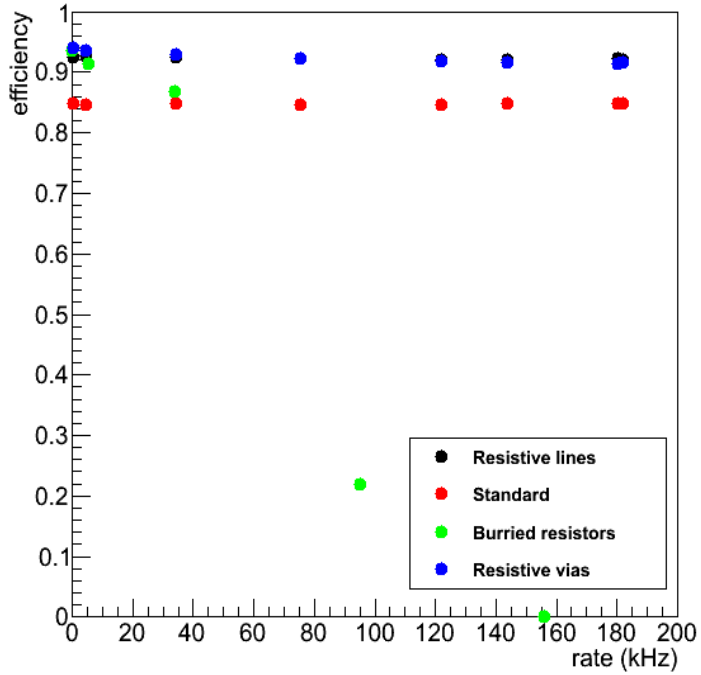


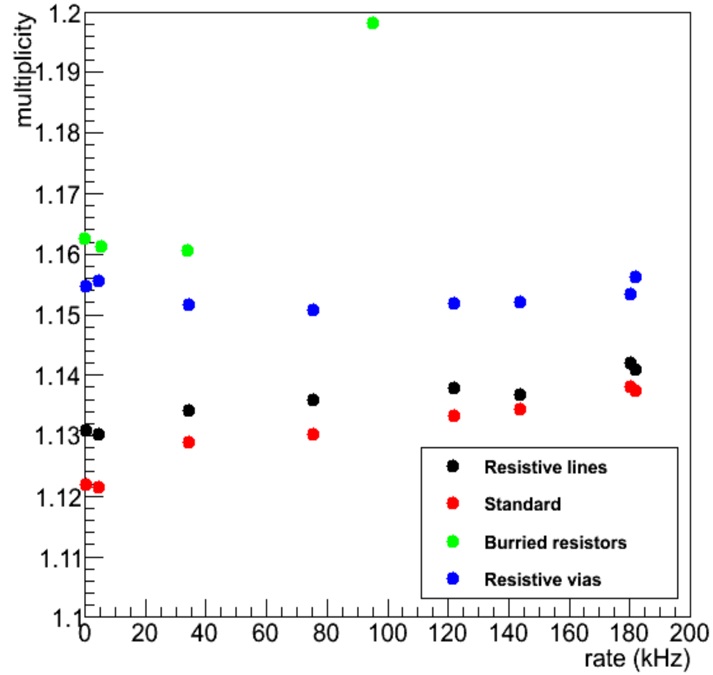
Burried resistors

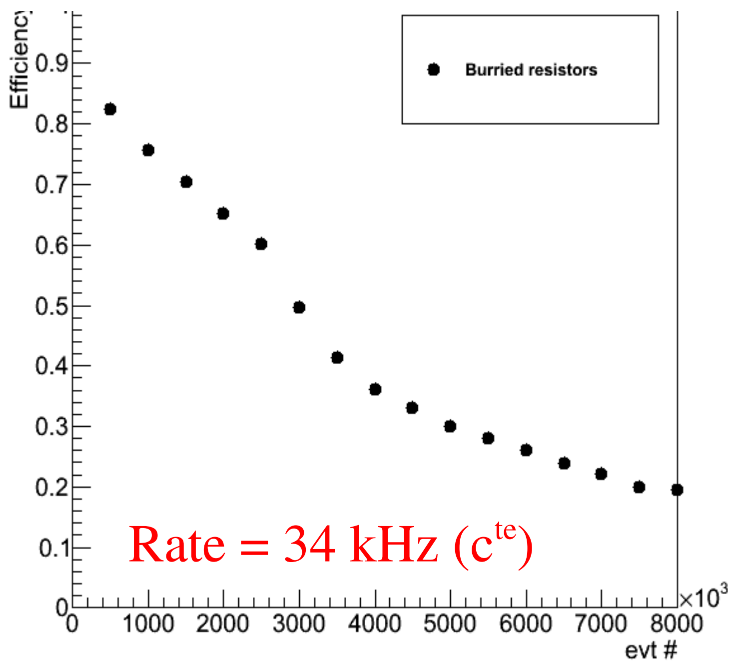
Chb #	Mean value (%)	RMS (%)
2 (resistive lines)	91.3	2
3 (standard)	96.5	1.4
4 (resistive vias)	94.4	1.3
4 (burried resistors)	72.8	35.3

Homogenous response over the all active area within ±2% for all chambers except the burried resistors

Rate capabilities



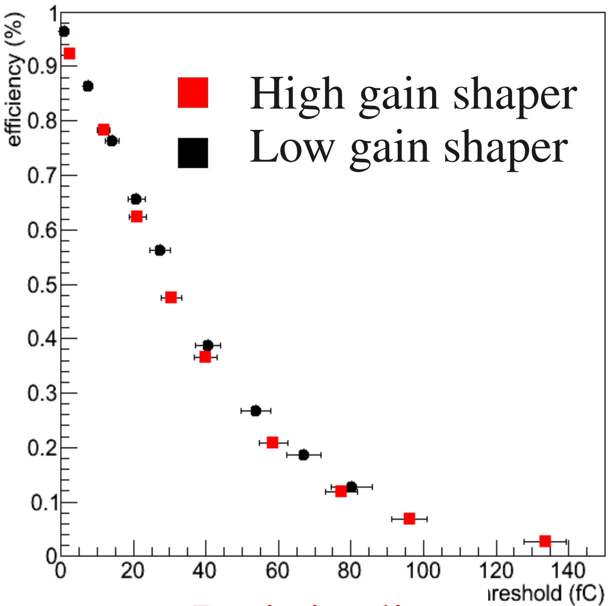




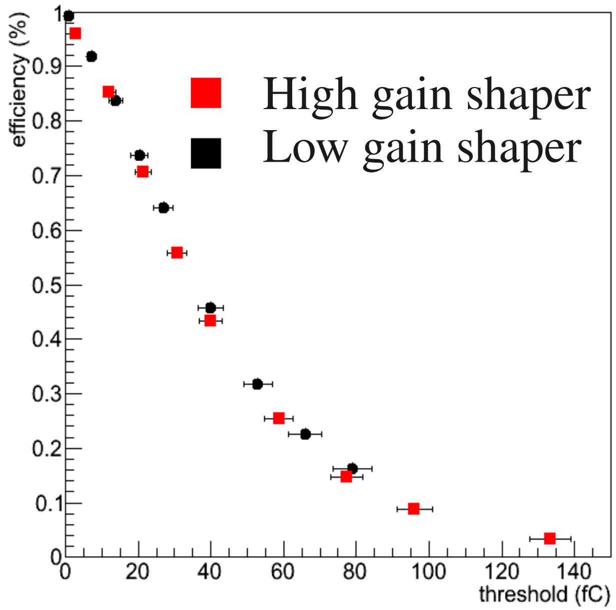
Efficiency and multiplicity remain constant from few kHz → 200 kHz (except for burried resistors chamber that showed a charging up effect due to the construction default)

Low voltage (85% eff.) on the standard Micromegas to avoid crash of the DAQ @ high rate

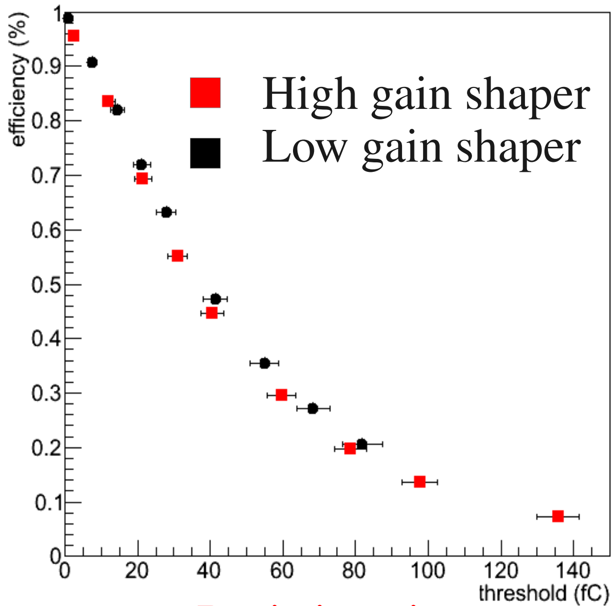
Threshold calibration



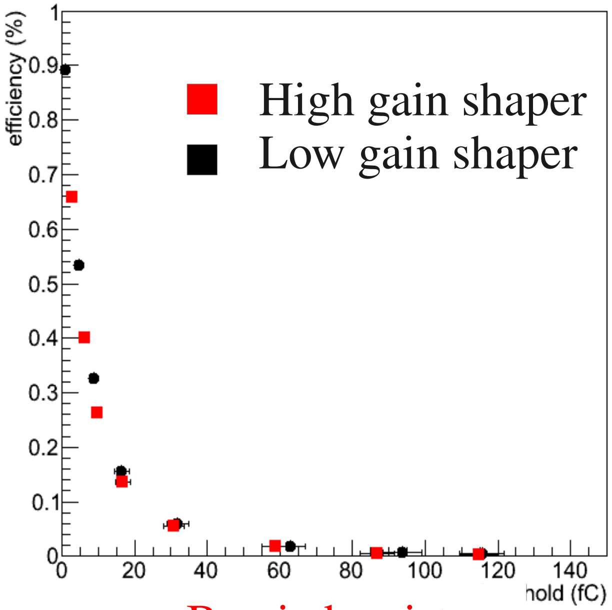
Resistive lines



Standard



Resistive vias



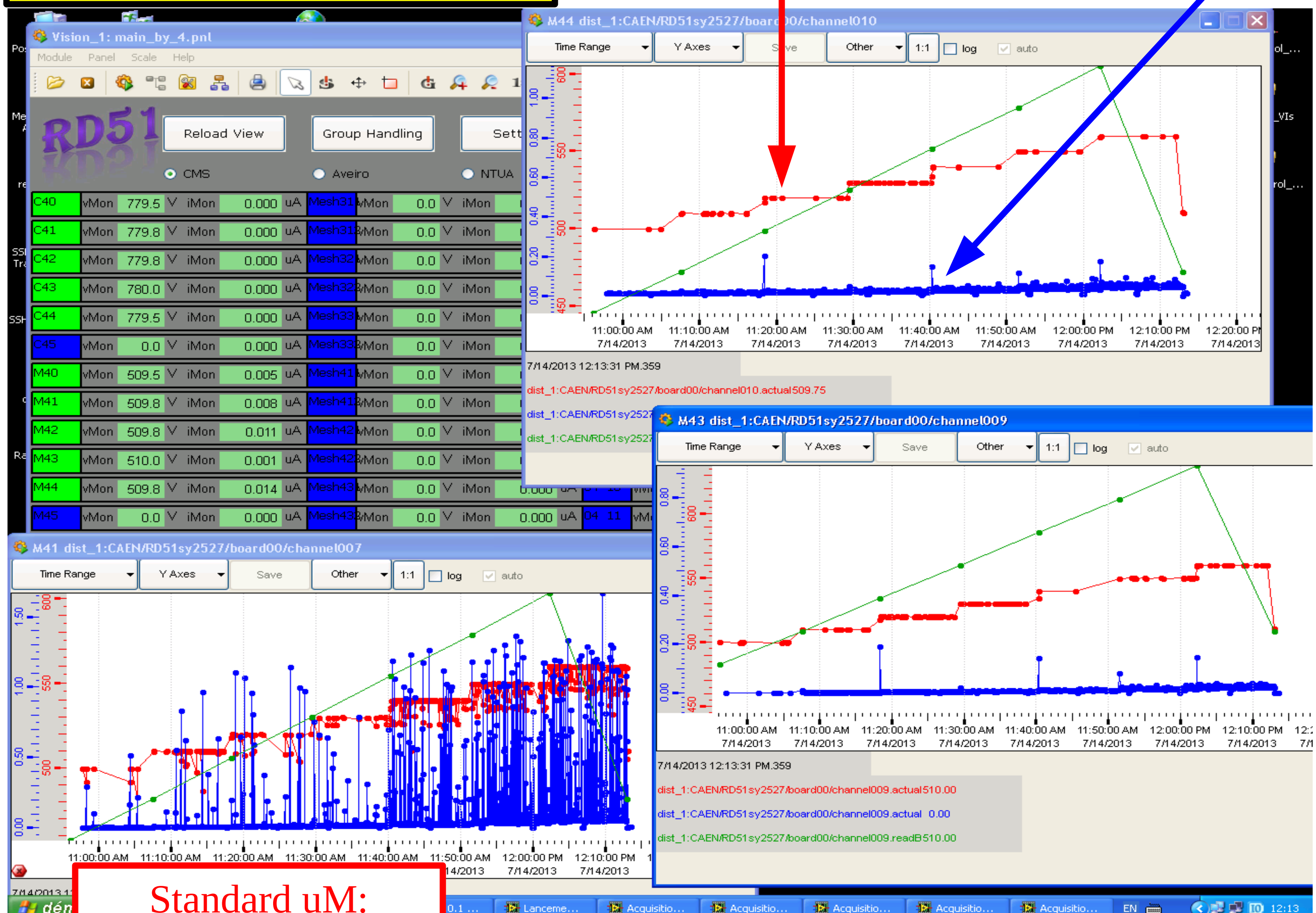
Burried resistors

For all chambers, trends superimpose → calibration factors (DAC/fC) OK

Spark rate

Spark study : increase Vmesh by step, look at current

Significant rate: 5 kHz / 4 cm^2

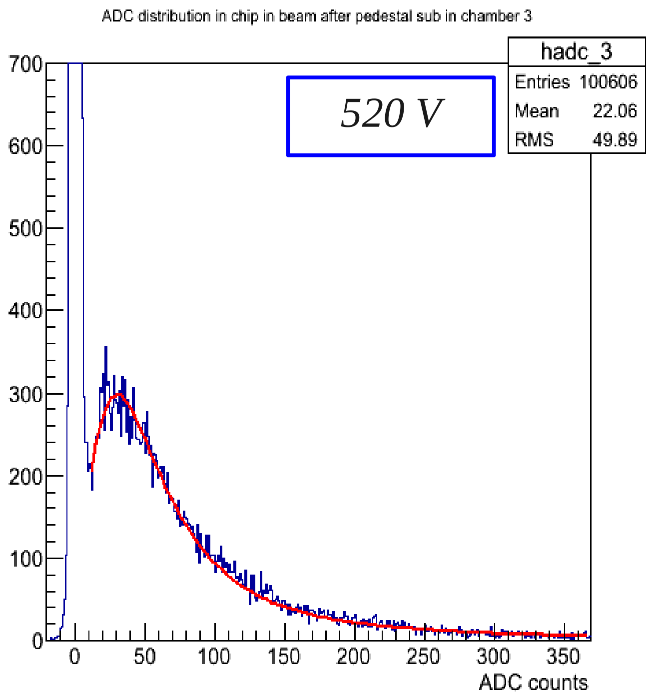


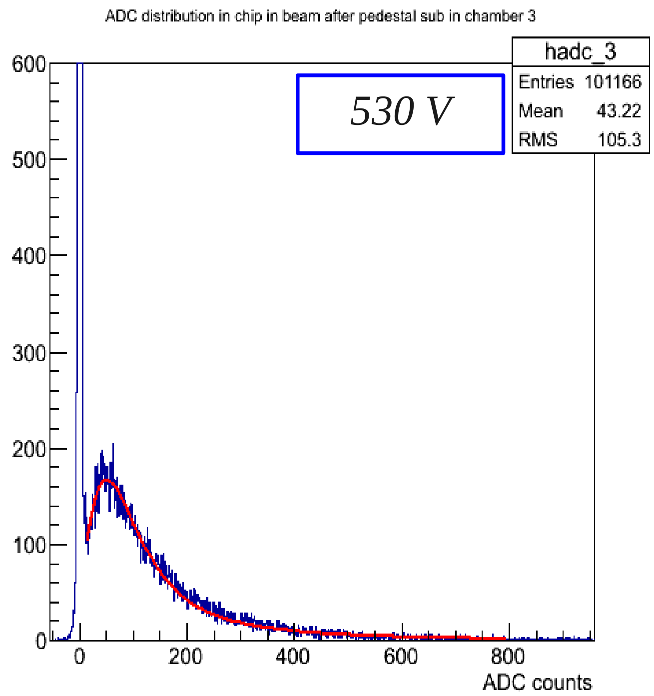
Resistive1 uM: QUIET!

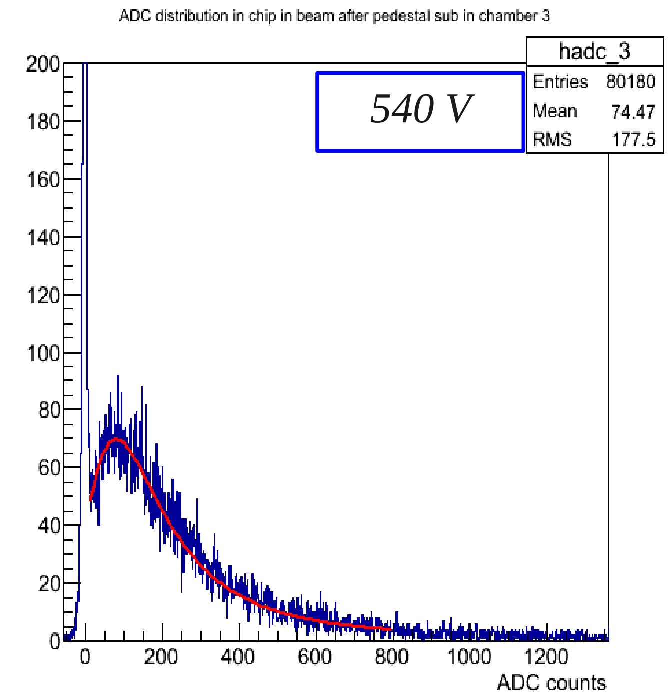
Resistive2 uM: QUIET!

Standard uM: WILD!

Analog readout







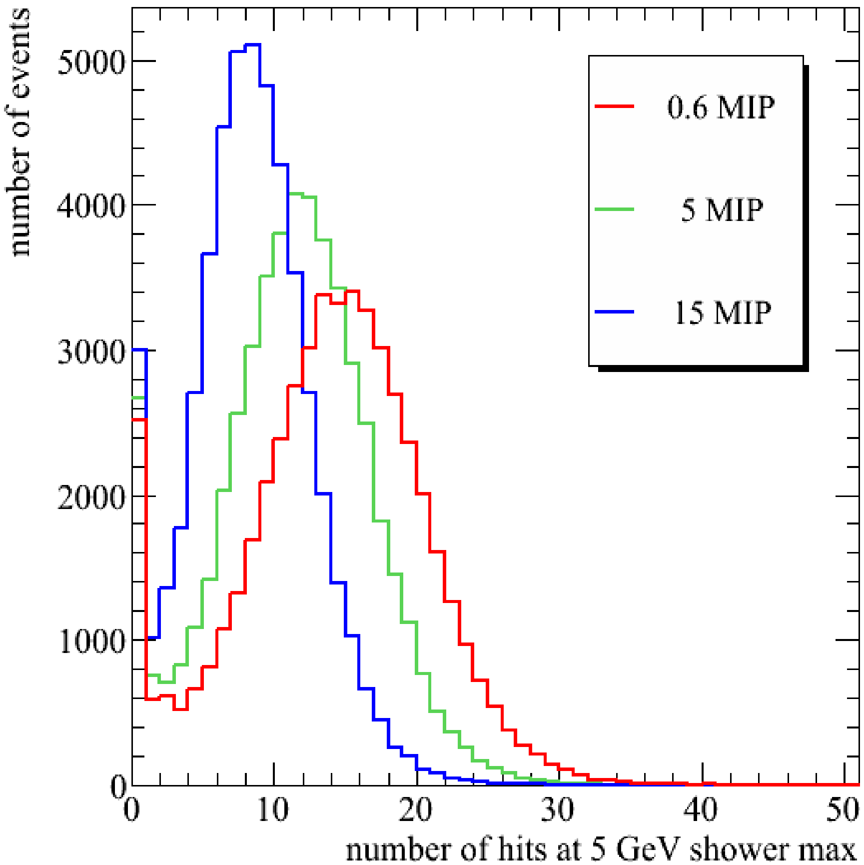
MIP measurements

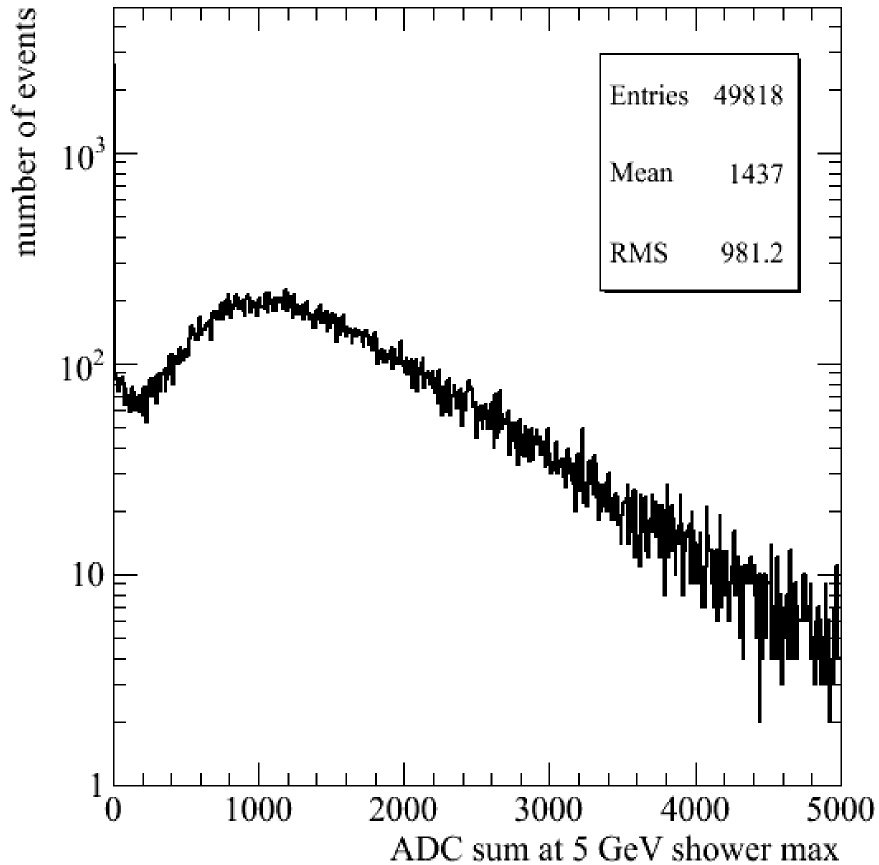
Very nice Landau distributions (pedestal will disappear after cut on digital info.)
Allows us to tune finely our threshold without any calibration constant

Shower measurements

→ *see next slides*

EM showers (1/3)



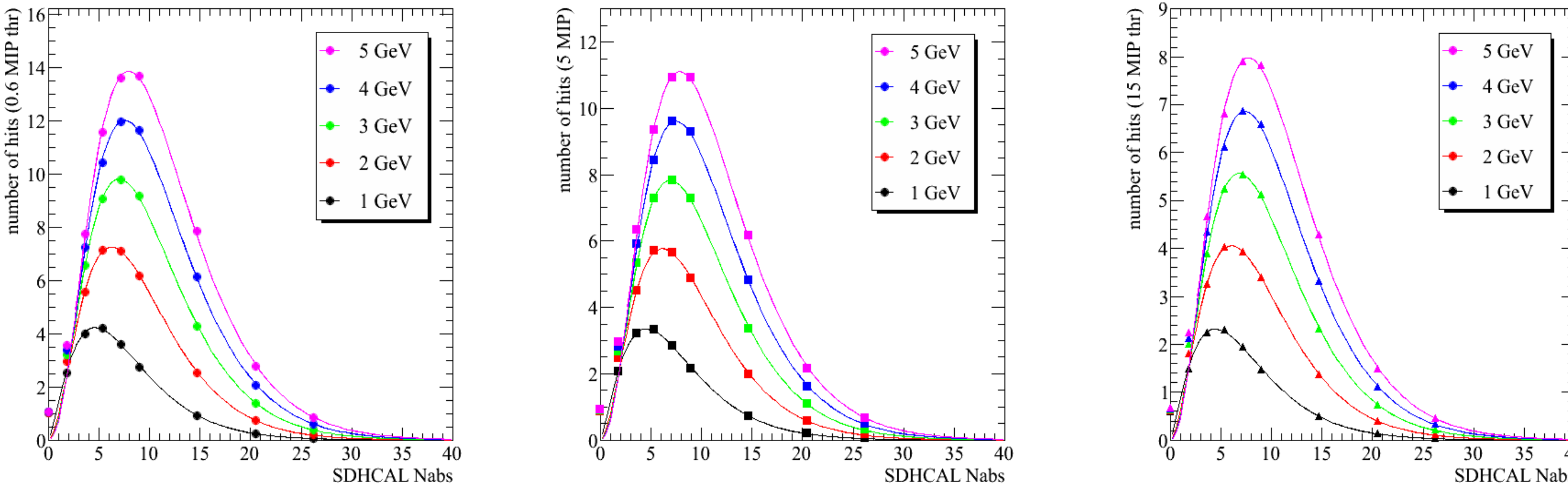


Digital response 1st chamber @ 5 GeV (7.2 cm absorber thickness)
Thr0 : mean value = 13.6 Nhits
Thr1 : mean value = 10.9 Nhits
Thr2 : mean value = 7.9 Nhits

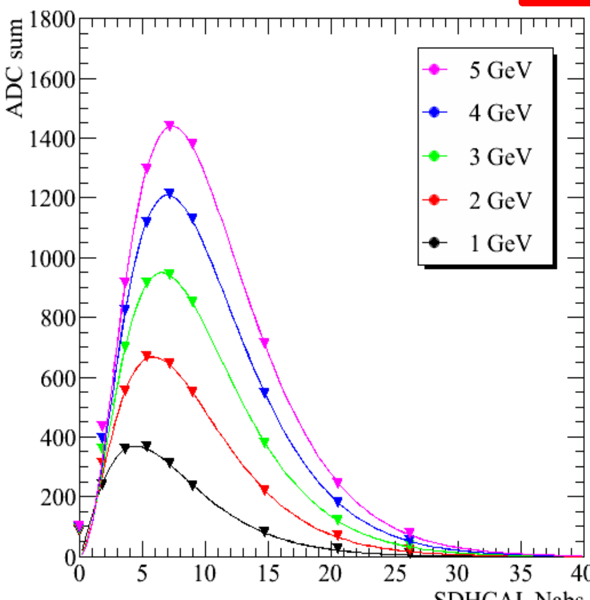
Analog response 1st chamber @ 5 GeV (7.2 cm absorber thickness)
Mean signal = 1437 ADC

Steel thickness (cm)	0	1.8	3.6	5.4	7.2	9	14.75	20.5	26.25

EM showers (2/3)



Digital EM shower longitudinal profile from 1 to 5 GeV



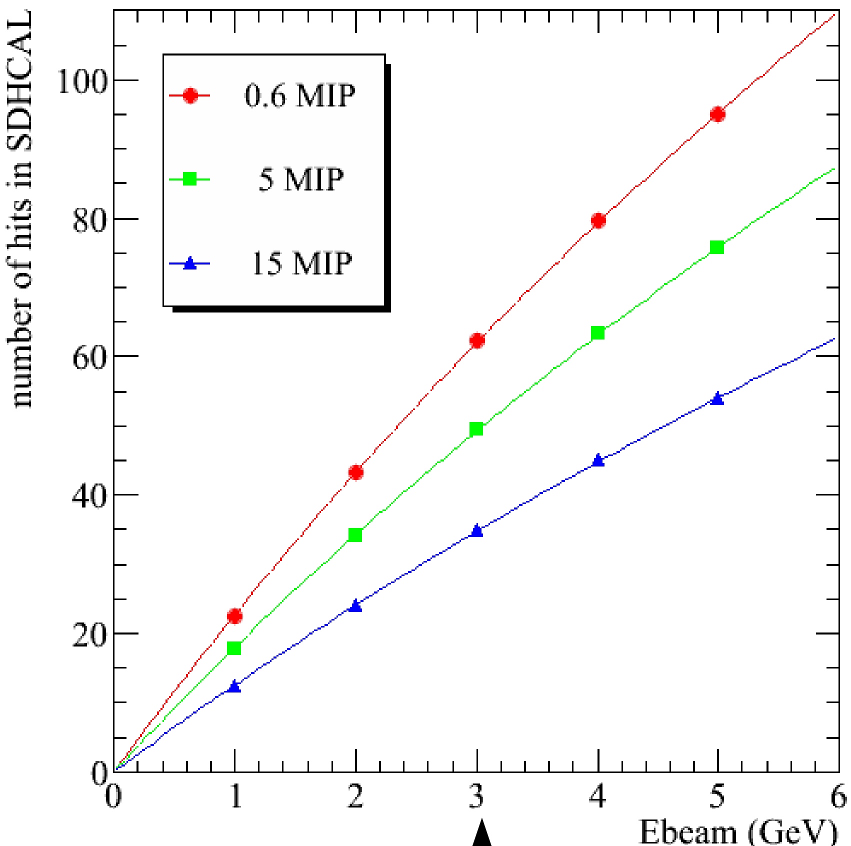
Analog and digital profiles → nice shapes

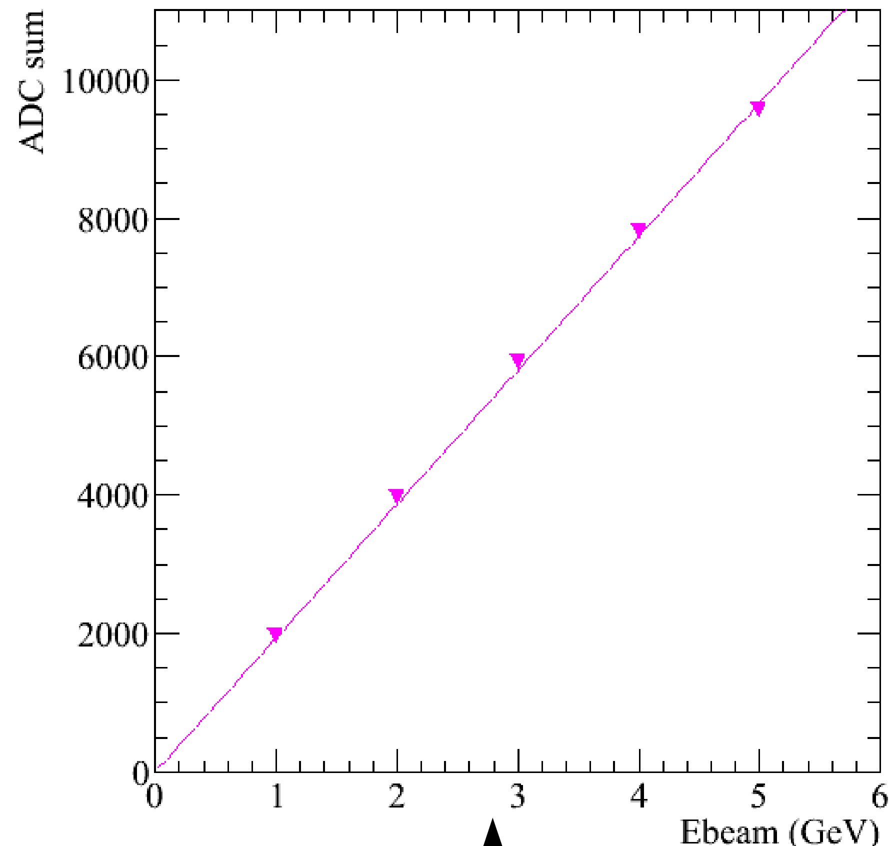
For both analog and digital profiles : Fit with $A.x^{B}.e^{-x/C}$

→ get the integrated response

Analog EM shower longitudinal profile from 1 to 5 GeV

EM showers (3/3)





Integrated profile

<u>Response of a Micromegas SDHCAL to electrons :</u>

→ Digital response shows strong saturation

→ Analog response almost fully linear

Conclusion

Resistive Micromegas → good physical performances

Efficiency ≥ 95 %

Multiplicity ∈ [1.03, 1.25]

Rate capabilities until at least 50 kHz/cm^2

Response uniformity ≤ 2 %

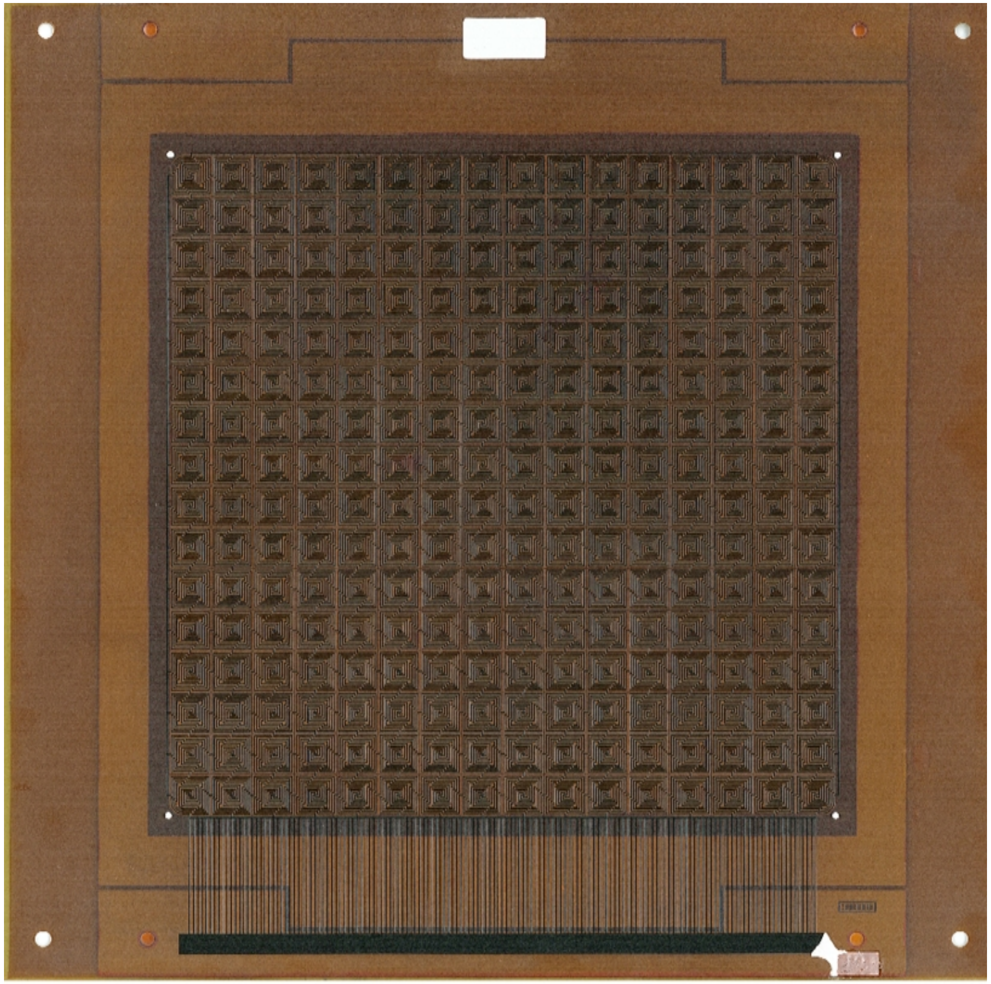
→ but also demonstrate their ability to face discharge without any damages on the R/O electronics, no voltage drop

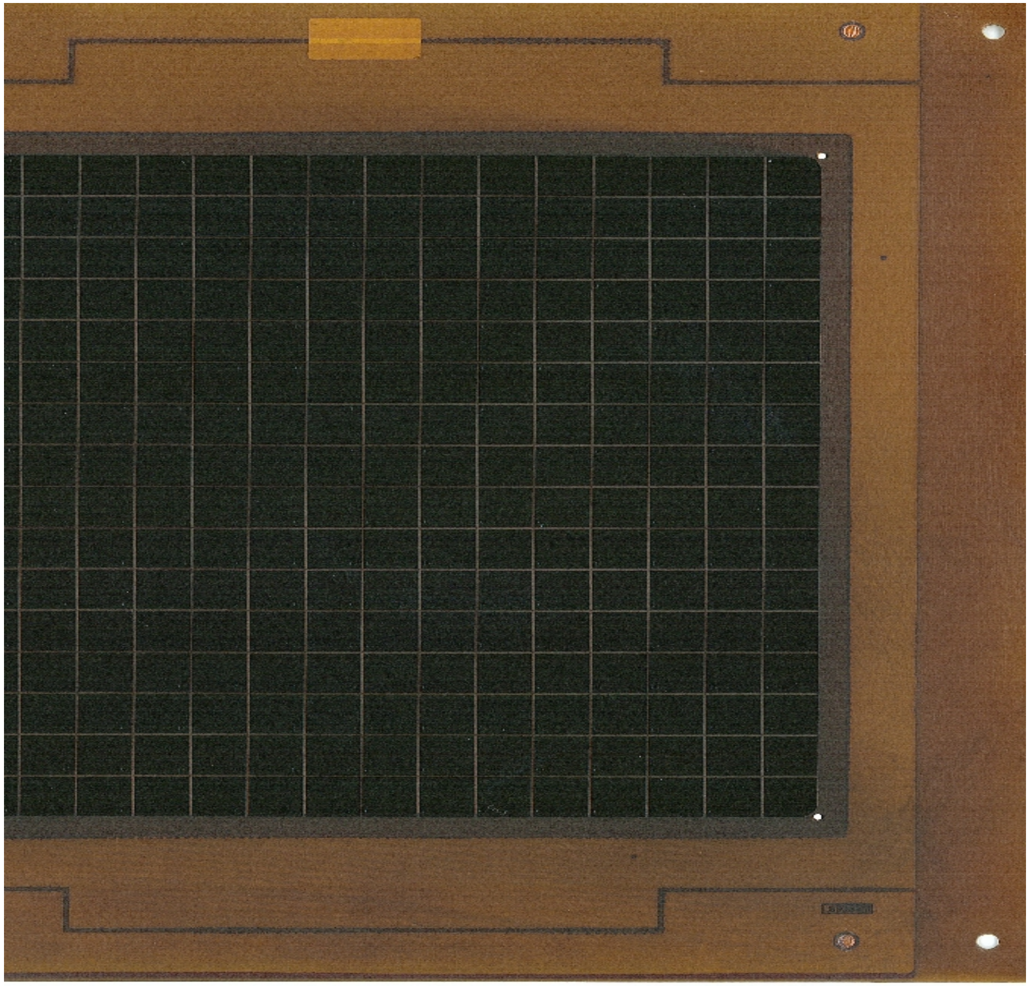
Configuration with burried resistors should be tested again with a correct construction to validate (or not ???) the principle

Thanks to DESY people for their help during the TB period : Katja, Mathias, Ralf and Sam

The (dream ???) team

Back up slide





Back up slide