AHCAL prototype overview

- goals
- status & plans:
  - hardware
  - analysis
  - DAQ
  - infrastructure
- conclusions & outlook

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CALICE Collaboration meeting

Annecy, 10 September 2013

HELMHOLTZ ASSOCIATION

Calorimeter for ILC

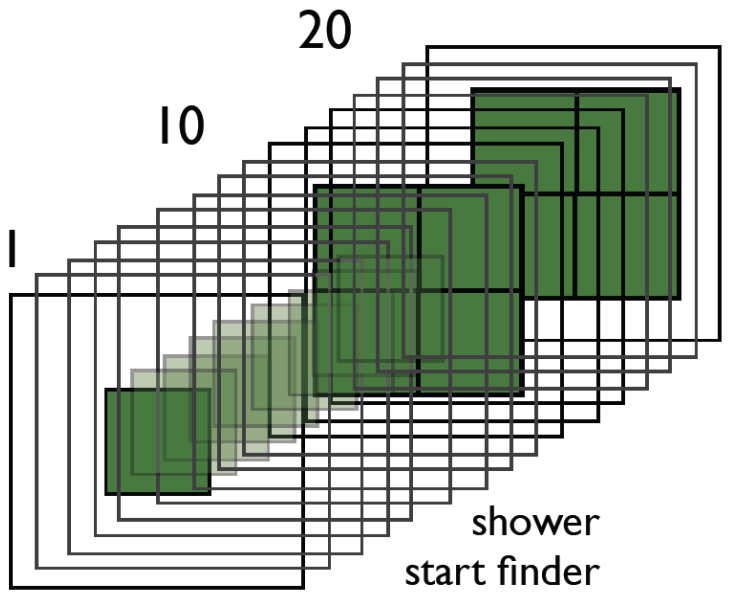
Universität Hamburg
DER FORSCHUNG | DER LEHRE | DER BILDUNG

DESY

On the way to a full engineering prototype

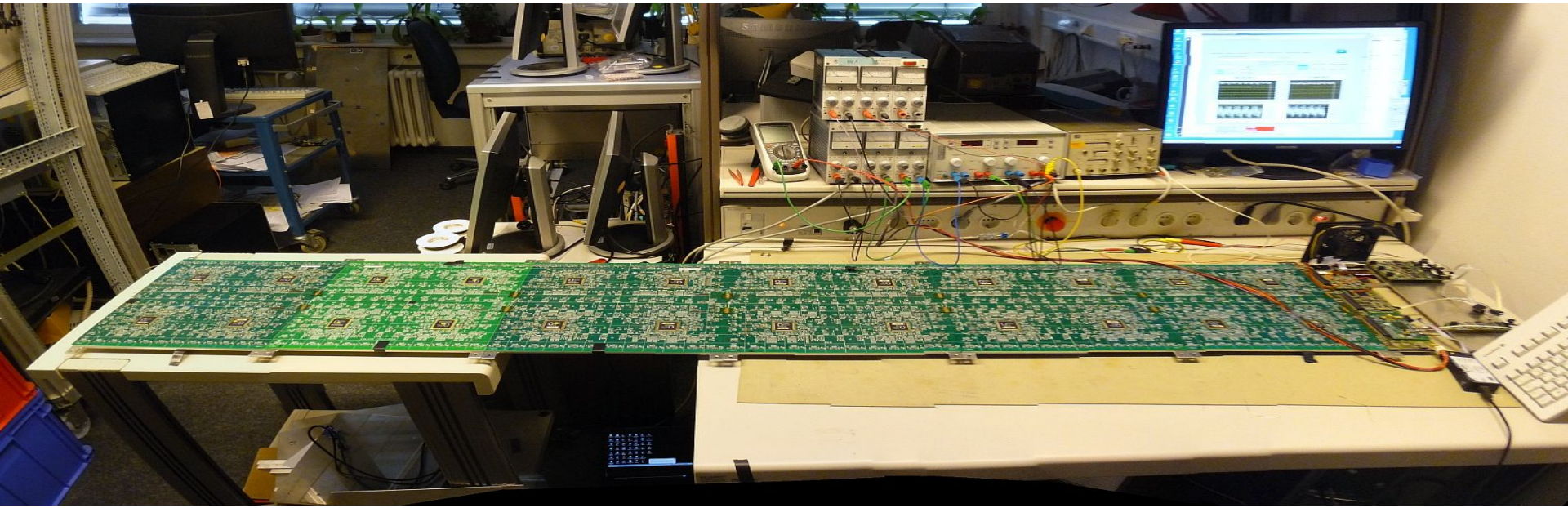
goals:

- 2013/2014:
  production, calibration and test of new hardware
- beginning of 2014:
  measurements of EM showers in the small ILD-like stack
- 2014/2015:
  first measurements of hadrons with a “shower start finder” and a few 2*2 HBU layers
  - ILD stack
  - tungsten stack
- longer term: fully equipped 1m^3



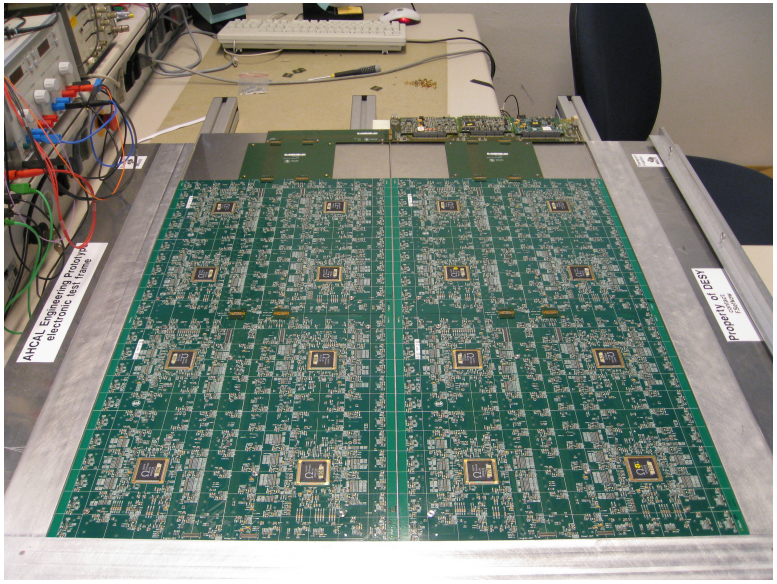
going from 1 HBU to a detector prototype: 1D

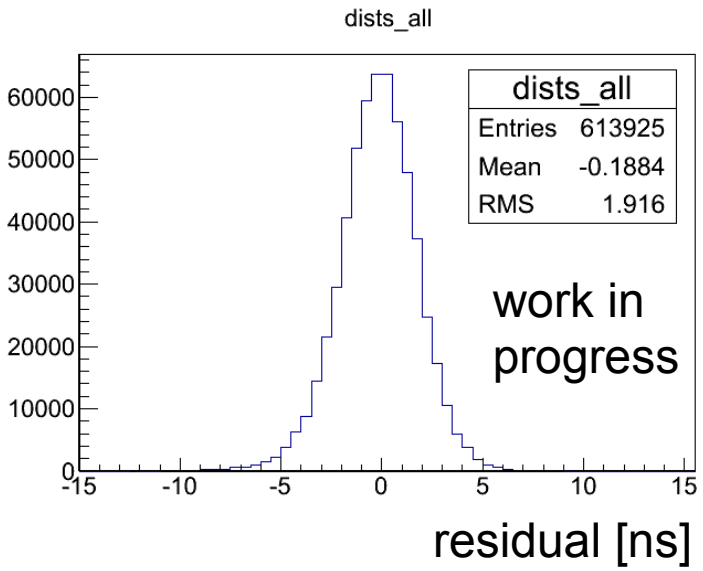
- single HBUs extensively tested and calibrated in lab
- cross check the calibration and the uniformity of all channels on one chip with MIPs in testbeam
- operation of a slab with 6 HBUs
- power pulsing with a full slab: started (more details in talk by S. Chen)



going from 1 HBU to a detector prototype: 2 (+1) D

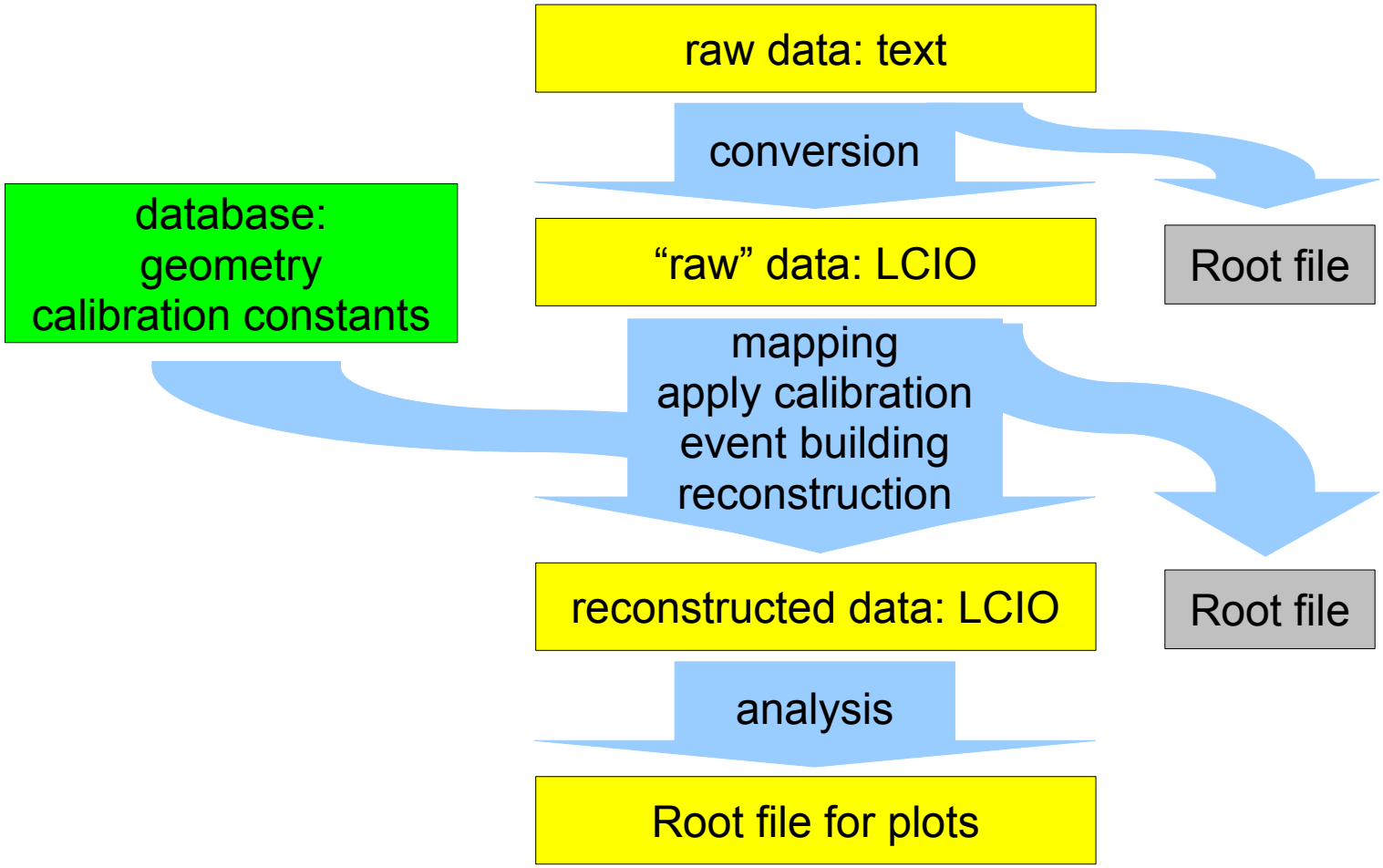
- 1 layer with 2*2 HBUs successfully operated in CERN SPS muon and pion testbeam
- calibration and analysis of the TDC time measurement in progress





Analysis of 2D testbeam data: software

- use standard ILCsoft based on LCIO framework, database to store geometry and calibration



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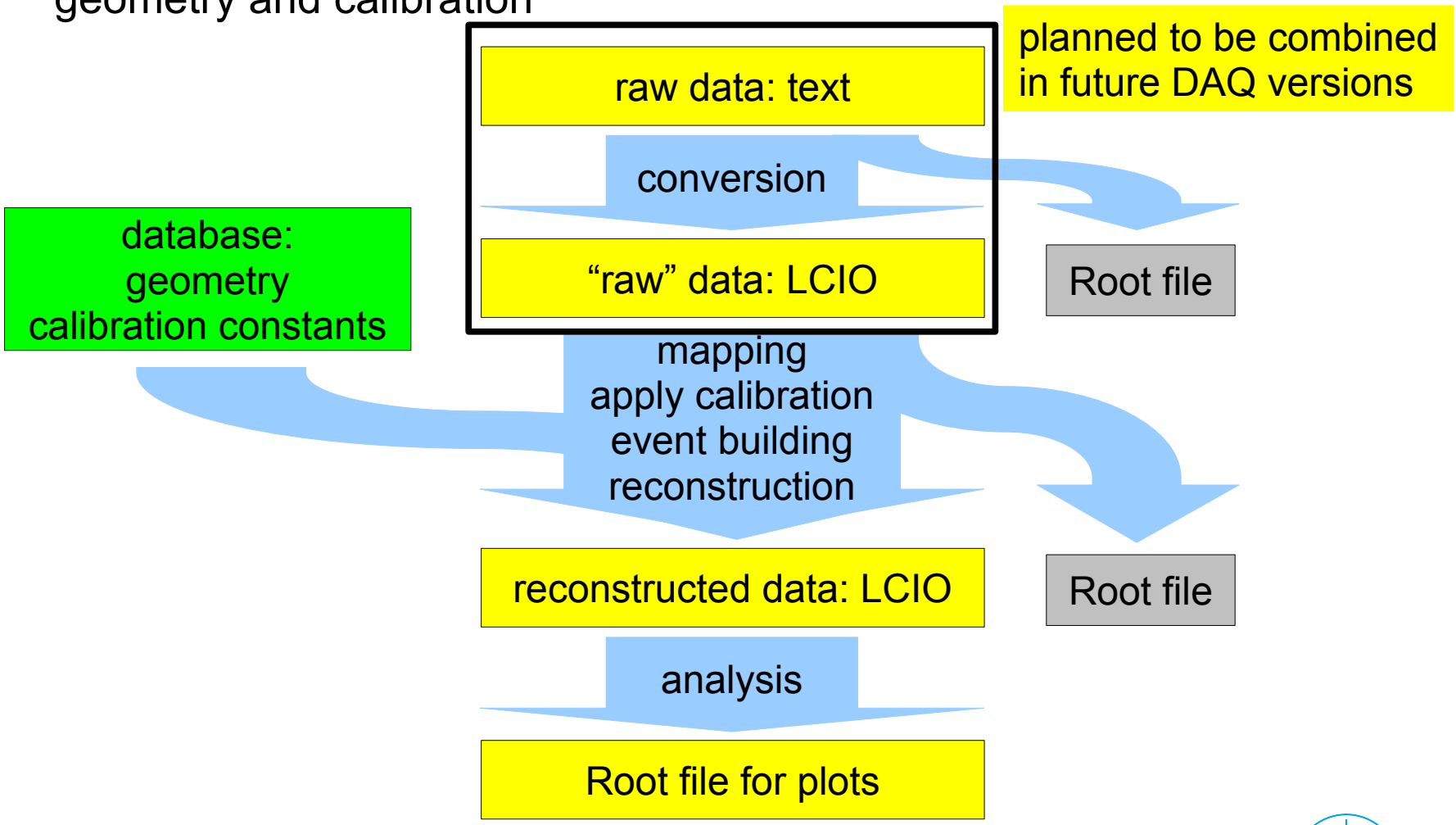


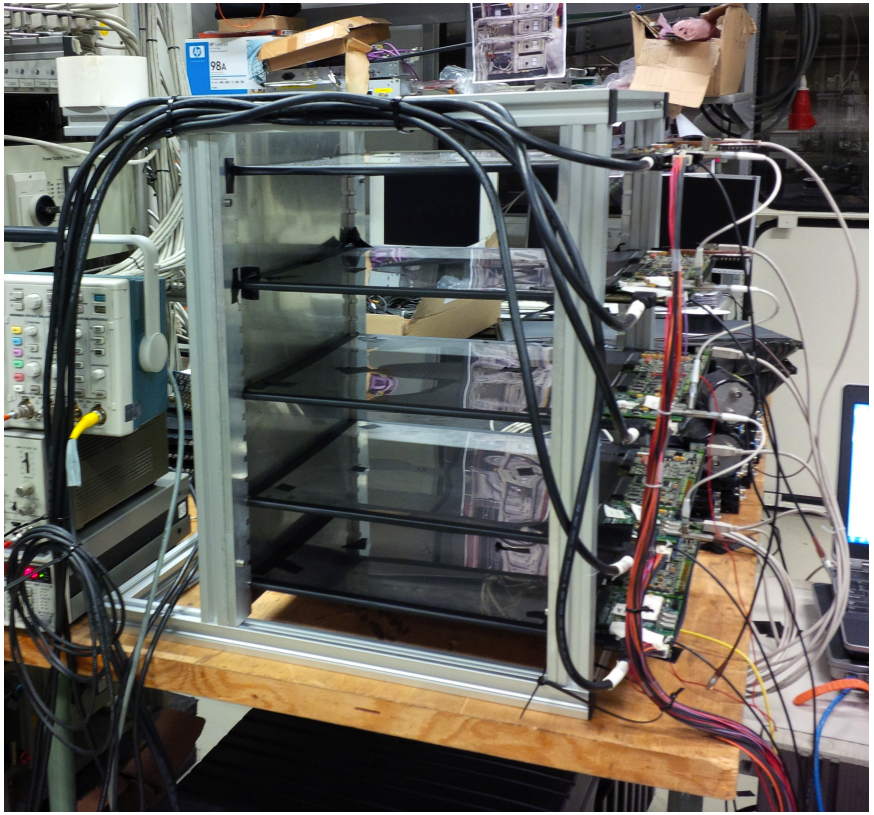
going from 1 HBU to a detector prototype: 3 (+1) D

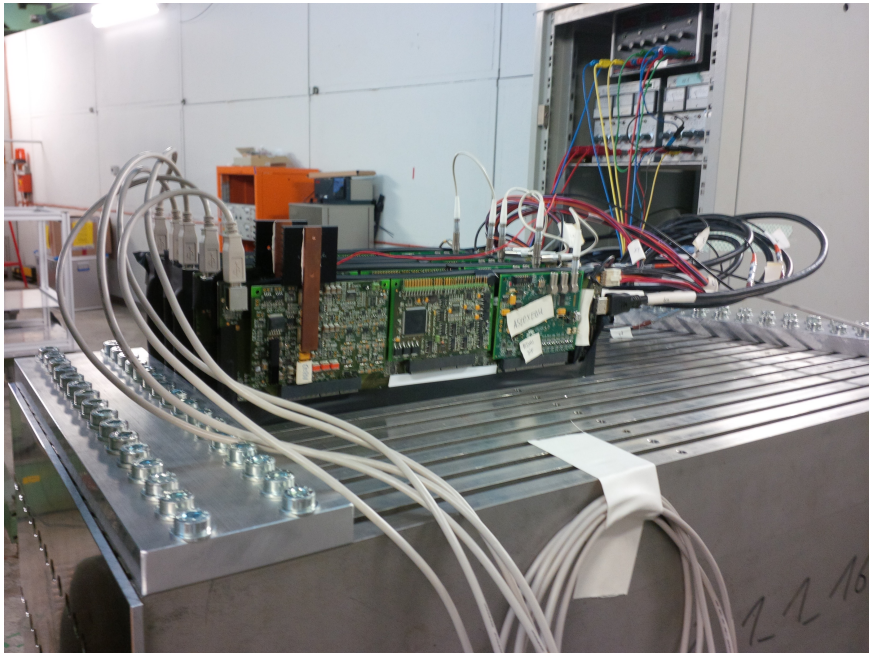
several challenges going 3D:

- mechanics:
  - absorber stack (+ air stack)
  - cassettes
- multi-layer DAQ
- power supply for many layers
- scaling: need more tiles, SiPMs, HBUs, CIBs, DIFs, …
  - mainly limited by tiles+SiPMs
  - layer-wise electronics (CIBs, DIFs, …) exist for 20 layers

Mechanics: Stacks

- air stack for 20 layers of 1 HBU used for cosmic test and MIP calibration
- ILD-like absorber stack for 15 layers (EM showers) installed "permanently" in DESY testbeam 22
- preparation of big ILD stack in HERA Hall North

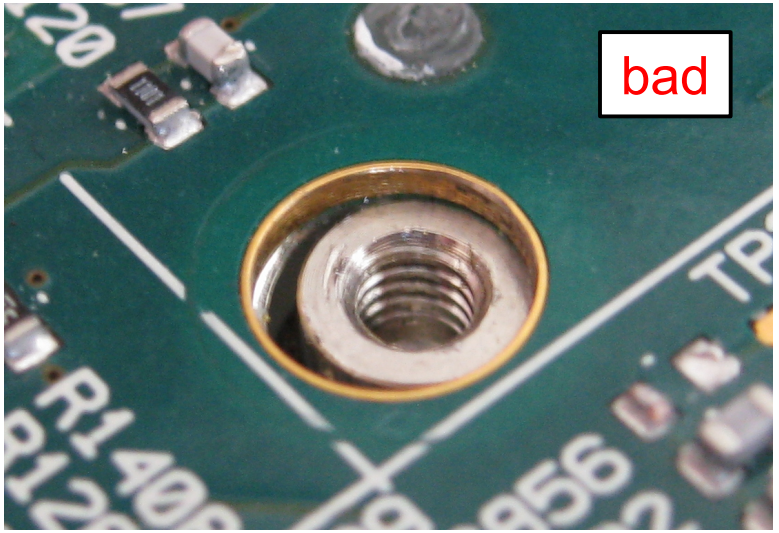




Mechanics: Quality Control

observed problems with mechanical accuracy of HBUs and cassettes:

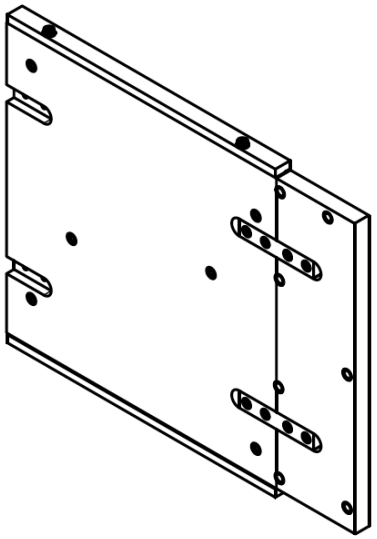
- in first batch of 6 HBUs, one “pin” of the cassettes misaligned, HBUs are OK
  - temporary solution: enlarging the holes in the HBUs
  - permanent solution: tool for quality control of cassettes

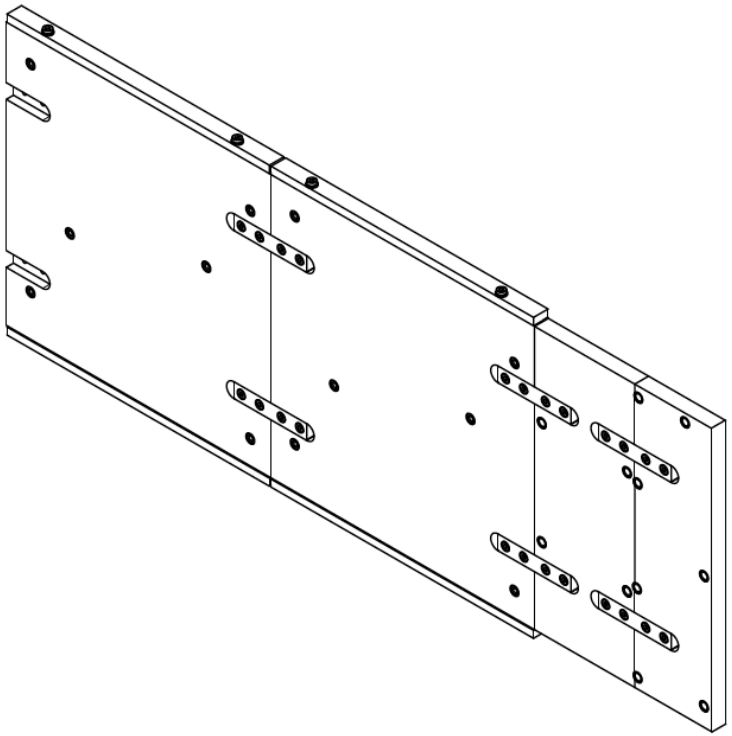


- in second batch of 8 HBUs, the HBUs do not fulfill the tolerances due to mistake in production process
  - problem is identified and understood, can be cured (as in first batch)
  - temporary solution: every HBU will get its own cassette
  - permanent solution: tool for quality control of HBUs

Mechanics: Tool for Quality Control of Cassettes and HBUs

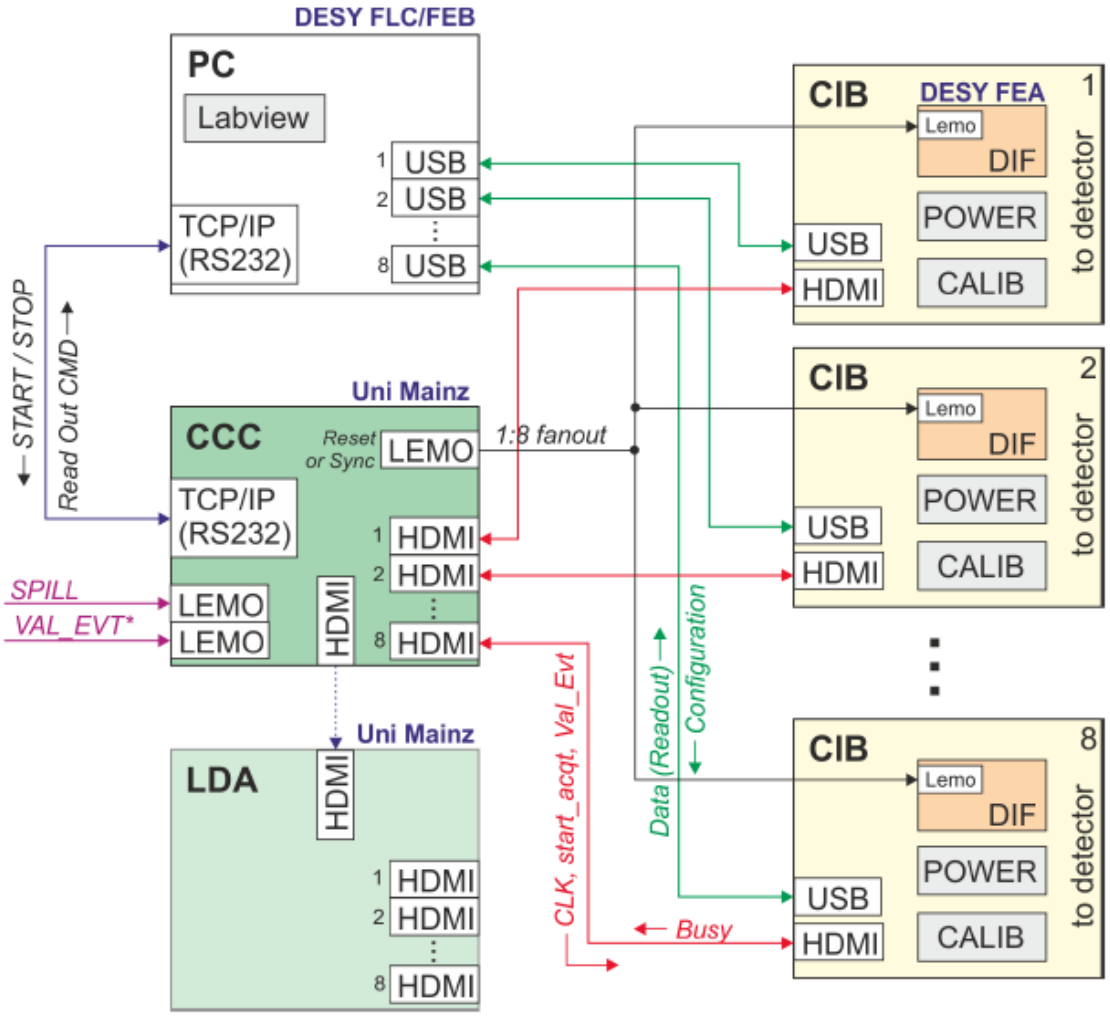
- modular tool to check dimensions
  - of cassettes and their pins
  - of HBUs and their holes
  - of additional boards: CIBs, SIBs, extenders
- parts designed and ordered





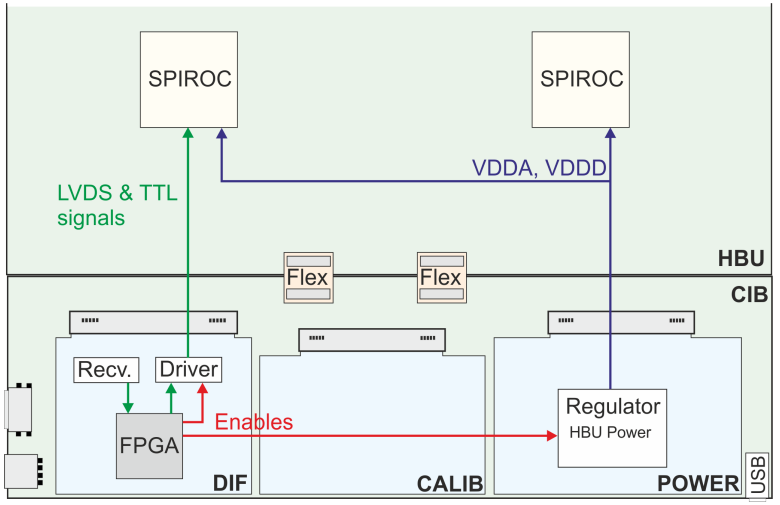
Progress towards a multi-layer AHCAL DAQ

- starting point: 1 layer DAQ (PC with Labview, 1 CIB) successfully operated lab and testbeams
- status: CCC (+fanout) included, fast signals via HDMI, operated successfully with 5 layers
- work on LDA integration started
- todo: switch to data transfer via HDMI
- more details in talk by A. Ebrahimi



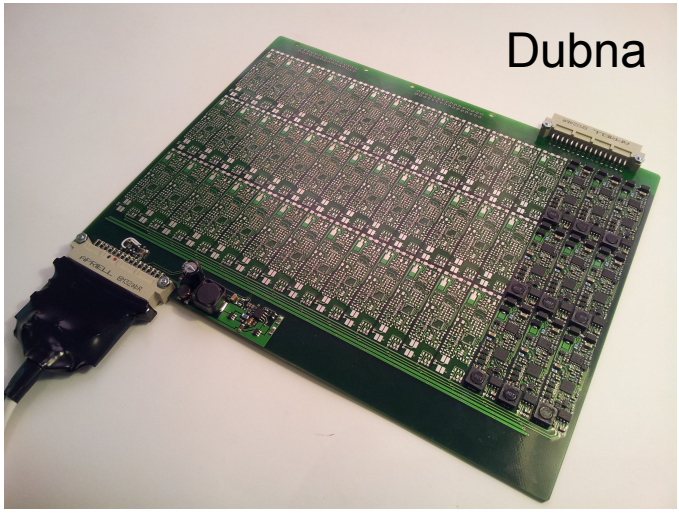
New power-on procedure

- first multi-layer beam test in June 2013 at DESY: observed problems with non-reproducible conditions in runs
  - changing dead and noisy channels
  - “stuck” TDCs
- problem identified and solved:
  - caused by switching on signals lines to SPIROC before power lines
  - solved by proper power-on procedure (with slightly modified power board)
- procedure successfully tested:
  - for ScECAL testbeam beginning of July 2013
  - dedicated tests with AHCAL in dedicated beam test end of July 2012
- more details in talks by M. Reinecke and A. Ebrahimi



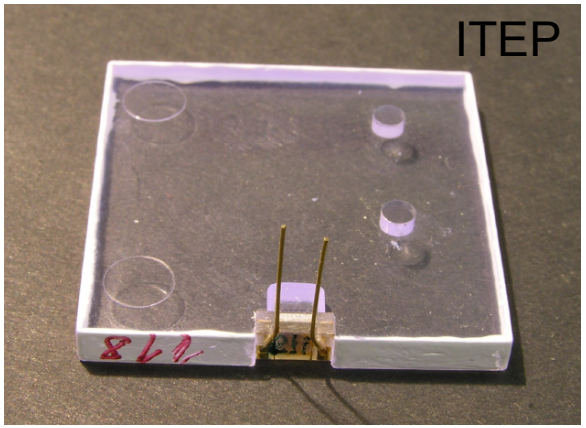
Power supply

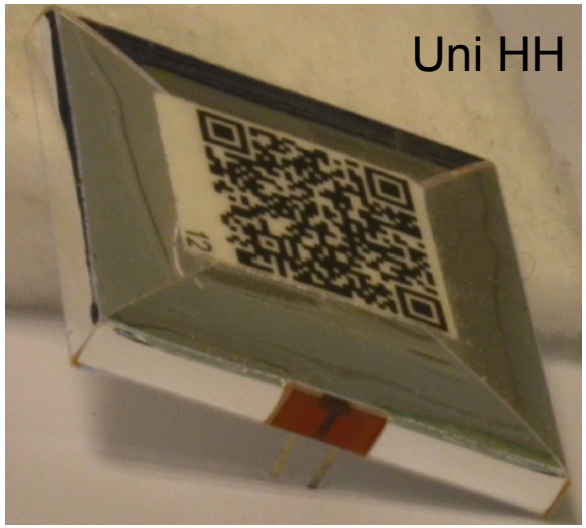
- dedicated, low-cost system, scalable to ILD size, is being developed at Dubna
- ordered short-term solution for testbeams: commercial system usable for up to 16 layers
  - upgradable to 48 layers
  - independent HV (up to 100 V), 12 V and 6 V supply for each layer
  - step-by-step transition to dedicated system planned
- started design of power distribution box
  - on the power supply side, the same voltages are on one board
  - on the detector side, 1 layer needs all 3 voltages



Going mass production: more tiles+SiPMs

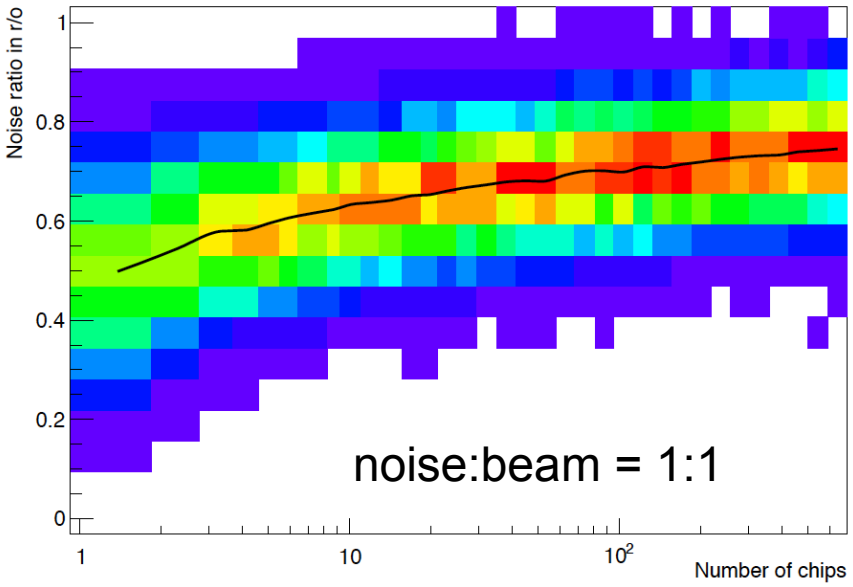
- ITEP produced direct-readout tiles (+ Ketek SiPMs with 12100 pixels) for 2 HBUs, paperwork ongoing
- NIU: 1 HBU with top-view SiPMs being tested
- Uni HH produced direct-readout tiles for 8 HBUs, Ketek SiPMs with 2300 pixels for 8 HBUs delivered and being tested now (more details in talk by K. Briggl)
- expect Hamamatsu MPPCs for 4 HBUs from Japan, ITEP agreed to produce direct-readout tiles
- mass assembly: talk by P. Chau
- testing several different options now, but for practical reasons will need to converge to 1 or 2 for larger prototypes (but this will not be an advance decision for ILD calo)





Other ASICs needed? (SPIROC2d or SPIROC3)

- started to look into rate dependency of fraction of noise events
  - for now focus on sequence
    - EM stack (<60 chips)
    - HCAL with shower start finder (~100 chips)
    - 1m^3 HCAL (600 chips)
  - plan to check simulation also for ILD calo
- fraction of useful events is OK with SPIROC2b for EM stack and HCAL with shower start finder

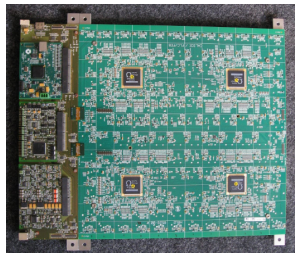


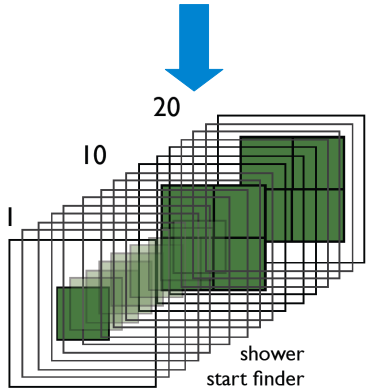
- data taking possible, but with non-optimal efficiency for 1m^3 HCAL with current SiPM noise rates, possible solutions:
  - close the validation gap
  - zero suppression (only the triggered channel read out, not all 36 channels on a chip)
- problem for both HCALs: “first event bug” (ADC values in first triggered event in every read-out cycle are zero)
- more details in talk by M. Reinecke

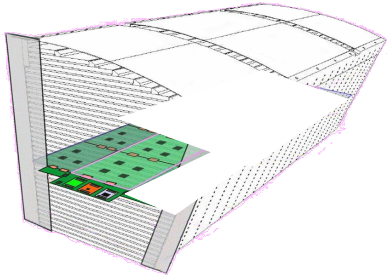
Conclusions and Outlook

preparations for a full engineering prototype:

- multi-layer DAQ: first version running, next steps:
  - integration of LDA
  - switch to HDMI readout
- work on quality assurance & infrastructure
- more hardware, especially tiles+SiPMs, in production







next testbeams at DESY:

- 1 week in October 2013
- 11 days in December 2013
- 2 weeks in January 2014