

SiECAL Technological prototype Test Beam at DESY

Tokusui meeting 2013

Yuji Sudo (Kyushu University)

Tokyo Univ. LAL LLR CALICE

SiW ECAL R&D

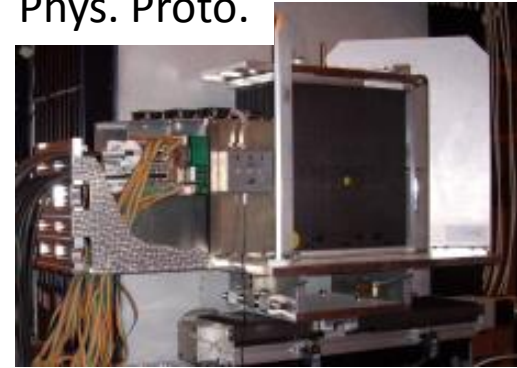
Physics Prototype 2003 - 2011

Proof of principle

Number of channels : 9720

Weight : ~ 200 Kg

Phys. Proto.



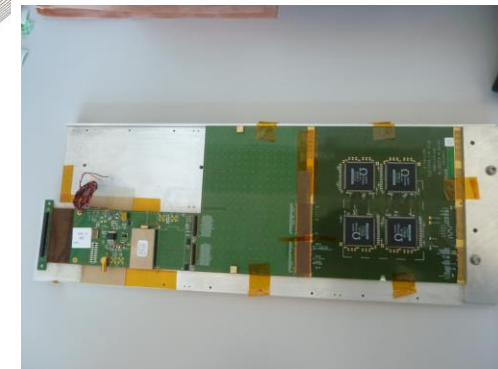
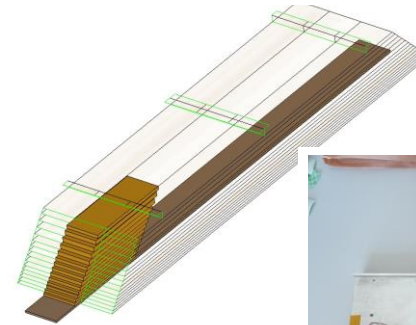
Tech. Proto.

Technological Prototype 2010 –

Technological solutions for the final detector

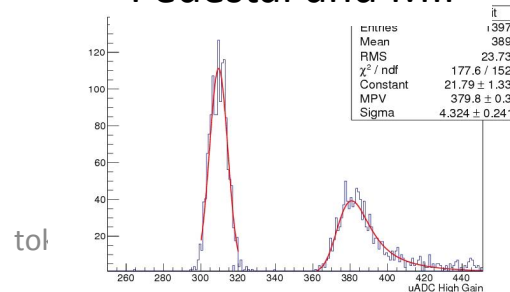
Test program

- 2012: Commissioning
 - Test of highly integrated electronics in continuous power mode
- 2013: Test of power pulsing
 - Test in magnetic field



2012 result

Pedestal and MIP

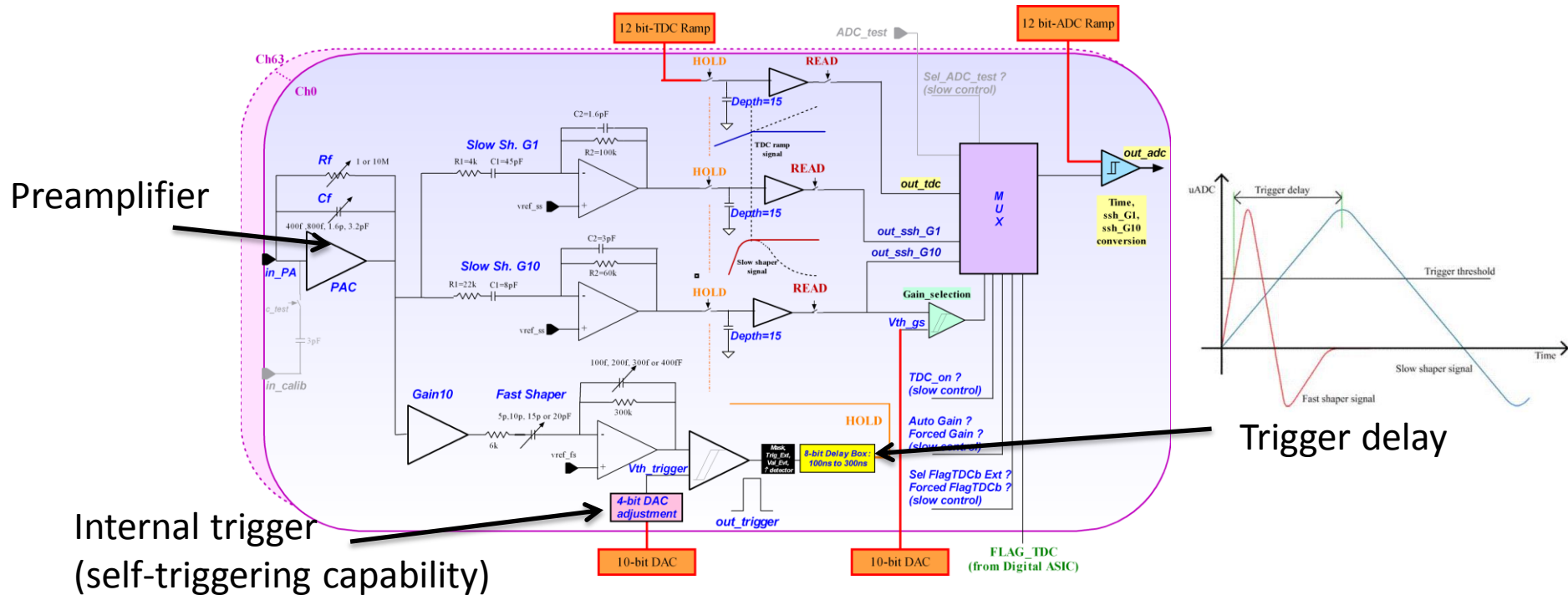
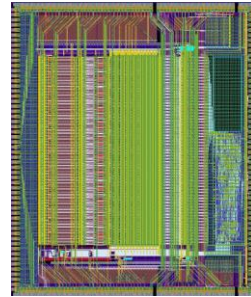


S/N > 10 (for all gains available with SKIROC2)
R&D target is S:N = 10:1

Front end electronics: SKIROC

SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- Size 7.5 mm x 8.7 mm, 64 channels
- Variable gain charge amp, 12-bit Wilkinson ADC, digital logic
- Large dynamic range (~2500 MIPs), low noise (~1/10 of a MIP)
- Self-triggerer
- Low Power: (25 μ W/ch) power pulsing



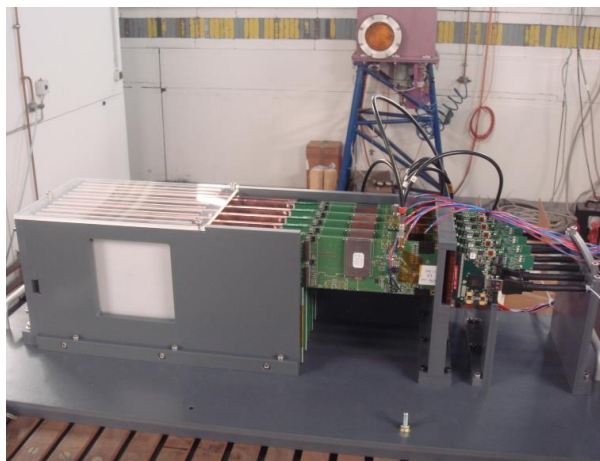
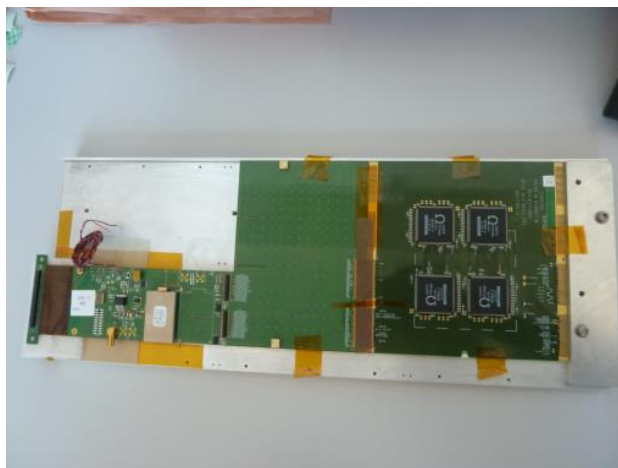
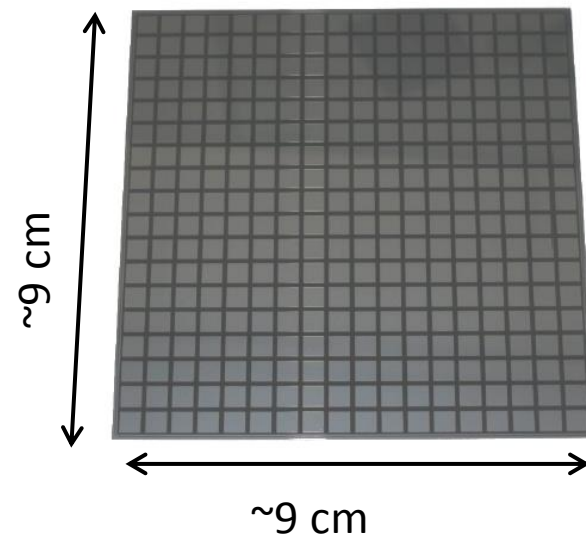
Test beams with fabricated layers

Layer design for beam tests

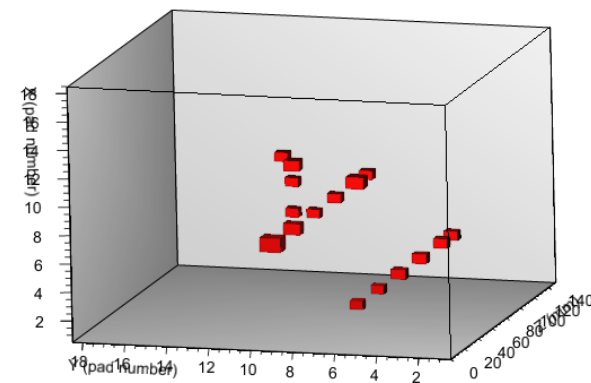
Integrated FE electronics

Conservative ASU design for beam test

- Si Sensor : $5 \times 5 \text{ mm}^2$ pixel and thickness of $325 \mu\text{m}$
- 256 ch readout/layer
- 4 ASICs in PQFP package
- Up to 10 layers



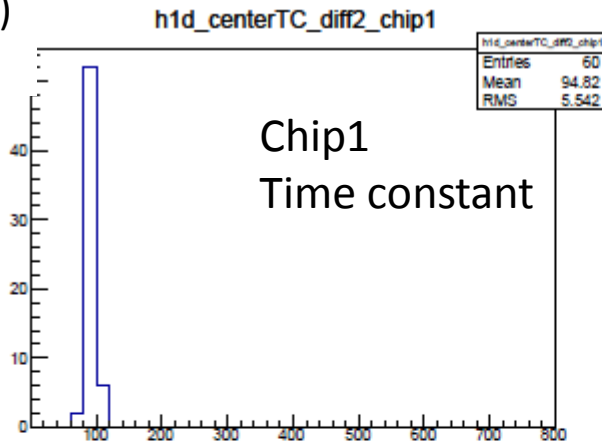
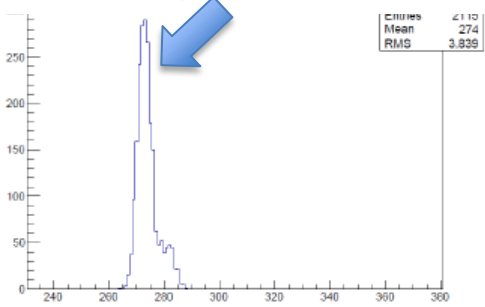
2 e- (3 GeV, no tungsten)



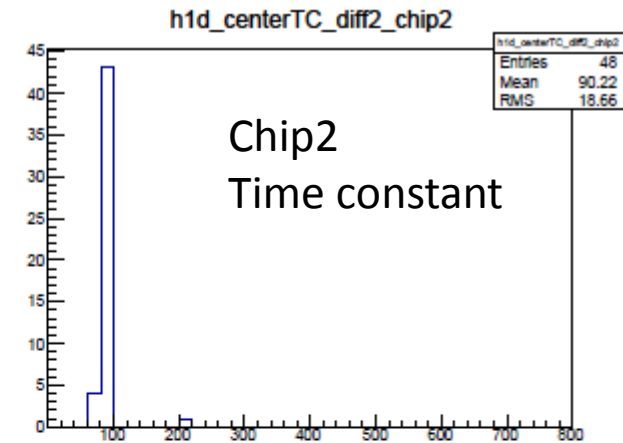
Time constant of pedestal (center value)

- MIP event (Power Pulsing)

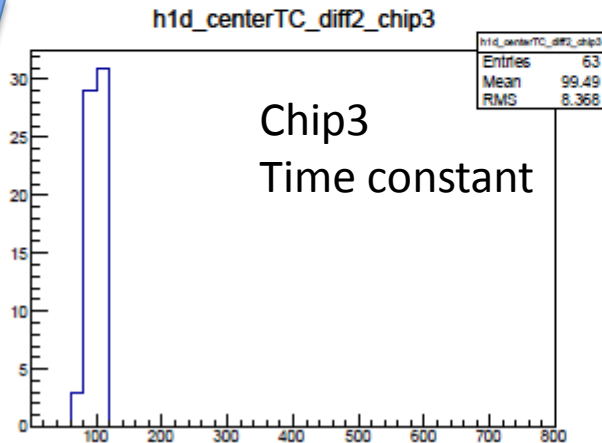
Fit with Gaussian around (+-5bin)
Pedestal peak for each channel



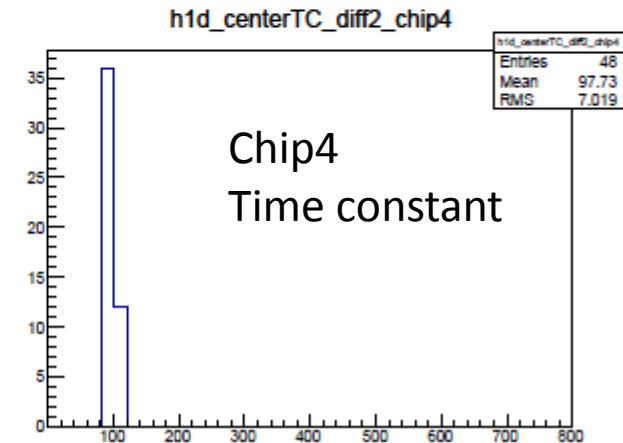
Chip1
Time constant



Chip2
Time constant

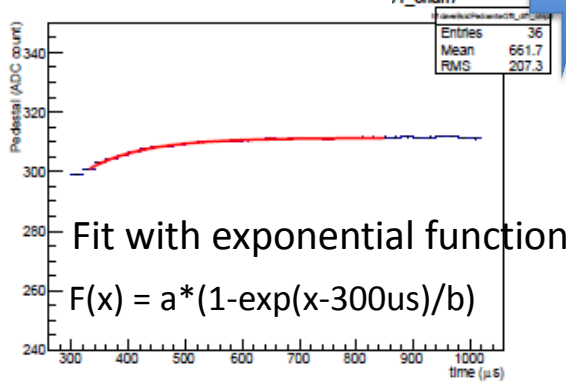


Chip3
Time constant



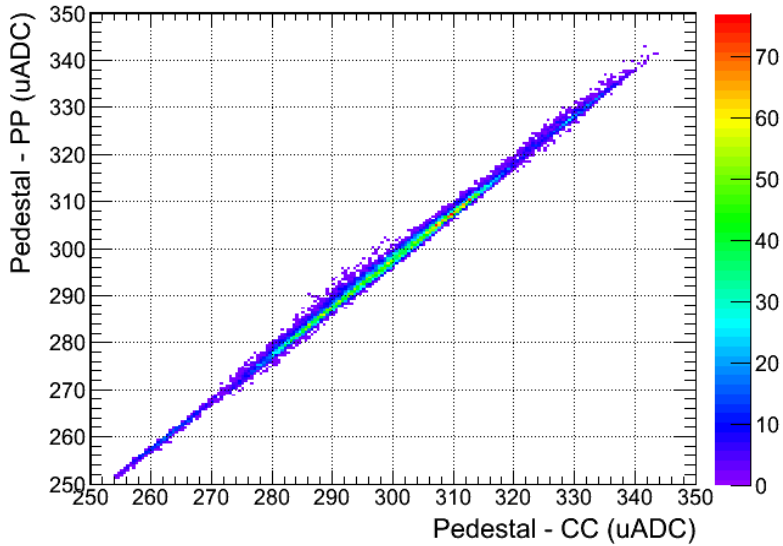
Chip4
Time constant

Dif2, chip4, chan7

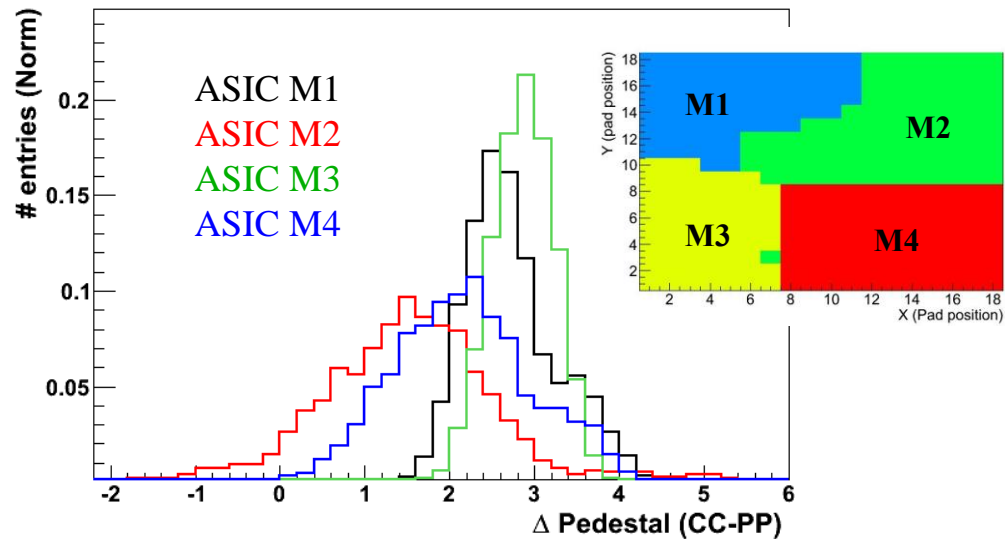
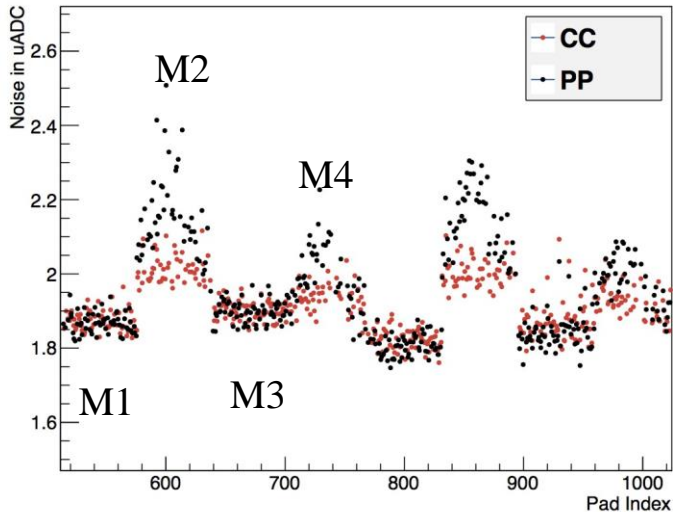


- Stable pedestal after around 600 μs.
- Time constant of pedestal ~100 μs.
- Time dependence of pedestal width is also ~100 us.
- It can be solved by changing FPGA firmware setting.

Power pulsing – Pedestal analysis



Noise for all the Pad of the detector

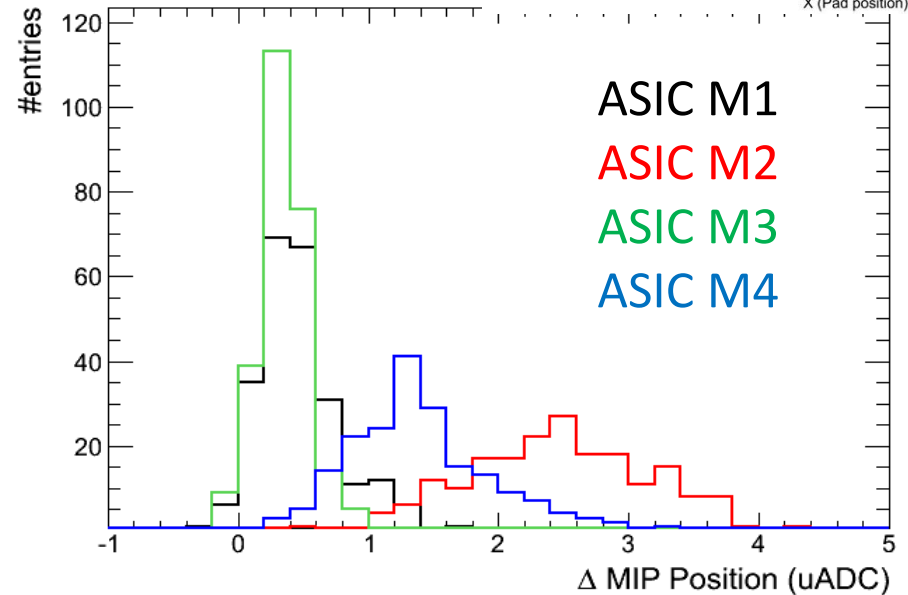
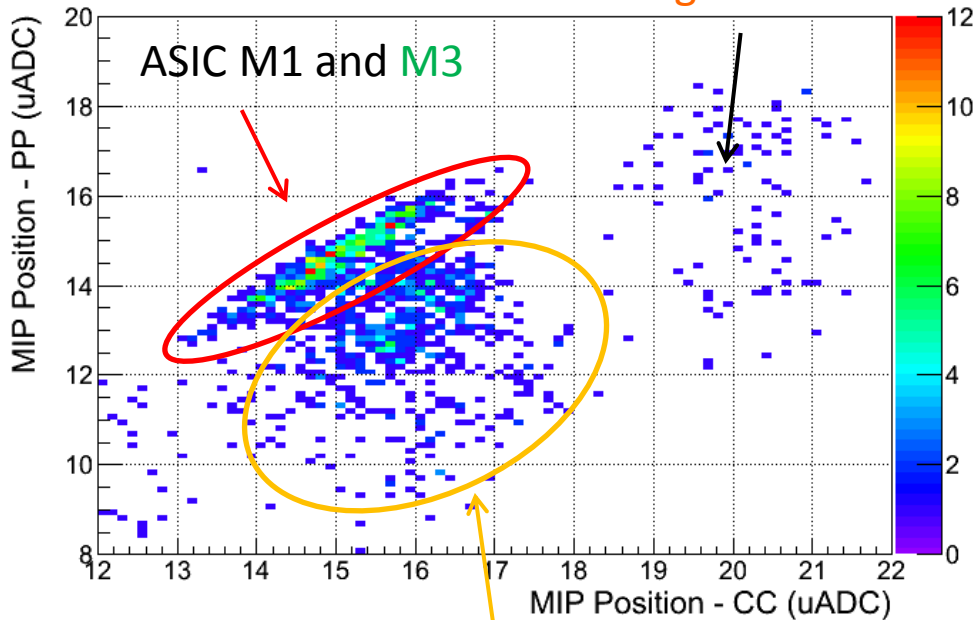
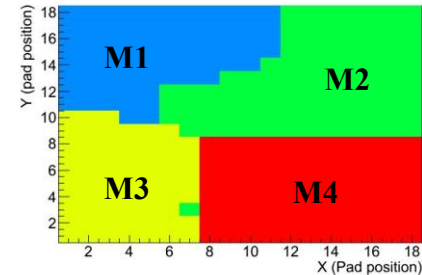


Clear pattern for ASICs M1, M3
 Pedestal shift of $\sim 1\%$ in PP mode
 Pedestal width constant
 Less clear situation for M2, M4
 PCB routing seems to distort
 pedestal spectra

Power pulsing – MIP analysis

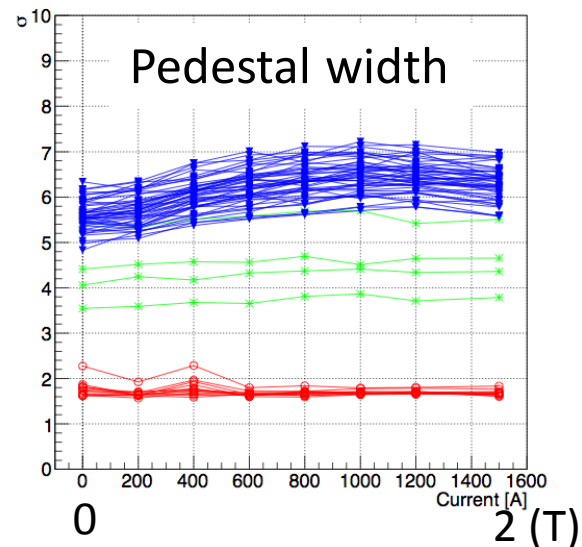
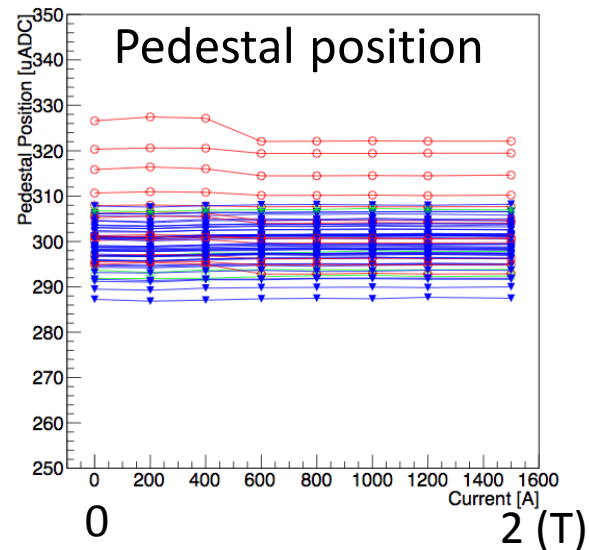
- Fit energy distribution: Landau convoluted with a Gaussian
- Sigma of the Gaussian is fixed to the noise

Trigger threshold
Too high



- ASIC M1 and M3 are ok under power pulsing operation.
- The activity of digital lines disrupts ASICs M2 and M4.

Power pulsing tests in magnetic field

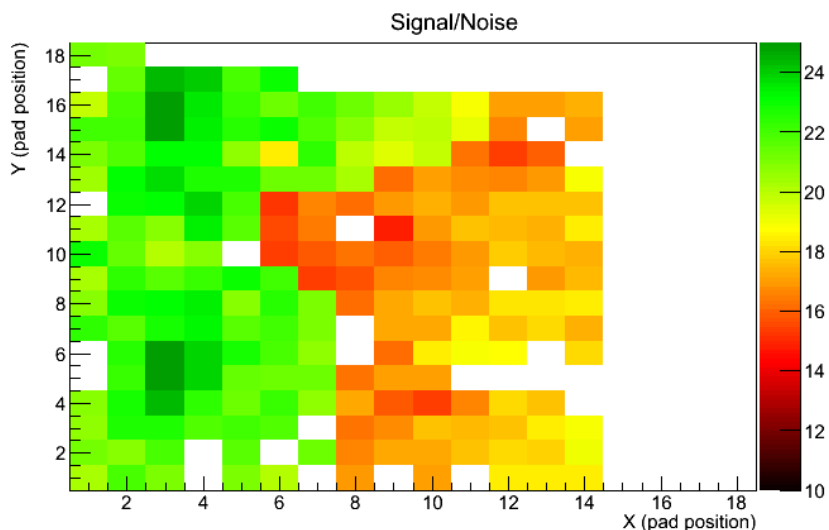


- Active channels are stable up to 2T B field

Conclusion and outlook

- 2013: We successfully operated tech. proto. in power pulsing mode and tested in 2T magnetic field.
- Two beam test with conservative design ASU
 - Detailed evaluation of performance of system
 - A number of observed odd behaviors were actually related to peripheral devices or non optimal power supply
 - Self-triggering ASICs require very careful power management
 - Active channels are stable up to 2T B field (pedestal study)
- Addressing now issues of a real calorimeter system
 - Large ASU : 16 ASICs par layer
 - Long Slab : 10 ASUs
 - Cooling
 - Test in strong B field

Data Analysis 2012 – Signal over Noise ratio



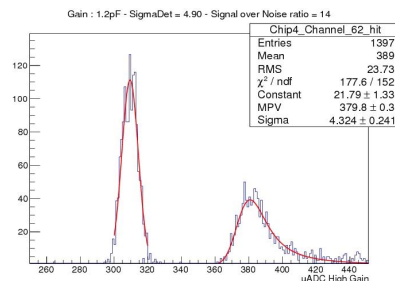
Results after setting of trigger thresholds and event filtering

White cells (noisy channel) : high threshold

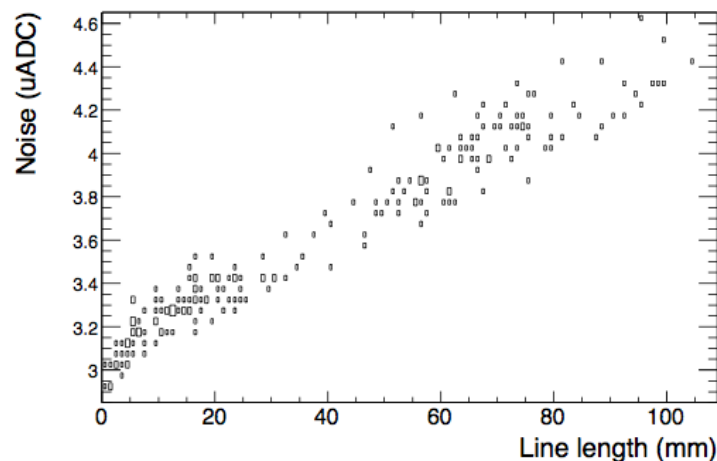
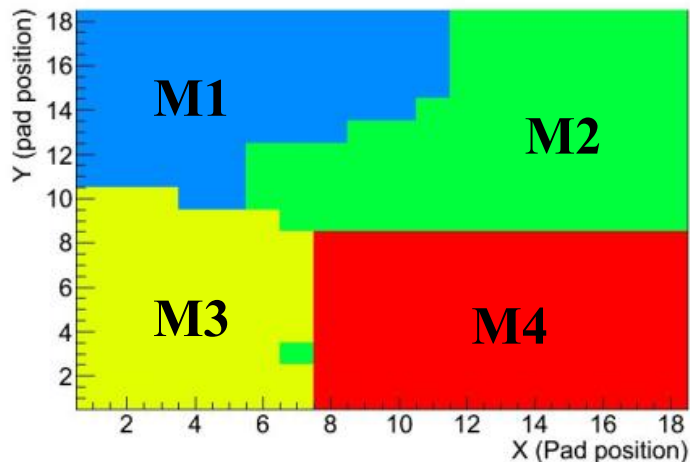
Correlation between noise and PCB routing

$S/N > 10$ (for all gains available with SKIROC2)

R&D target is S:N = 10:1

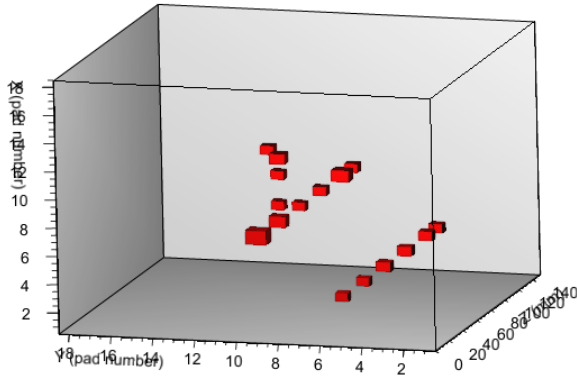


4 ASICs are mounted on a layer

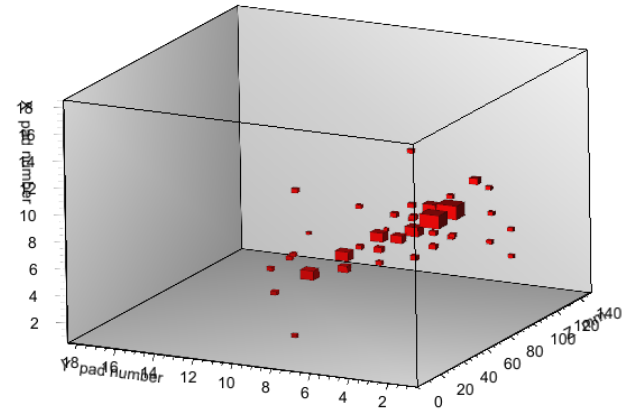


Event displays

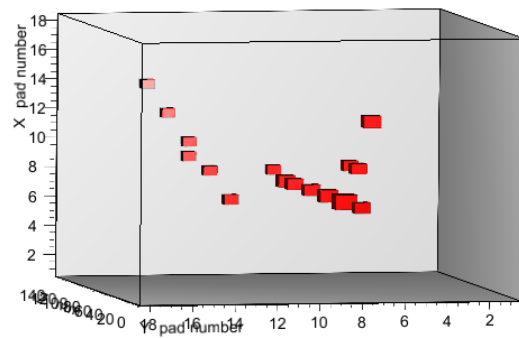
2 e- (3 GeV, no tungsten)



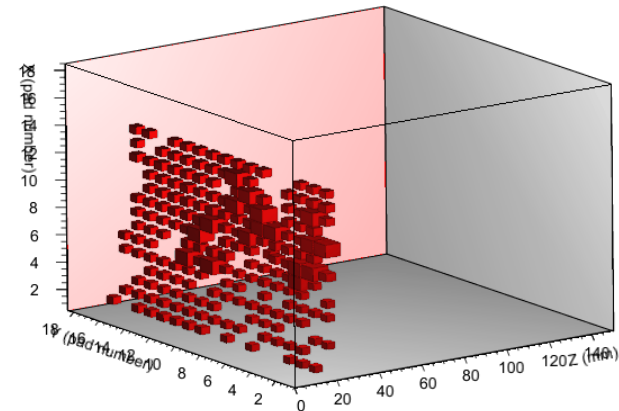
**1 e- (5 GeV)
5 W plates between layers**



**1 cosmic + 1 e-
(3 GeV, no tungsten)**

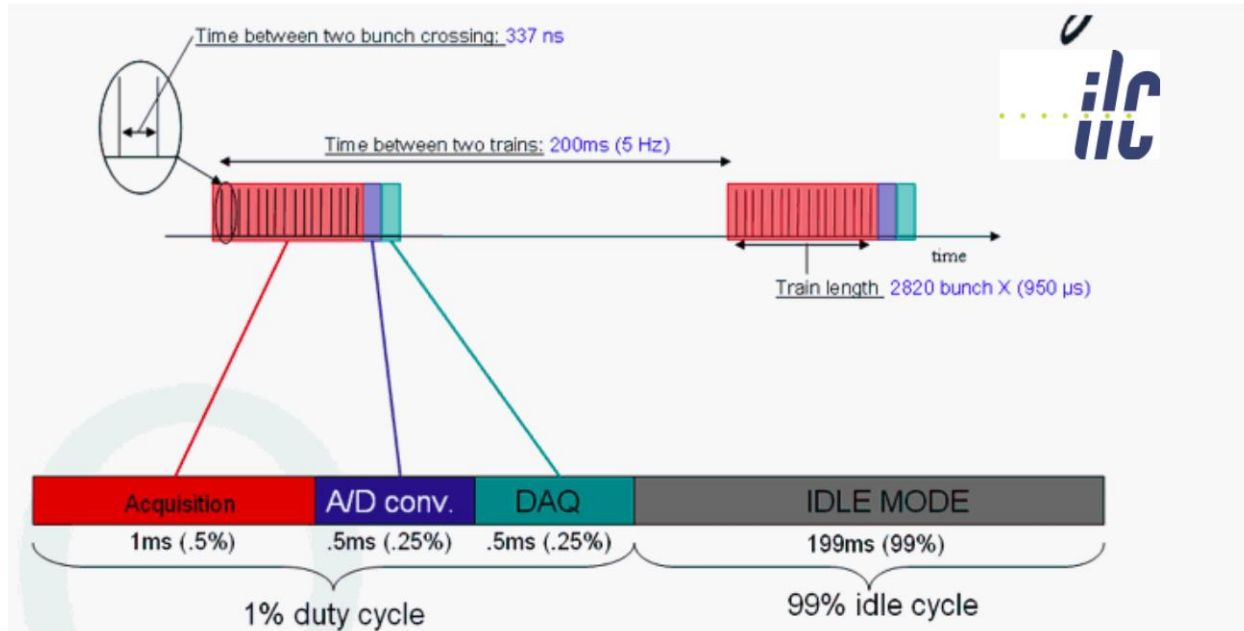


'Plane events???'



Observed in 2012 with significant frequency
can be remedied by correct PreAmplifier reference

Power pulsing



N.B. Final numbers may vary

- Electronics switched on during $> \sim 1$ ms of ILC bunch train and data acquisition
- Bias currents shut down between bunch trains

Mastering of technology is essential for operation of ILC detectors

Calibration of ASICs

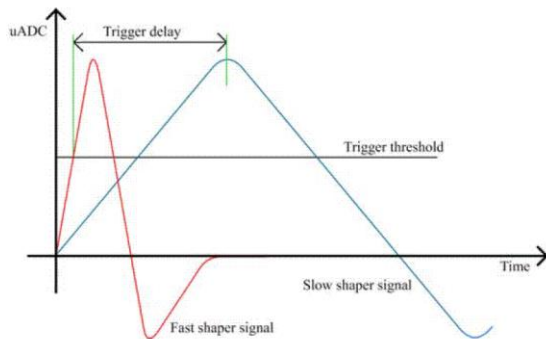
Establishment of calibration procedure for a larger number of cells

Trigger threshold

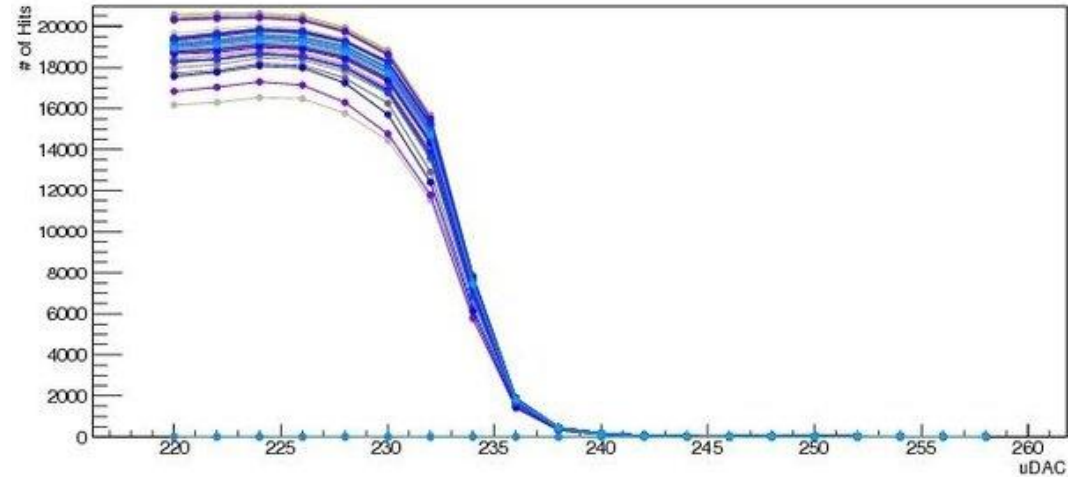
- depends on the gain

Trigger delay

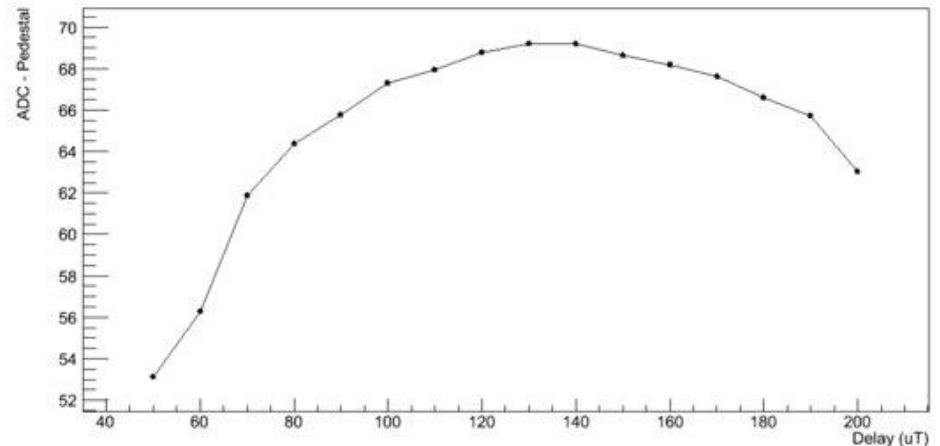
- depends on the trigger threshold



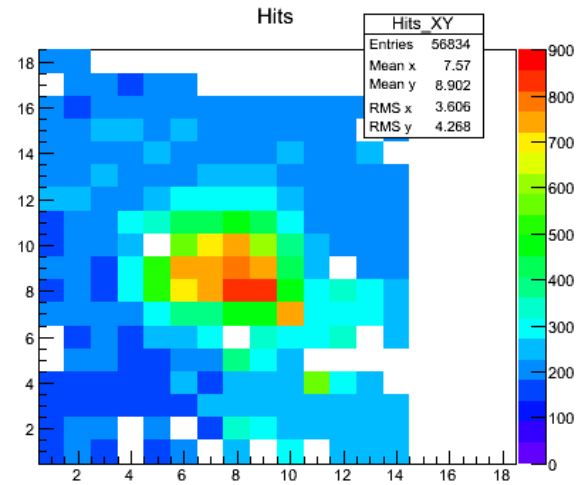
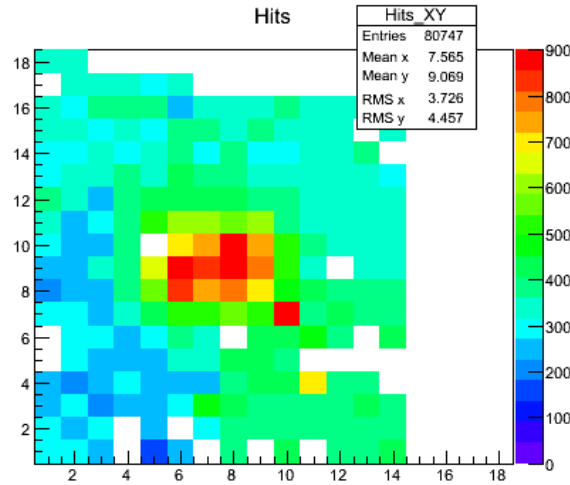
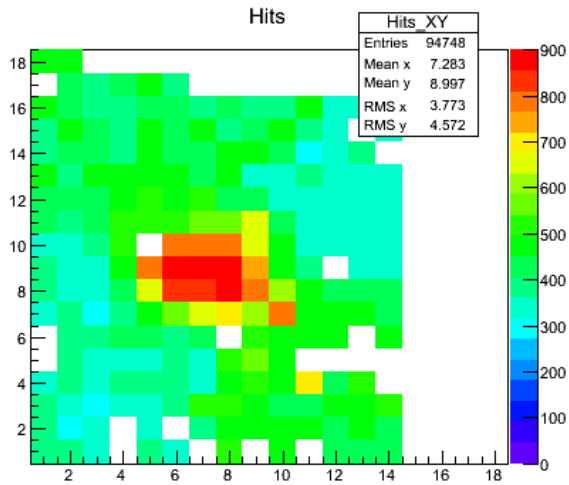
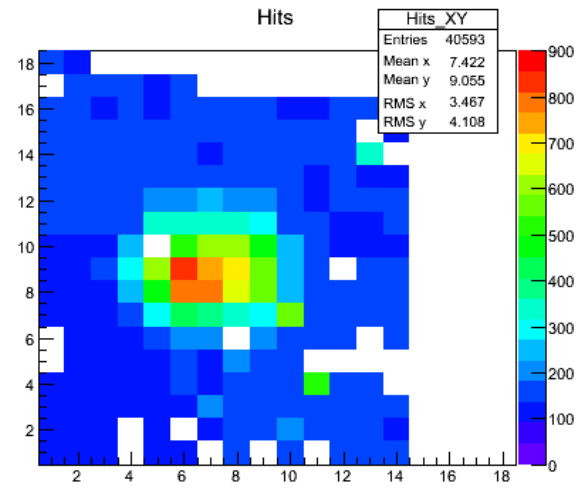
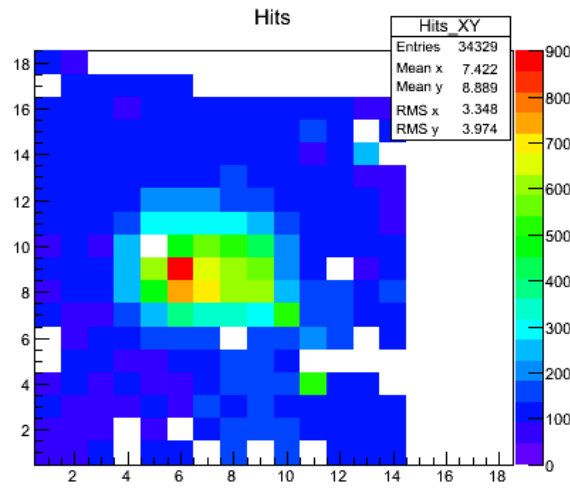
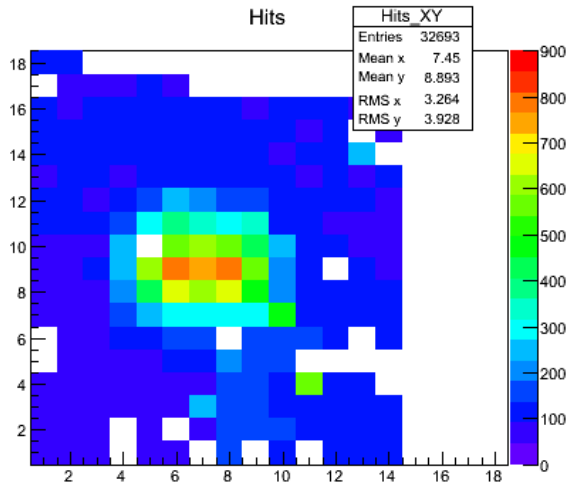
S-Curves for all the channels



Holdscan - All SCA - Pedestal corrected



Beam spot



Detection efficiency

Data: 3GeV – No W – XY scan

Total number of events: $2,3 \cdot 10^6$

Track selection:

At least 3 layers with hits

Linear fit of the e- track

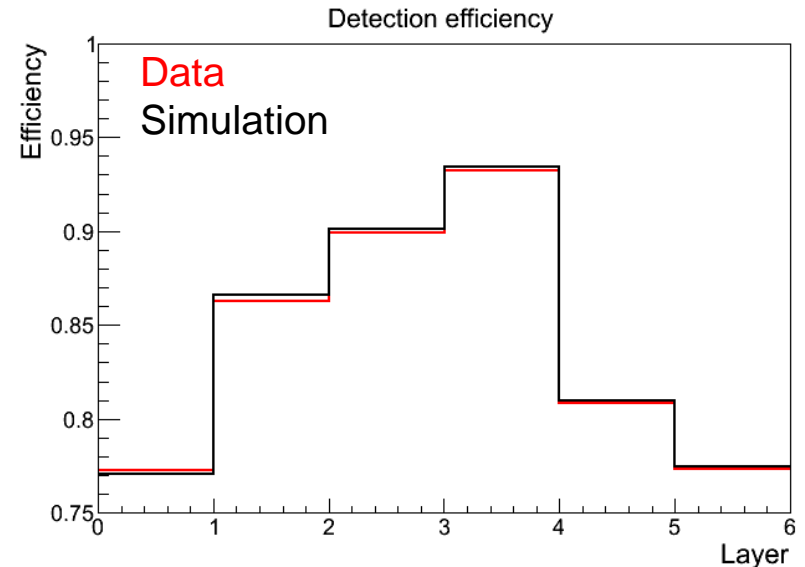
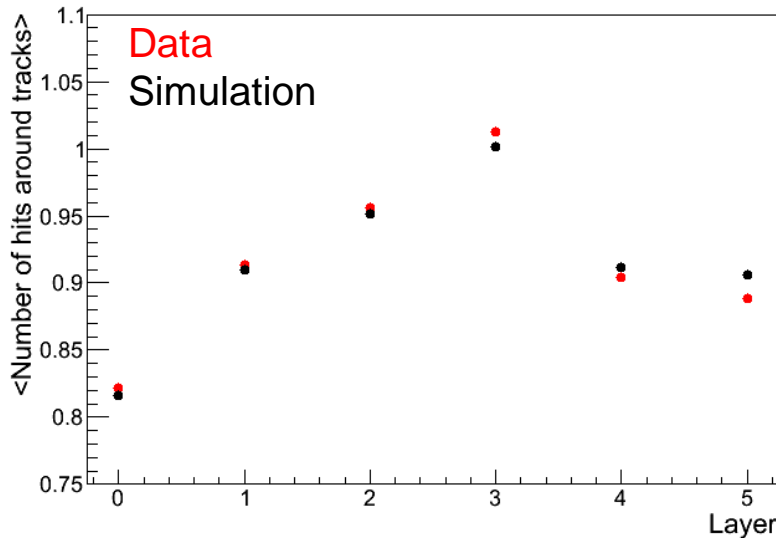
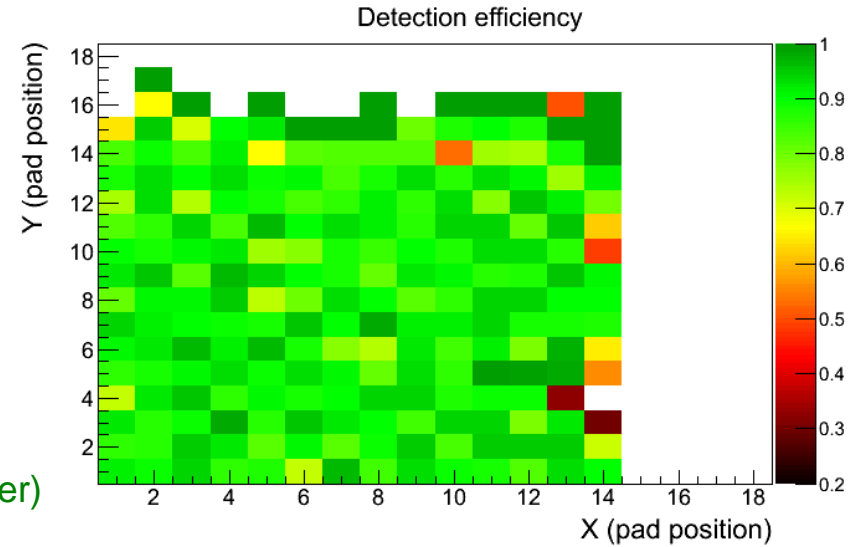
Nhits < 10

Inefficiencies due to:

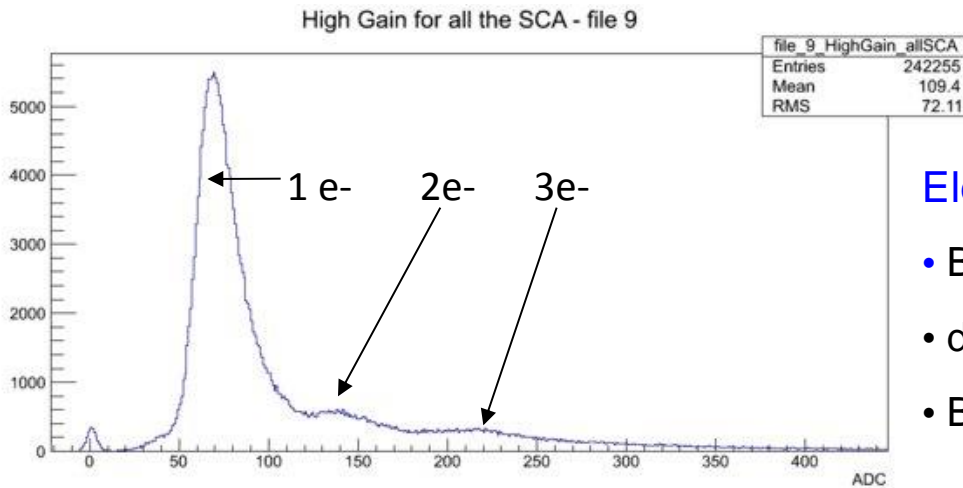
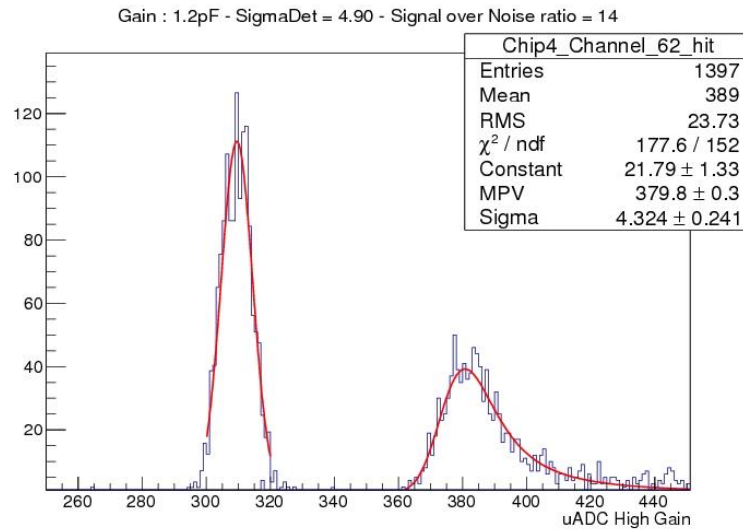
Switched off channels

Too high trigger thresholds (80%-95% of the MIP)

➔ Should be improved with the next test beam (December)



Energy measurement



Electron sources:

- Beam
 - delta rays
 - Bremsstrahlung
- + gamma conversion (2e-)
+ Compton

Energy calibration

Establishment of calibration procedure for a larger number of cells
Homogeneity of response (x,y scan of detector)

