TestBeam Activity of Scintillator ECAL Engineering Prototype

Annual meeting
17 / 12 / 2013 @ KEK
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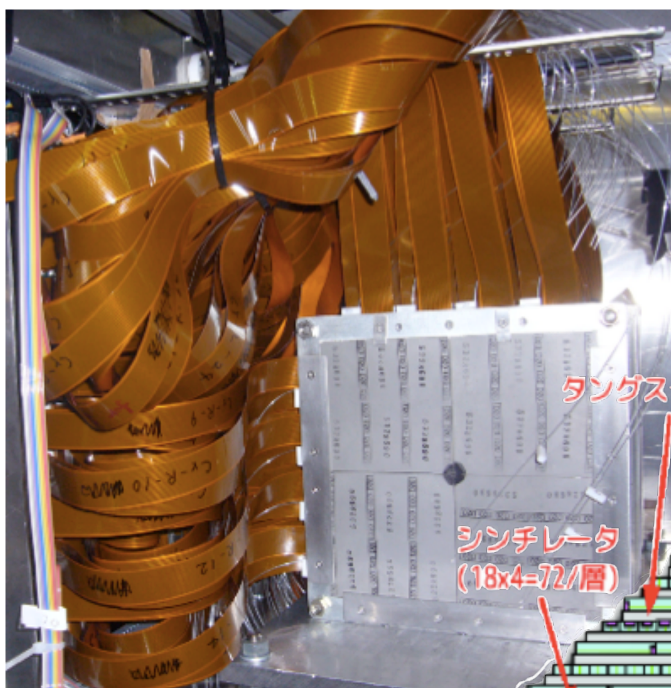
Motivation of Developing Electronics for ScECAL.

- ScECAL Physics Prototype has been studied at FNAL 2008 and 2009, and shown good performance

- ScECAL group is at stage of development of the readout electronics to match it with the ILD ECAL module thickness.

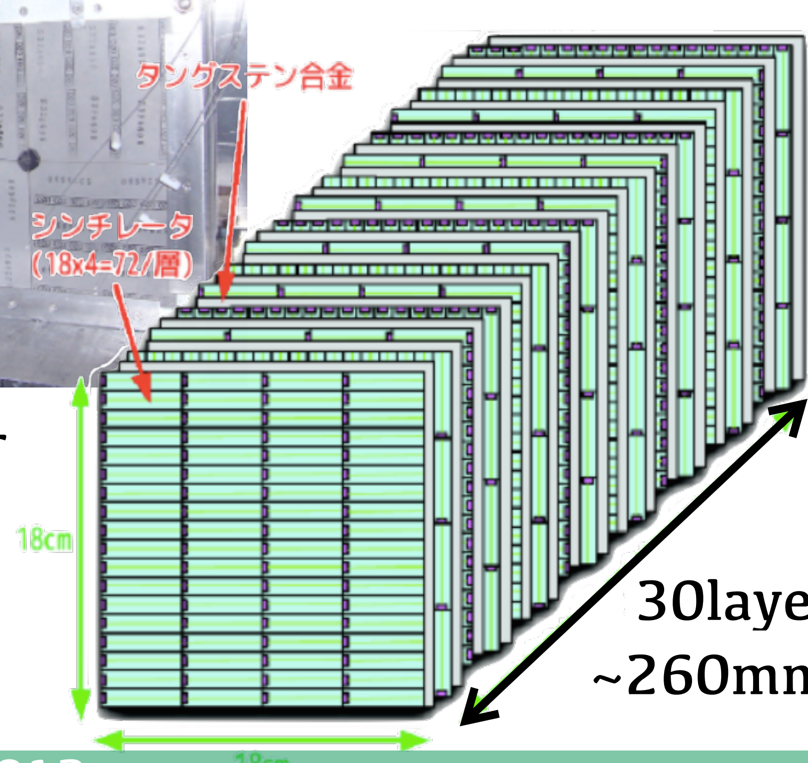
    - to put 30 layers within ECAL thickness ~1850mm.

    - to fully integrate into active layers 10 million channels on ScECAL electronics.



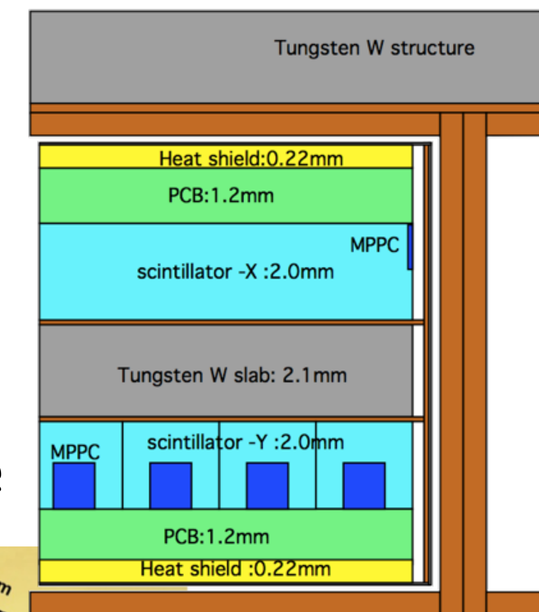
2009 FNAL BT

Physics Prototype

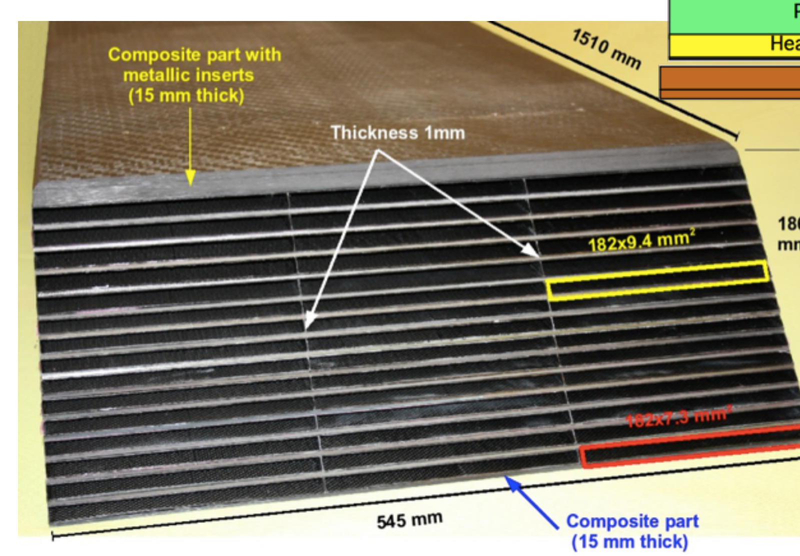


30layers
~260mm

Engineering Prototype



ECAL alveolar structure



30layers
~185mm

Developing Electronics for ScECAL.

- ScECAL group and DESY AHCAL people has developed the electronics "EBU" which a readout chip is embedded at, based on AHCAL electronics "HBU".

- About "EBU"

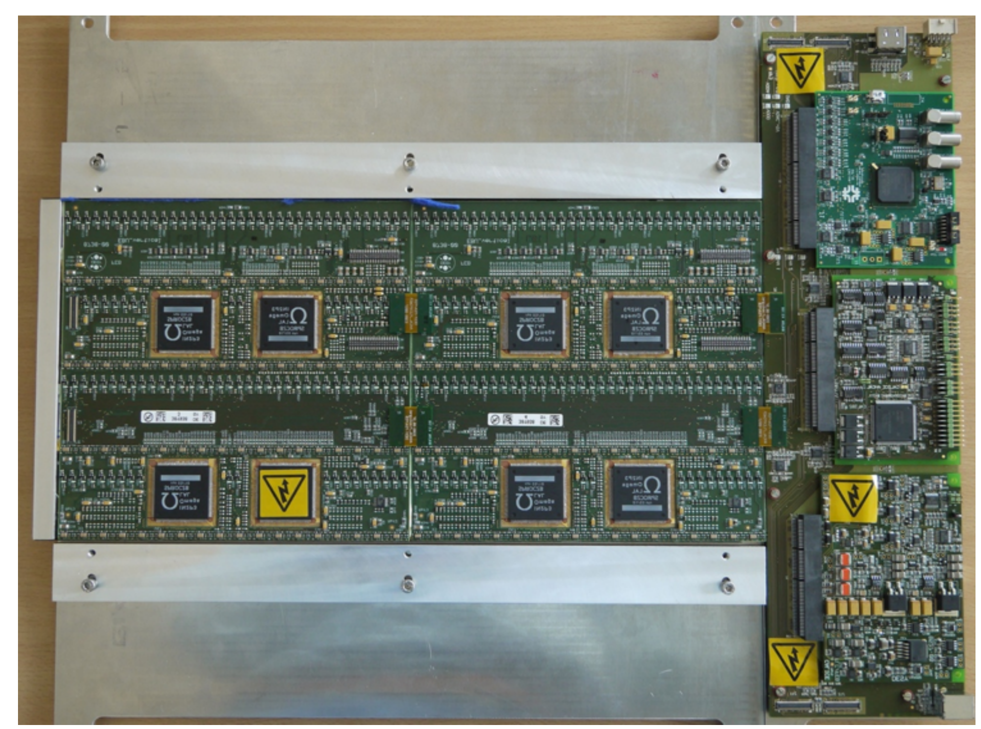
  - is embedded four readout chips "SPIROC" at one EBU.
  - can readout for 144 channels at one EBU.
  - is equipped LEDs for each channel to gain calibration.
  - is quarter the size of HBU.

- Same technology is used for both electronics.

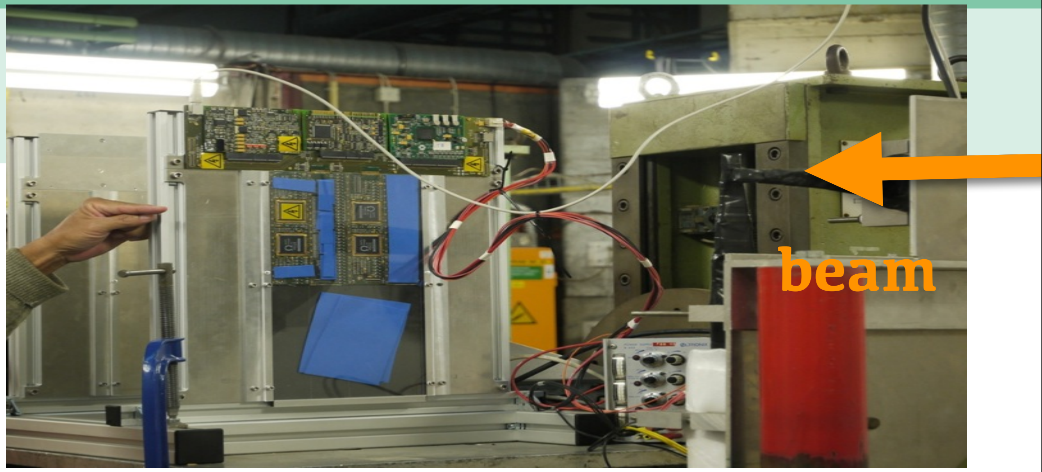
  - Synchronized data taking from EBU and HBU is expected to be achievable.

AHCAL layer : HBU(36cmx36cm)

ScECAL layer : EBU(18cmx18cm)

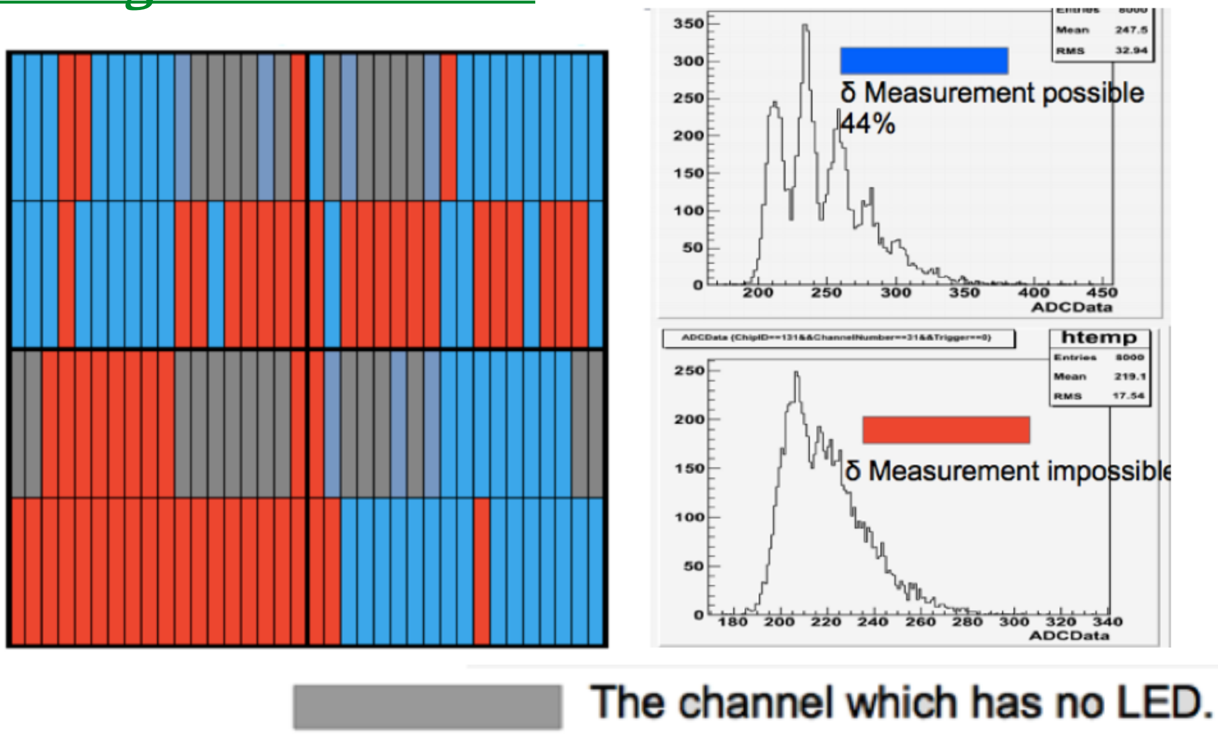


First TestBeam 2012 Oct.



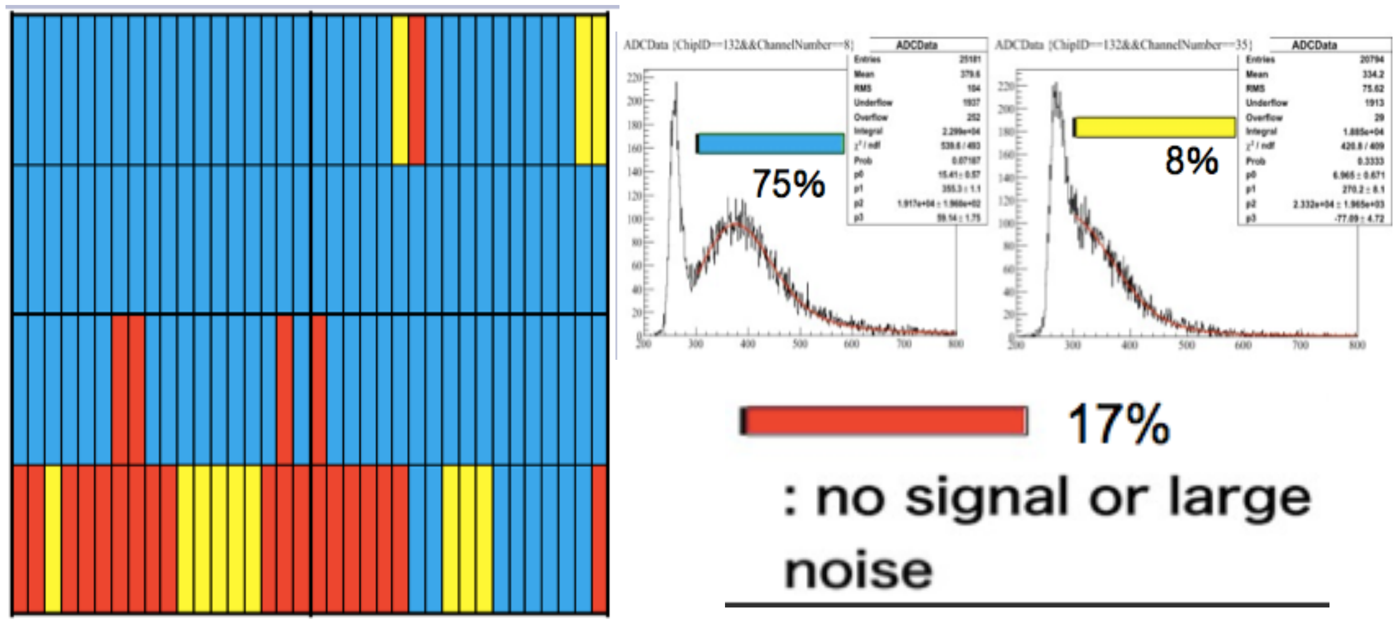
- Using one prototype of EBU on one layer,
  first TestBeam was held on 2012 Oct.

LED gain calibration



- Succeeded 50% out of 112ch,
  and 50% of channels had problems.

MIP calibration

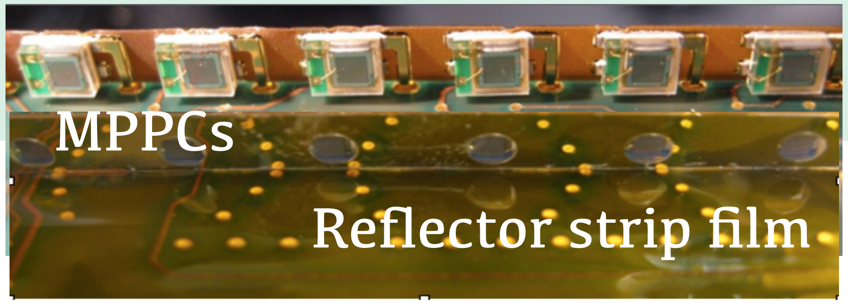


- 108(75%) channels out of 144ch could be measured MIPs.
- 25% of channels had problems

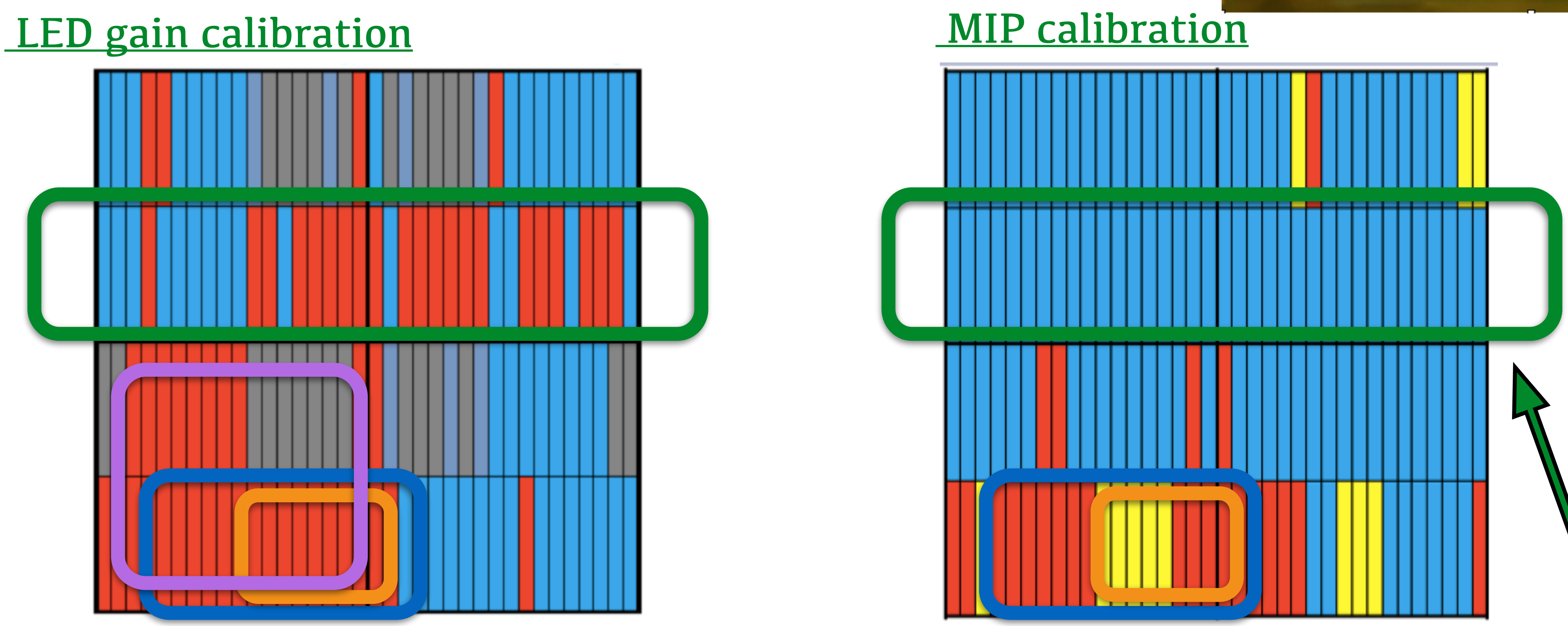
One professor said at last annual meeting,

- We can not use such almost bad electronics as the ILD ECAL.
  You must clear the reason.

First TestBeam 2012 Oct.



- The reasons of some bad channels.



- 1. Some channels of bias voltage provided to the MPPCs were too low.

  - For some channels preparation measurement of MPPC's break down voltage was insufficient. And input DAC voltage was very small.

- 2. Reflector strip film in front of MPPCs probably touched some metals of the electronics of the EBU,and made problems.

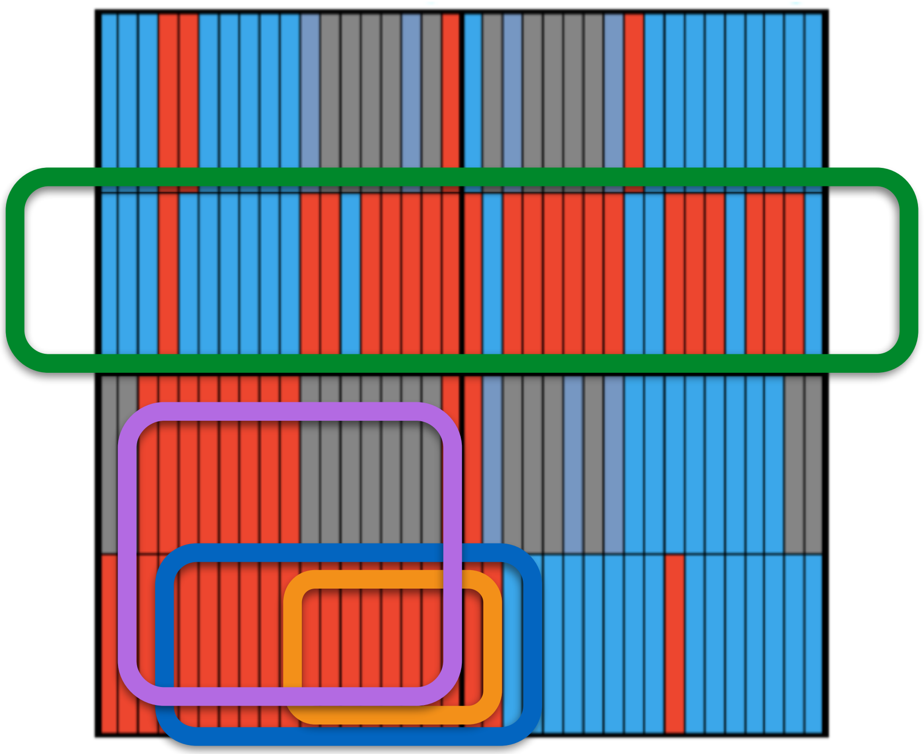
  - Took scintillators off and attached it once again, they turned blue.

  - But did not have time to confirm with LED calibration mode.

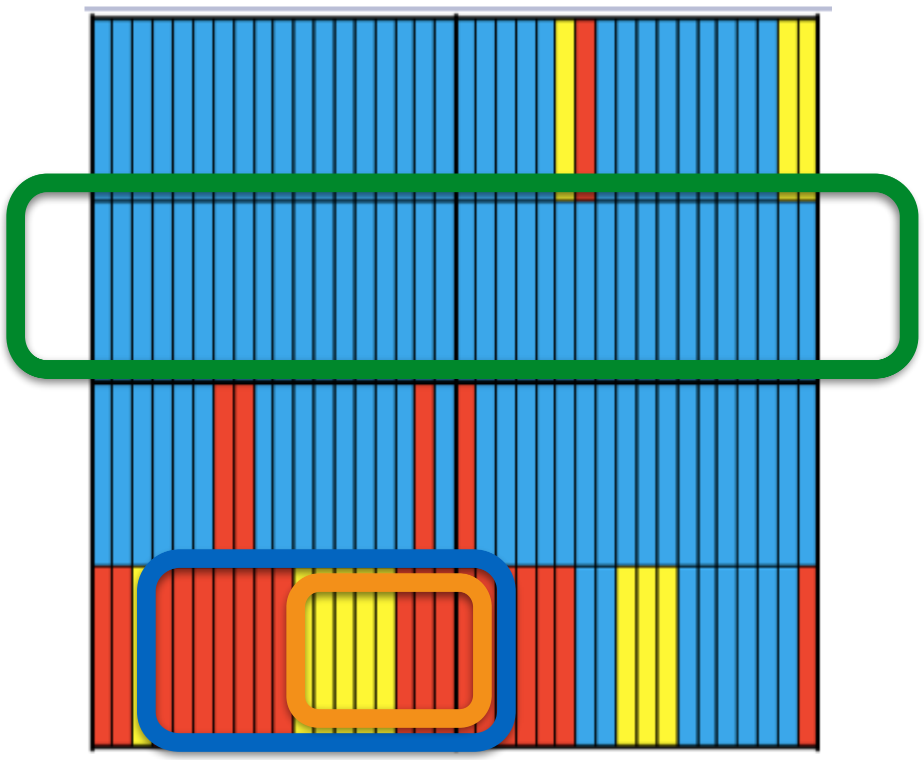
First TestBeam 2012 Oct.

- The reasons of some bad channels.

LED gain calibration



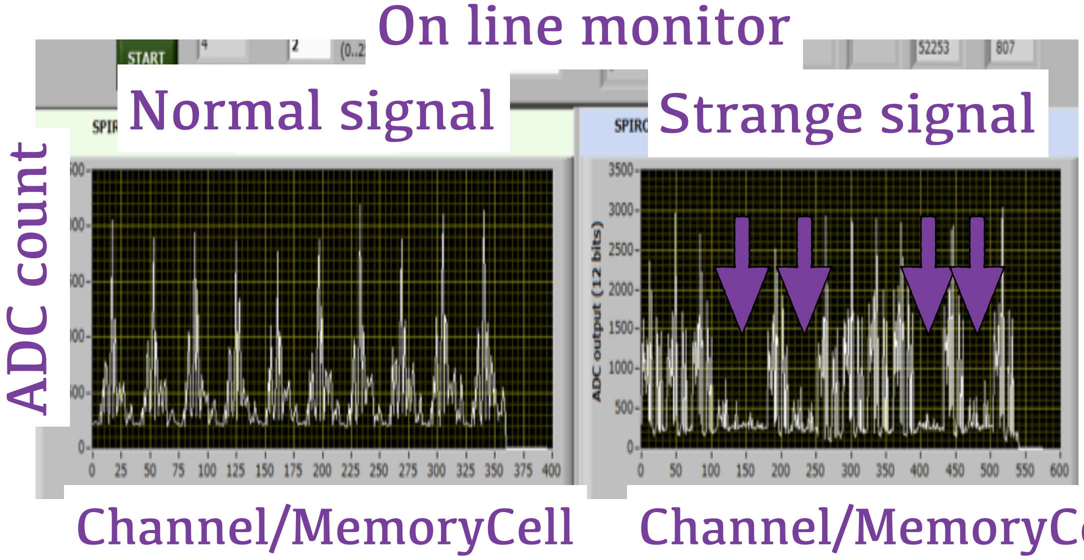
MIP calibration



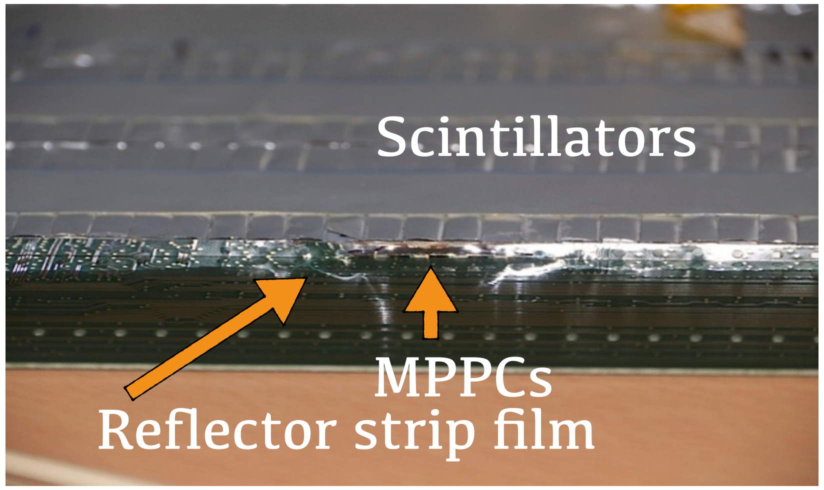
- 3. ▢ One controlled area of an ASIC has the problem on LED calibration mode.

- 4. ▢ The bending reflector strip film in front of MPPCs also made problems on the ASIC.

On line monitor



Signal lost in the middle of events and includes noise.



The Purpose of TestBeam 2013 July.

→ First Multi-EBU setup in a beam environment
(+HBU, +Si layer)

- Prepared two layers (Forward and Backward) .

  Forward layer consists of two EBUs (middle & terminal)

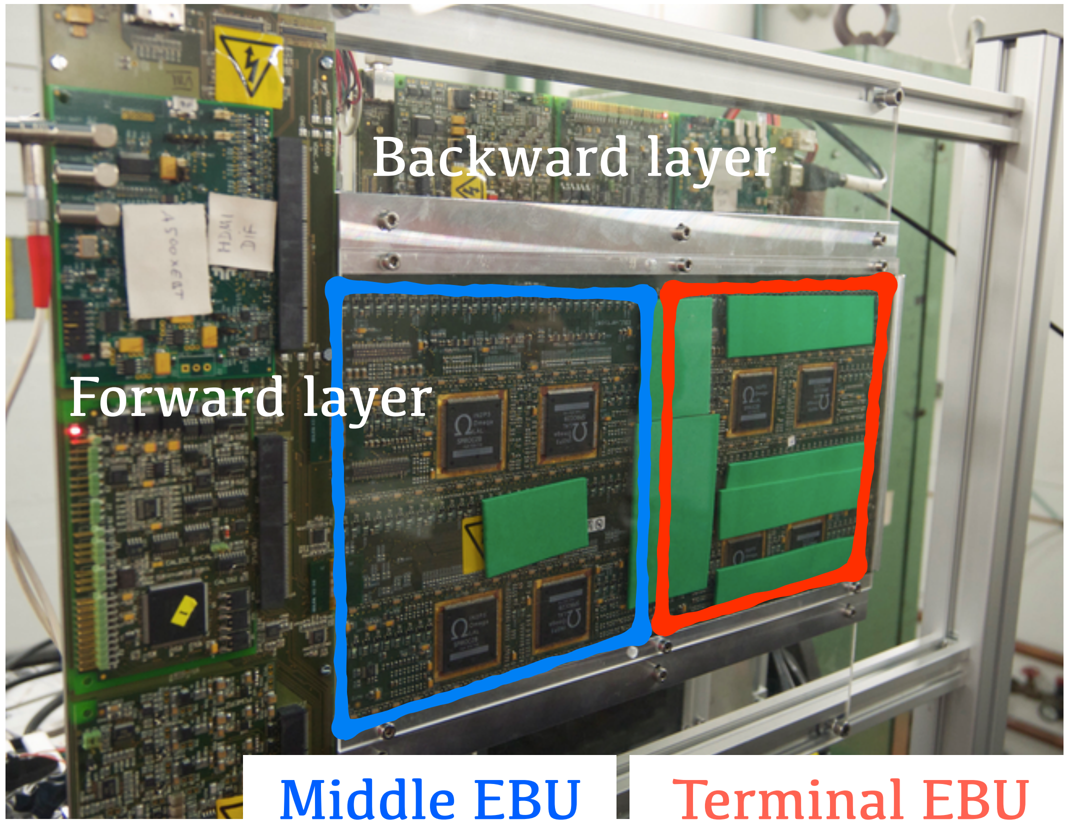
  Backward layer consists of one EBU.

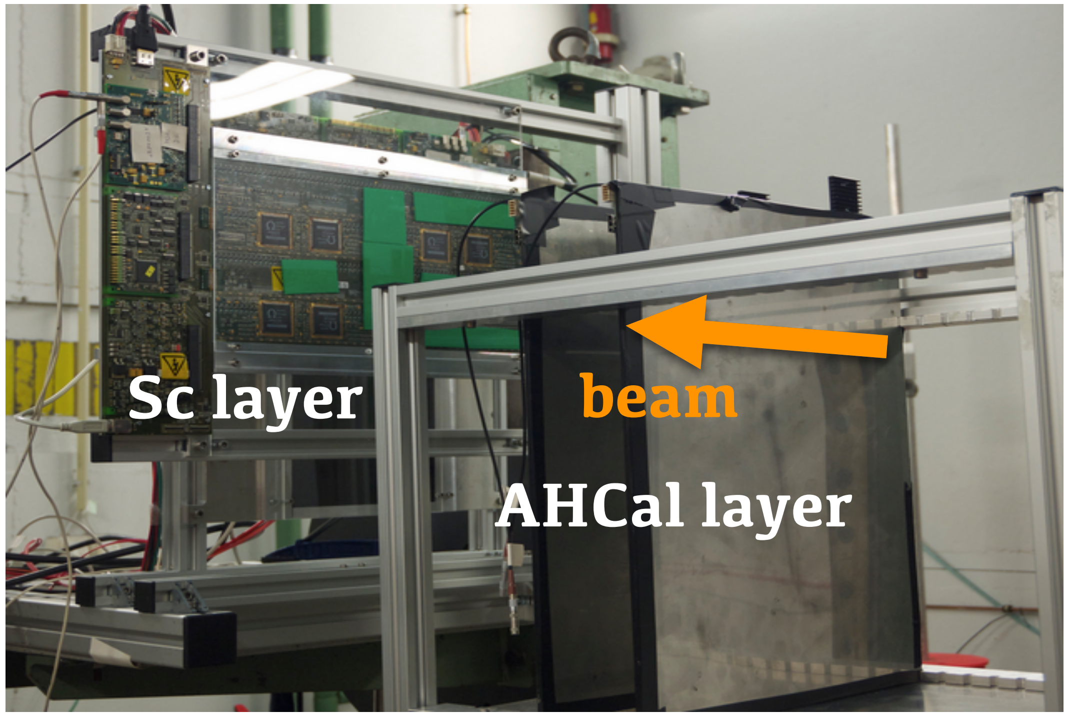
- Need to confirm.

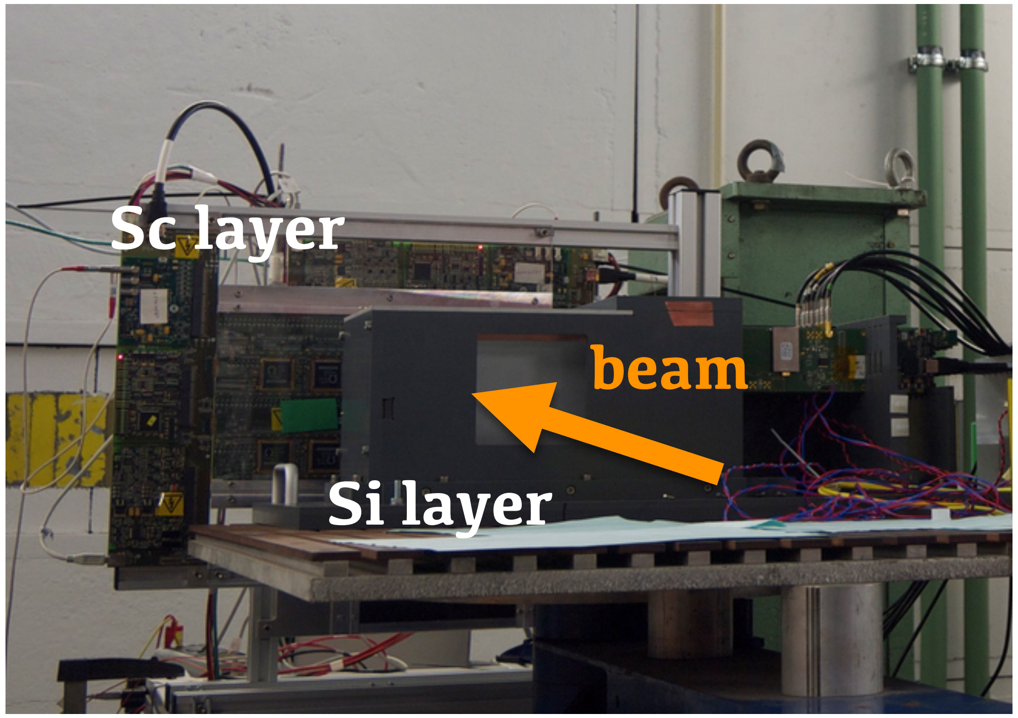
  - Can we make two layers three EBUs synchronize?

- Additionally

  - Can we make EBU synchronize with HBU?
  - Can we make EBU synchronize with SiECal for Hybrid?



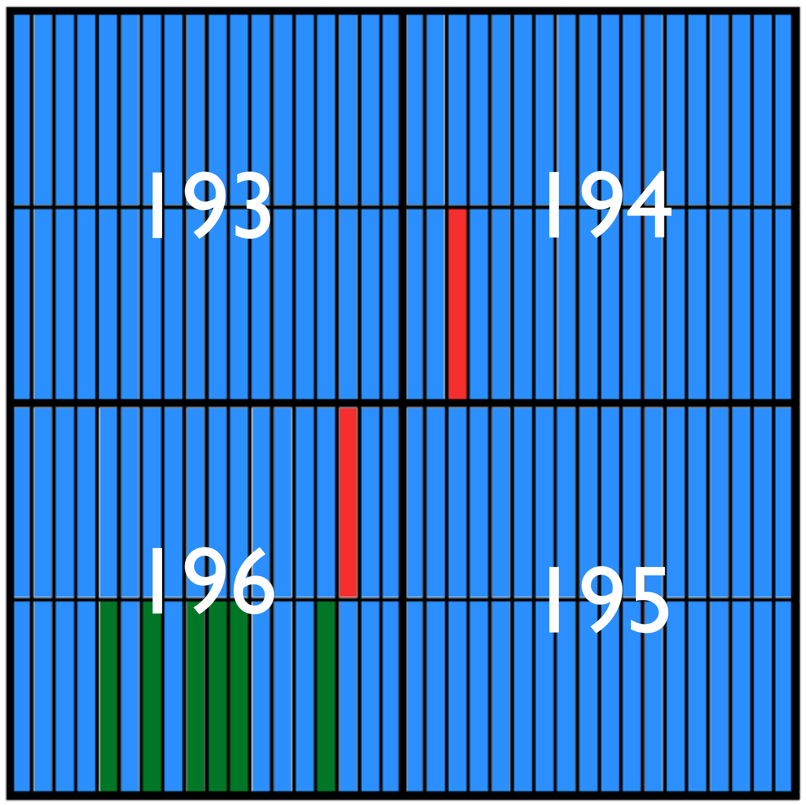




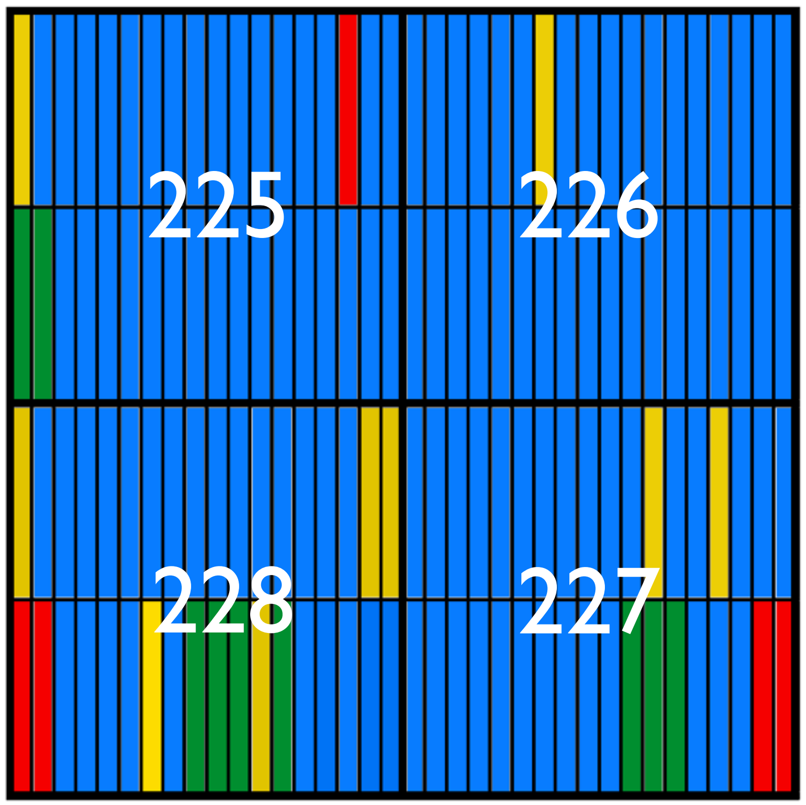
MIP Calibration.

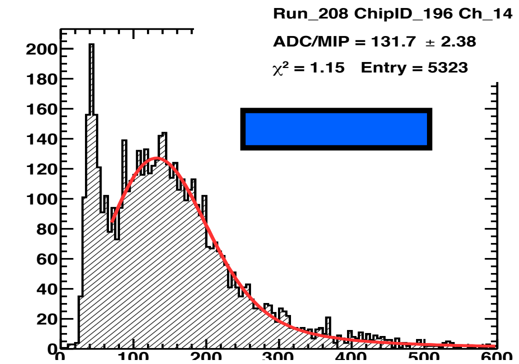
- Two EBUs on two layers were calibrated with 3GeV electron beam.
- Applied pedestal subtraction and fit with Landau-Gaussian to estimate ADC/MIP factor.

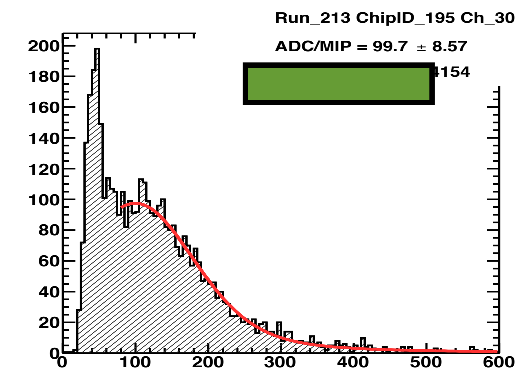
Forward layer result (NEW)

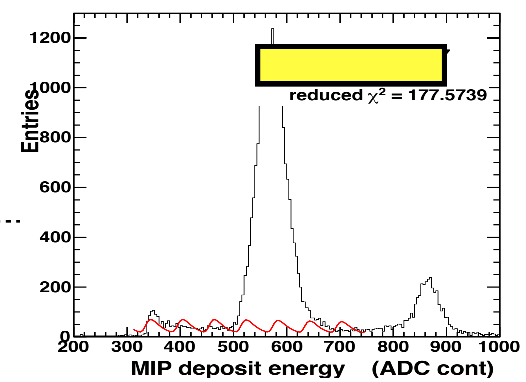


Backward layer result (employed 2012TB)









- MIP calibration result at DESY.

good MIP separation.

is difficult to separate MIP.

strange signal (noisy)

No signal

→ On forward layer, about 95% channels could be calibrated (only blue channels).

→ On backward layer, about 84% channels could be calibrated (only blue channels).

MIP Calibration.

- ADC/MIP conversion factor ※ Include only blue channels.

On forward layer

average of ADC/MIP factor = 115.6 ADC

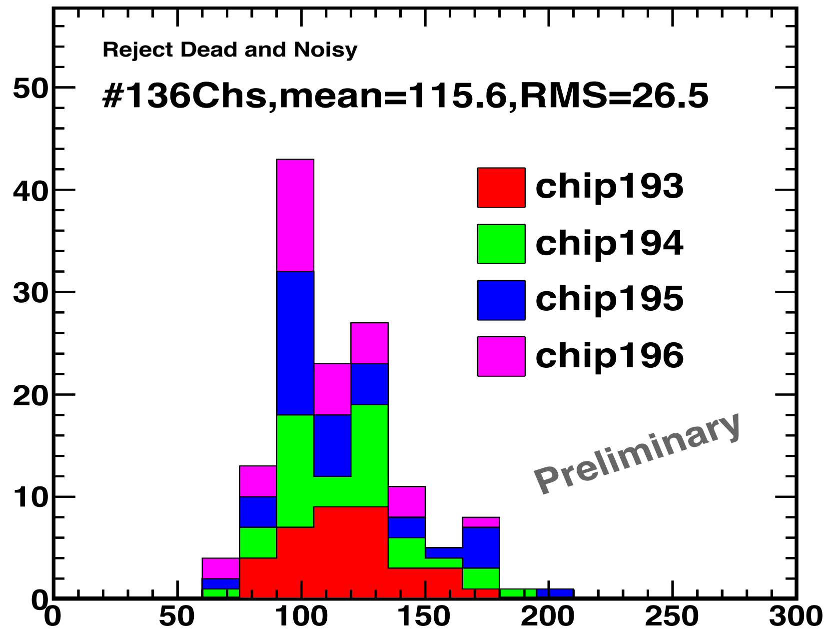
RMS/Mean = 22.9%

On backward layer

average of ADC/MIP factor = 159.7 ADC

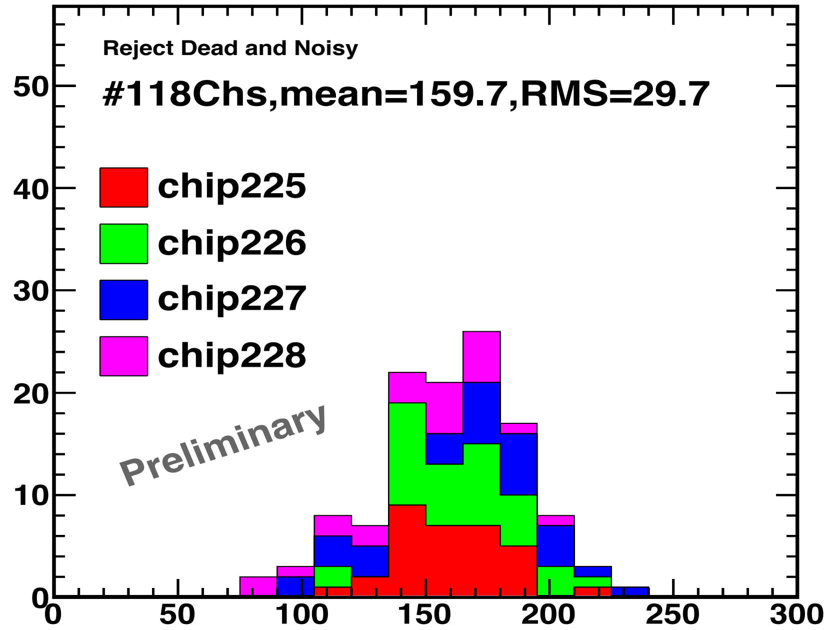
RMS/Mean = 18.6%

Forward layer ADC/MIP



ADC/MIP conversion factor [ADC count]

Backward layer ADC/MIP



ADC/MIP conversion factor [ADC count]

- Average values are little bit different between both layer despite we intended to set the same bias voltage for each channel.

(set voltage ΔV = +3.0 from break down for all channels)

→ Need to clear the reason of this difference.

Deposit Energy on 5x5mm cells estimated by simple SSA.

- lateral EM shower shape.

  - We could observe the spread of shower according to the thickness of the absorbers.

  - Strip splitting algorithm also works well. And we could observe 5x5mm cell resolution.

※ Energy deposit on backward is smaller than on forward.

→ Small energy particles stop in forward layer and can't reach backward one.

- We compared the longitudinal shower shape.

  → We used 3 GeV electron.

- On physics prototype, max deposit occurred at 7 or 8 absorbers.

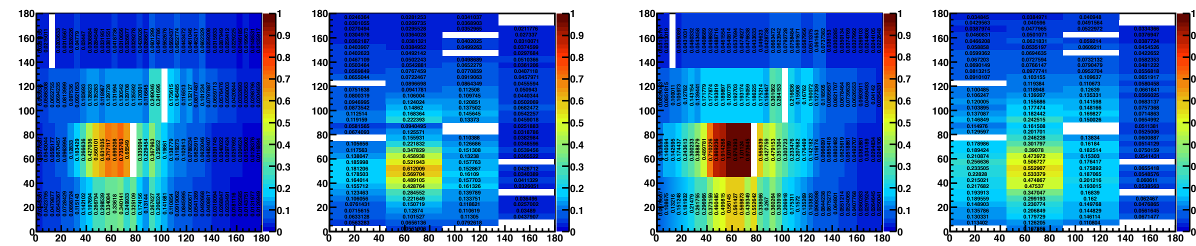
- On engineering prototype, max deposit occurred 6 or 7 absorbers.

→ For both case we do not reject noises and calibrate sufficiently.

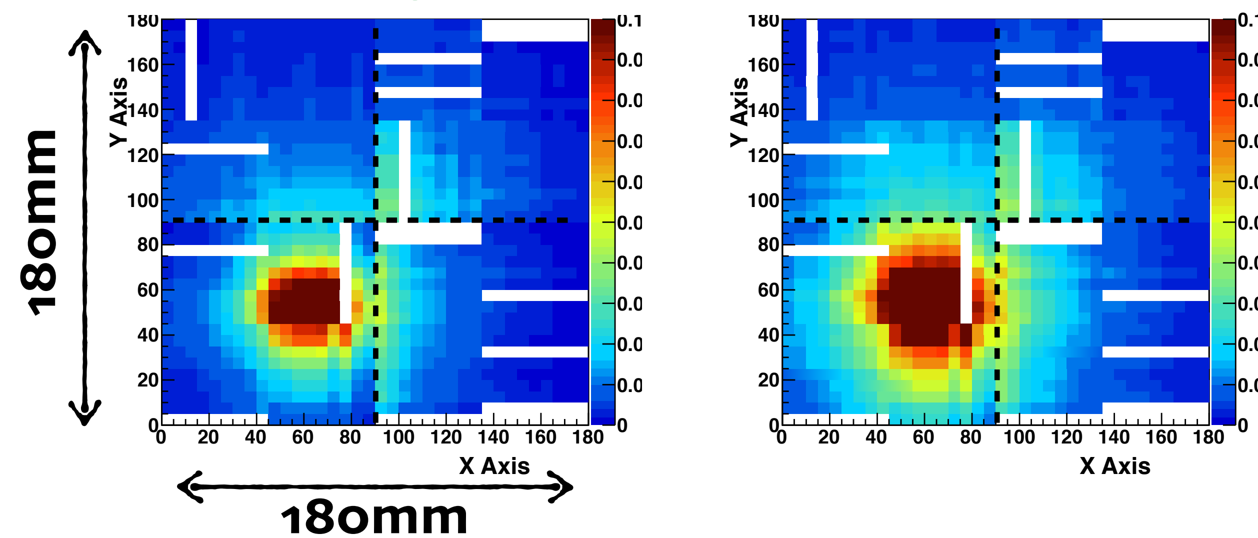
Tungsten x 2

Tungsten x 7

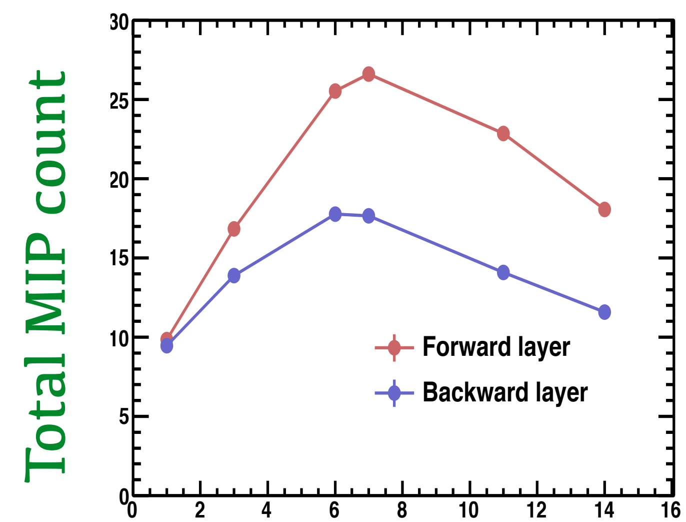
Forward layer & Backward layer



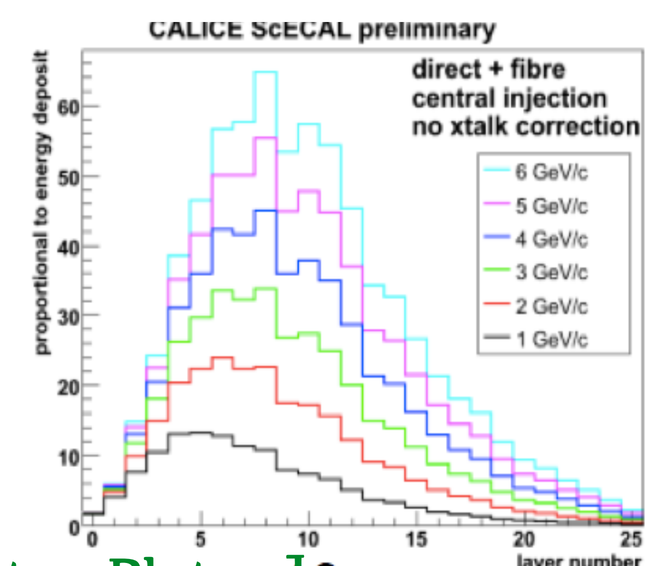
SSA on 2 layers



Engineering Prototype



Physics Prototype



[N of Tungsten Plates]

Hit Map with EBU/HBU Synchronized Data.

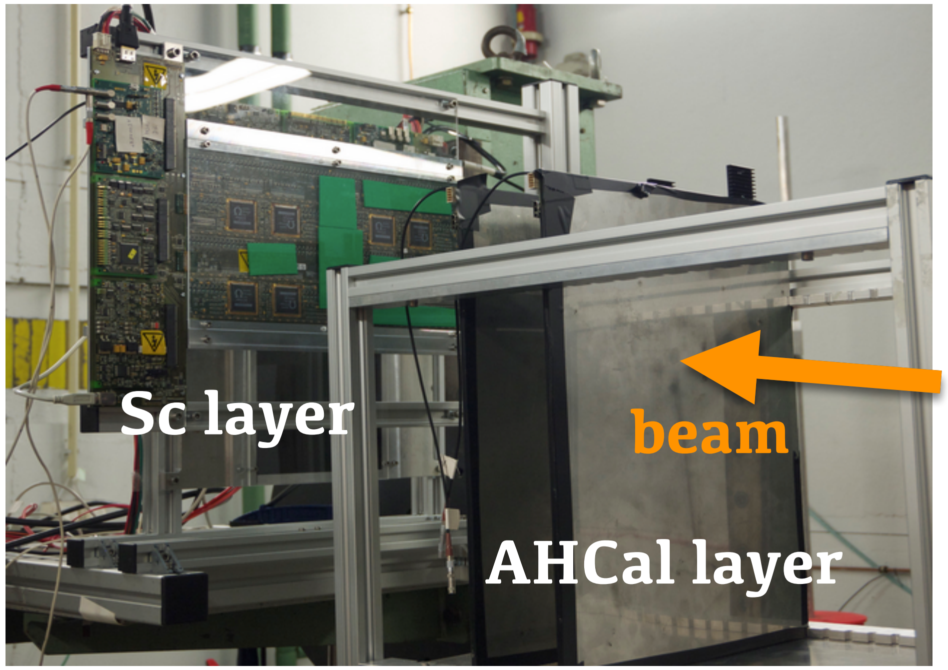
- Made EBU and HBU synchronize and plot the hit map.

- In case of 4 layers coincidence, we consider as being hit

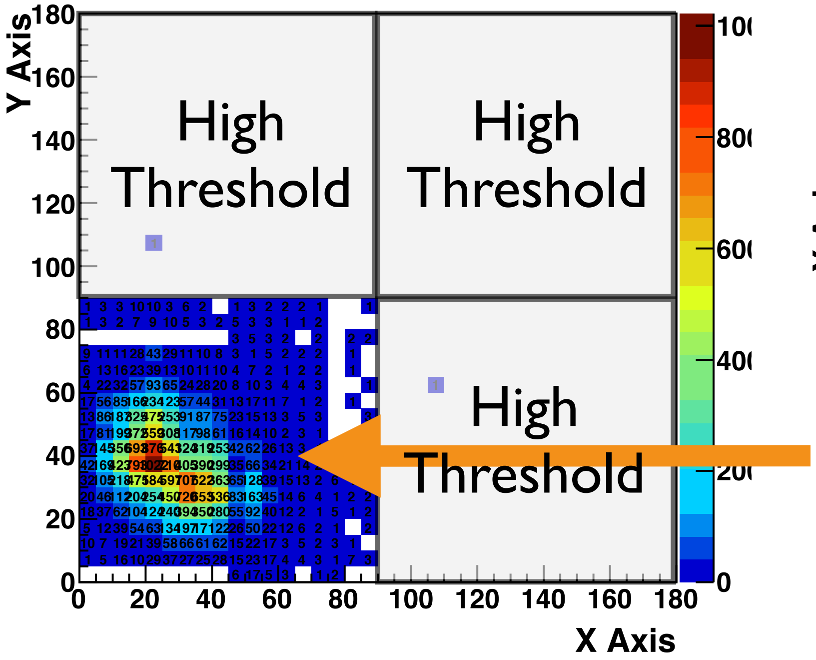
- A diagonal area of HBU were set at high threshold

  → Hits are concentrated in opposite diagonal area.

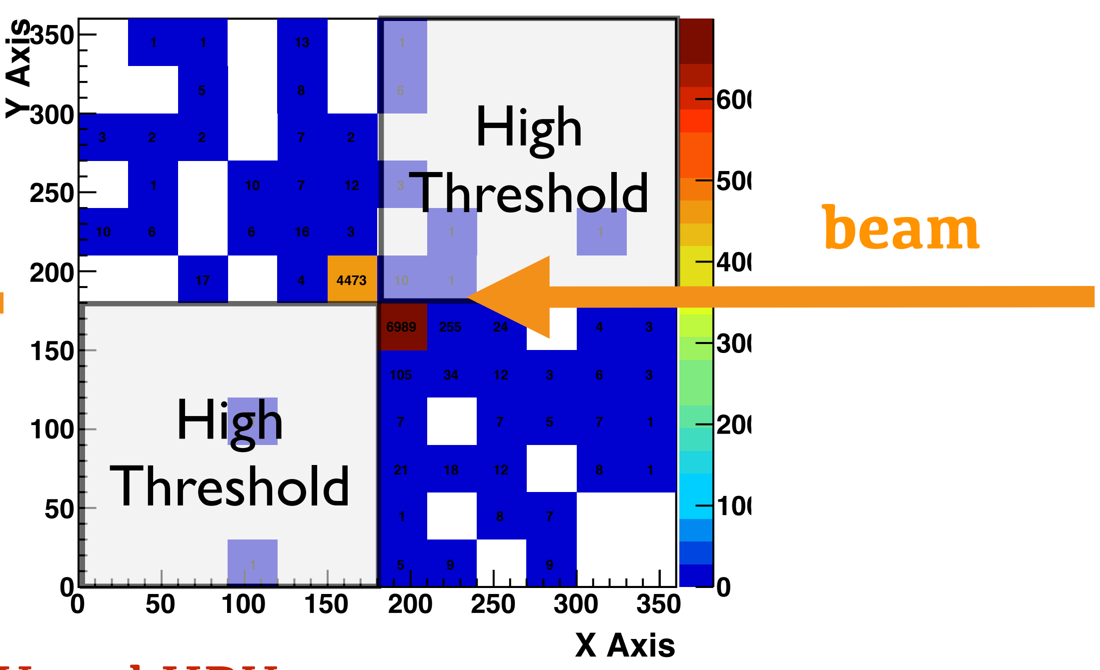
  → On EBU, hits are concentrated in same diagonal area with fine resolution.



Hit Map of EBU



Hit Map of HBU



→ We could observe correlation between EBU and HBU.

Summary & Outlook.

- Two ScECAL engineering prototype were tested at DESY with electron beam.

  → we could calibrate about 95% and 84% channels with MIP calibration on forward layer and backward layer respectively.

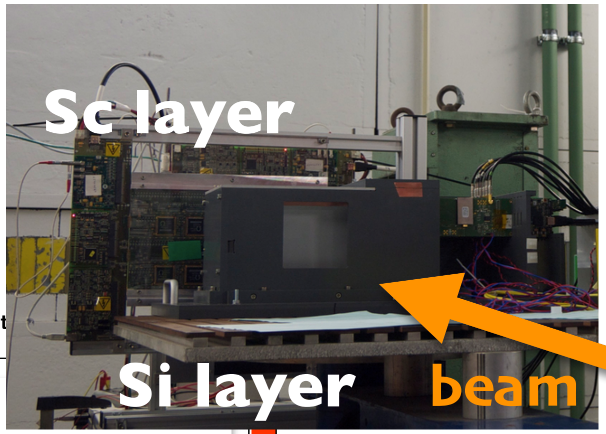
- SSA works well.

  → We could confirm SSA works well for the lateral shower shape, but need to reject noise properly.

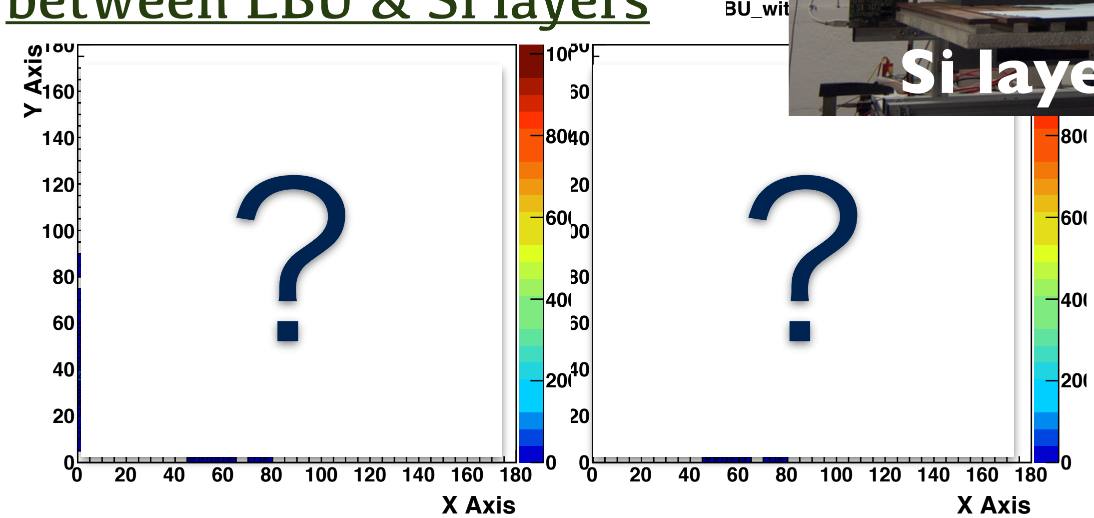
- Two ScECAL layers successfully worked with AHCAL layers in a "Real synchronization".

  → We could observe the correlation between EBU and HBU.

  → Next, We need to confirm the correlation between EBU and Si layers.



Synchronization between EBU & Si layers



- Outlook for hardware R&D

  - Check Power pulsing with EBU.

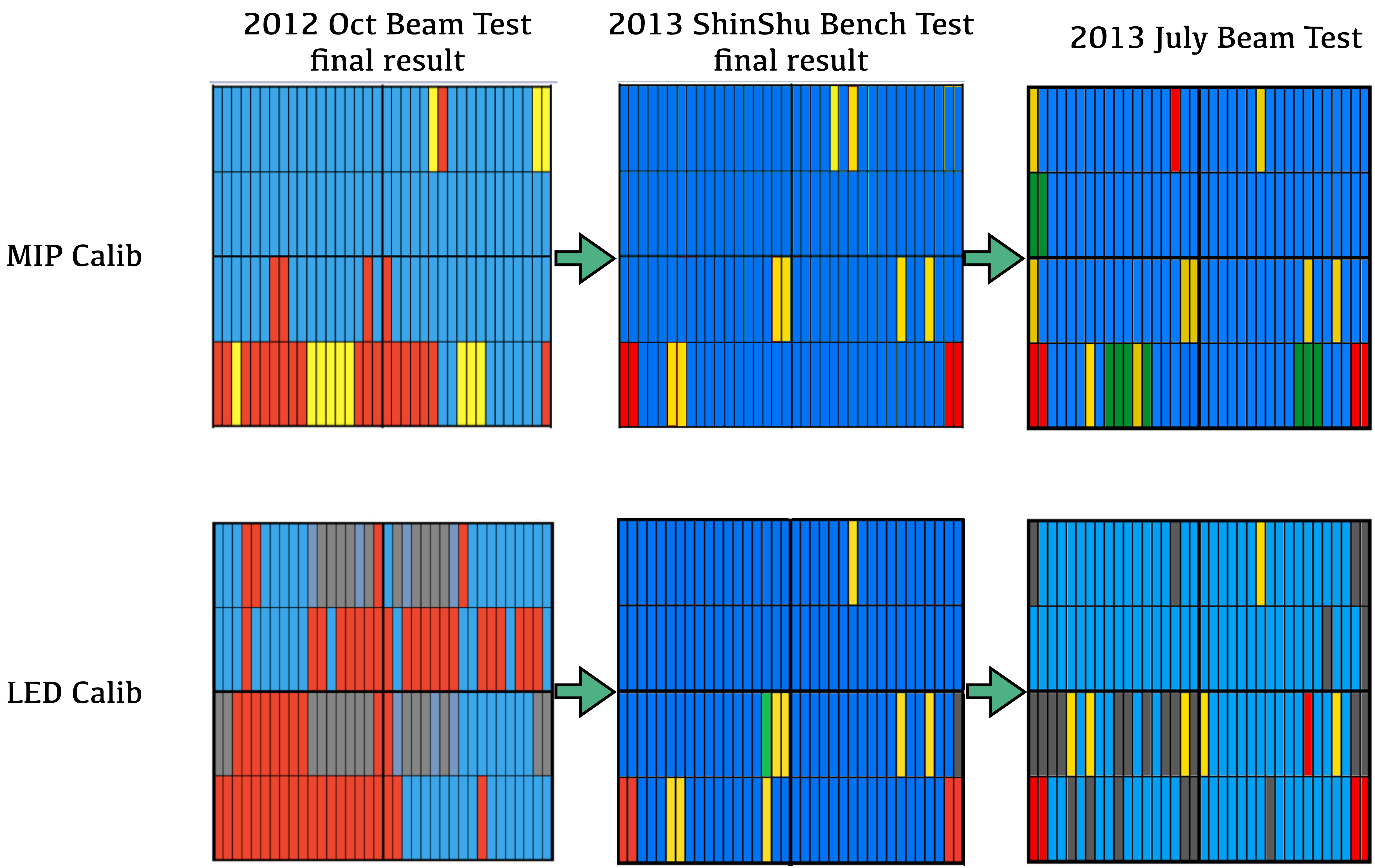
  - Check real SSA.

  - Real Si-Sc-ECAL synchronization

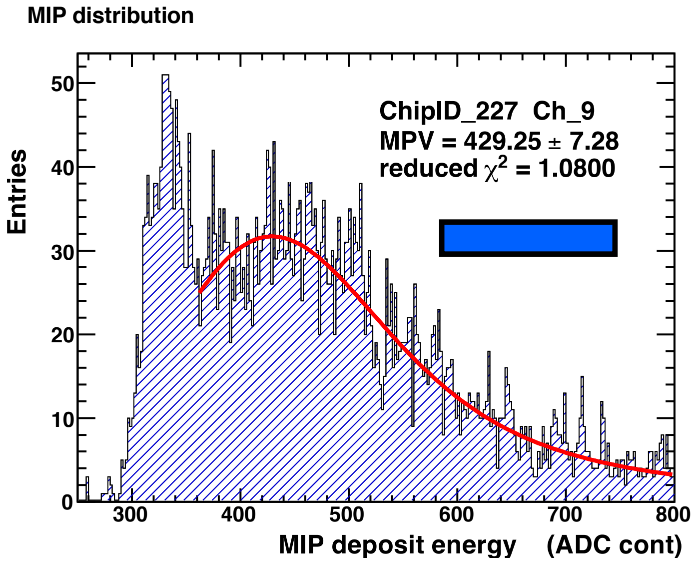
  - Synchronization with more layers (Si+Sc, Sc+AHCal, Si+Sc+AHCal)

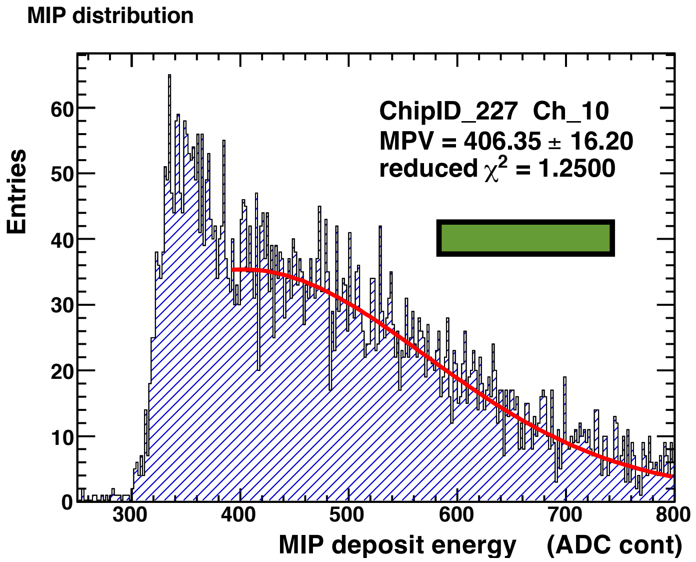
Back Up.

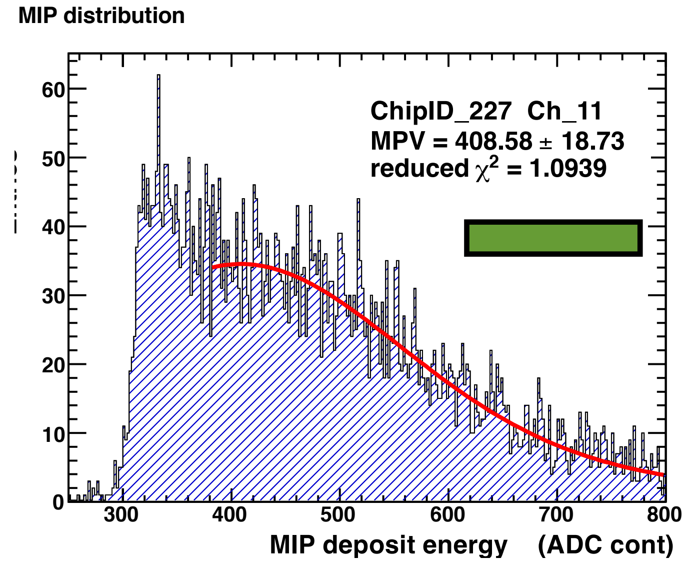
Transition of Backward Layer (employed 2012TB).

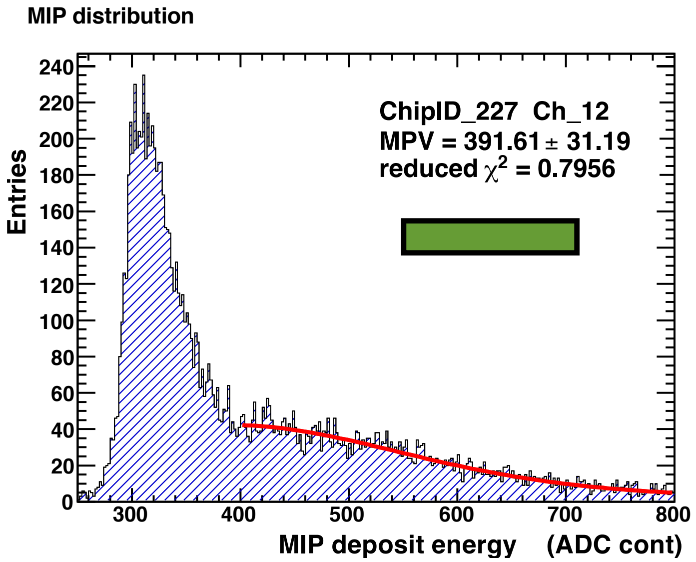


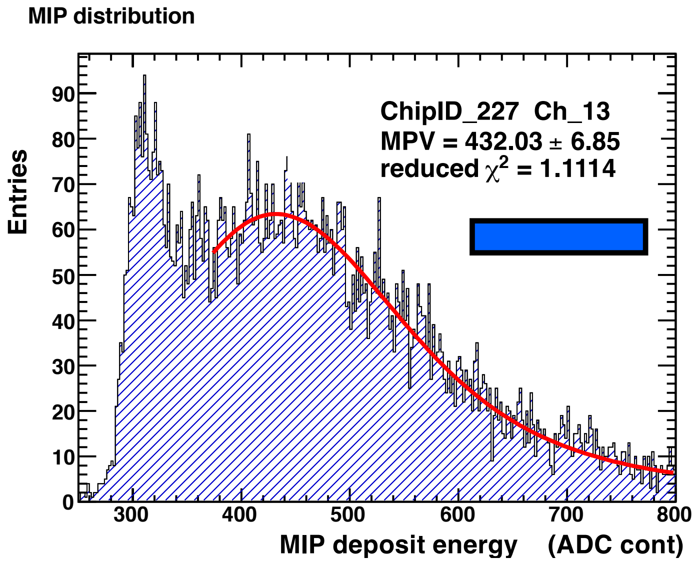
Chip227 4th row



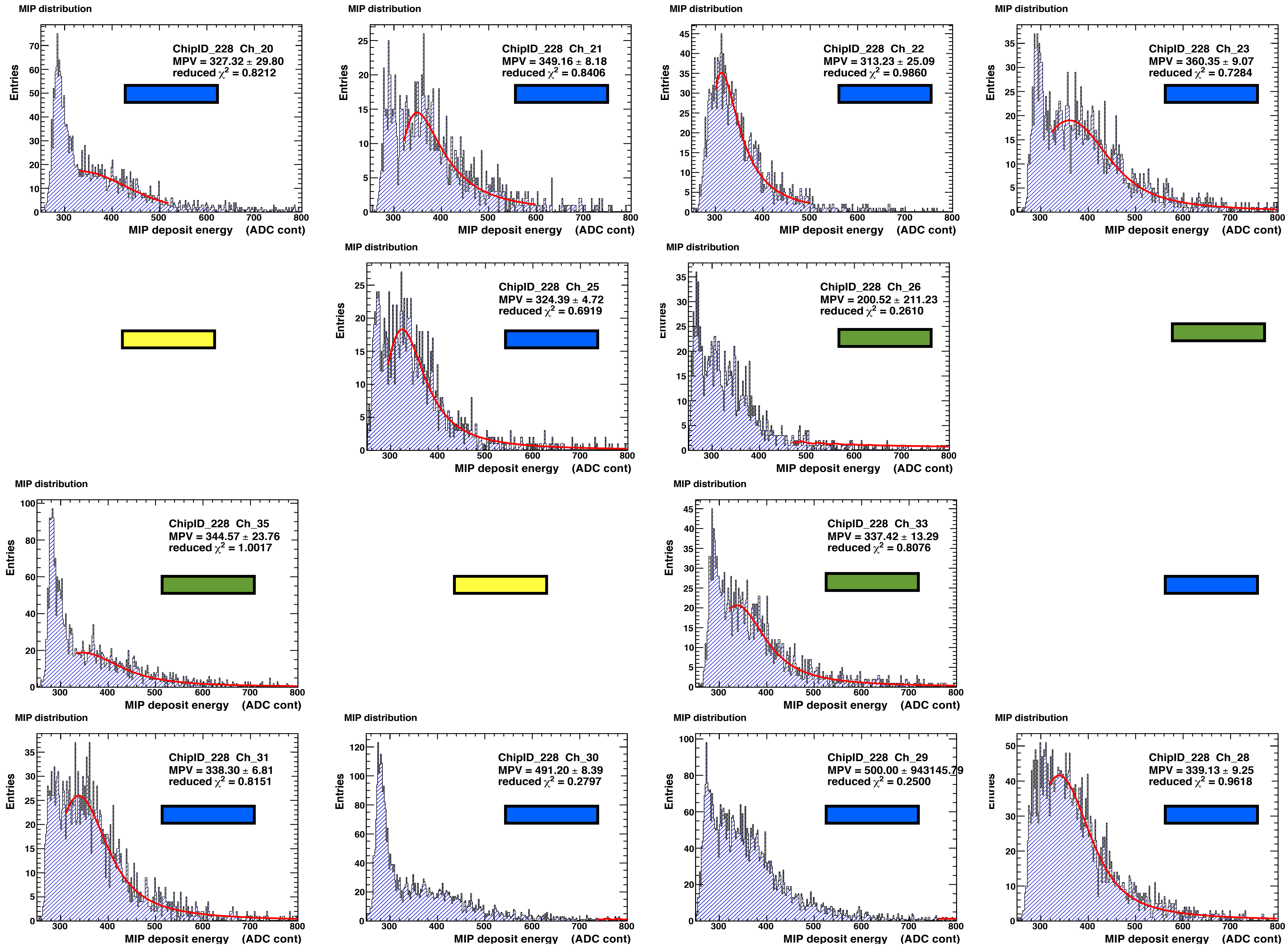








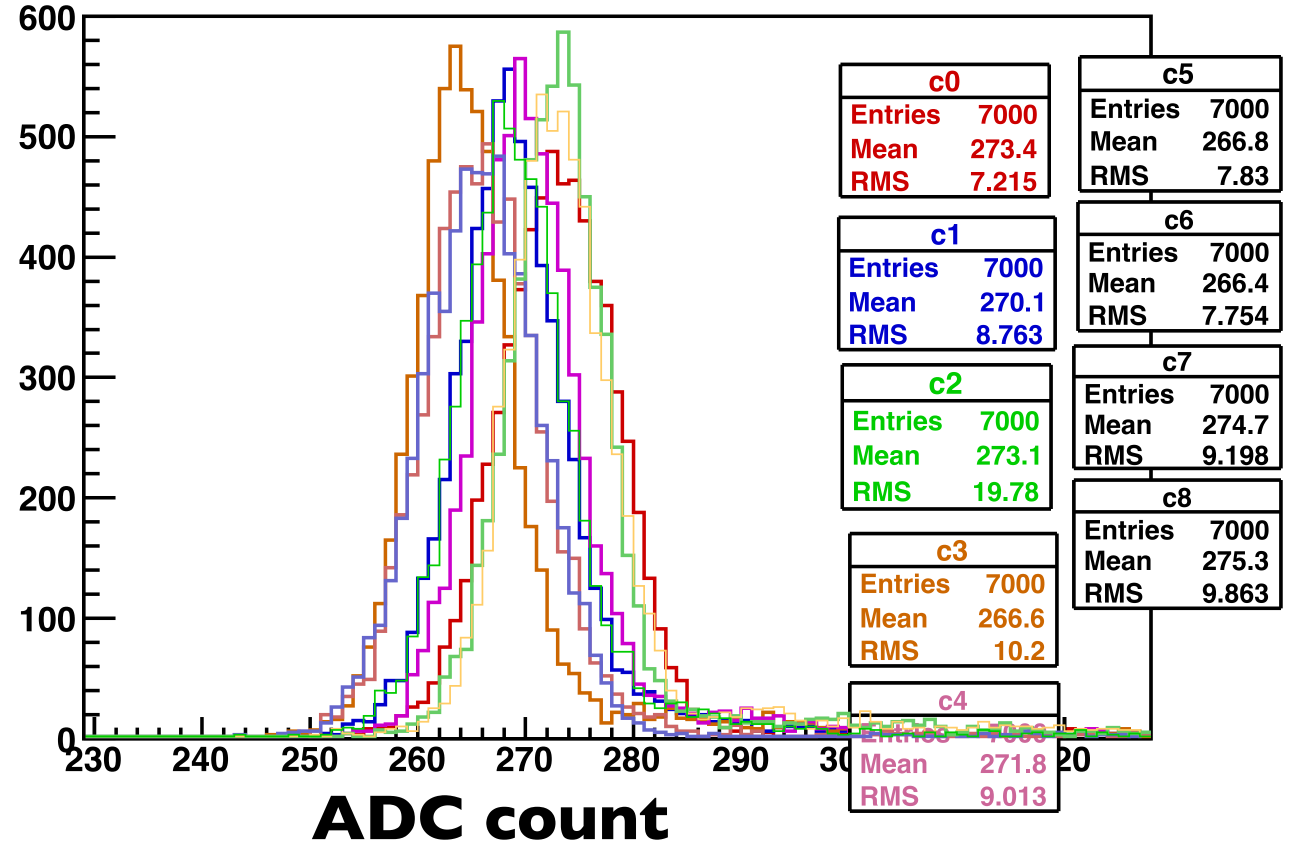
Chip228 4th row



Problem of Analog Memory Cells

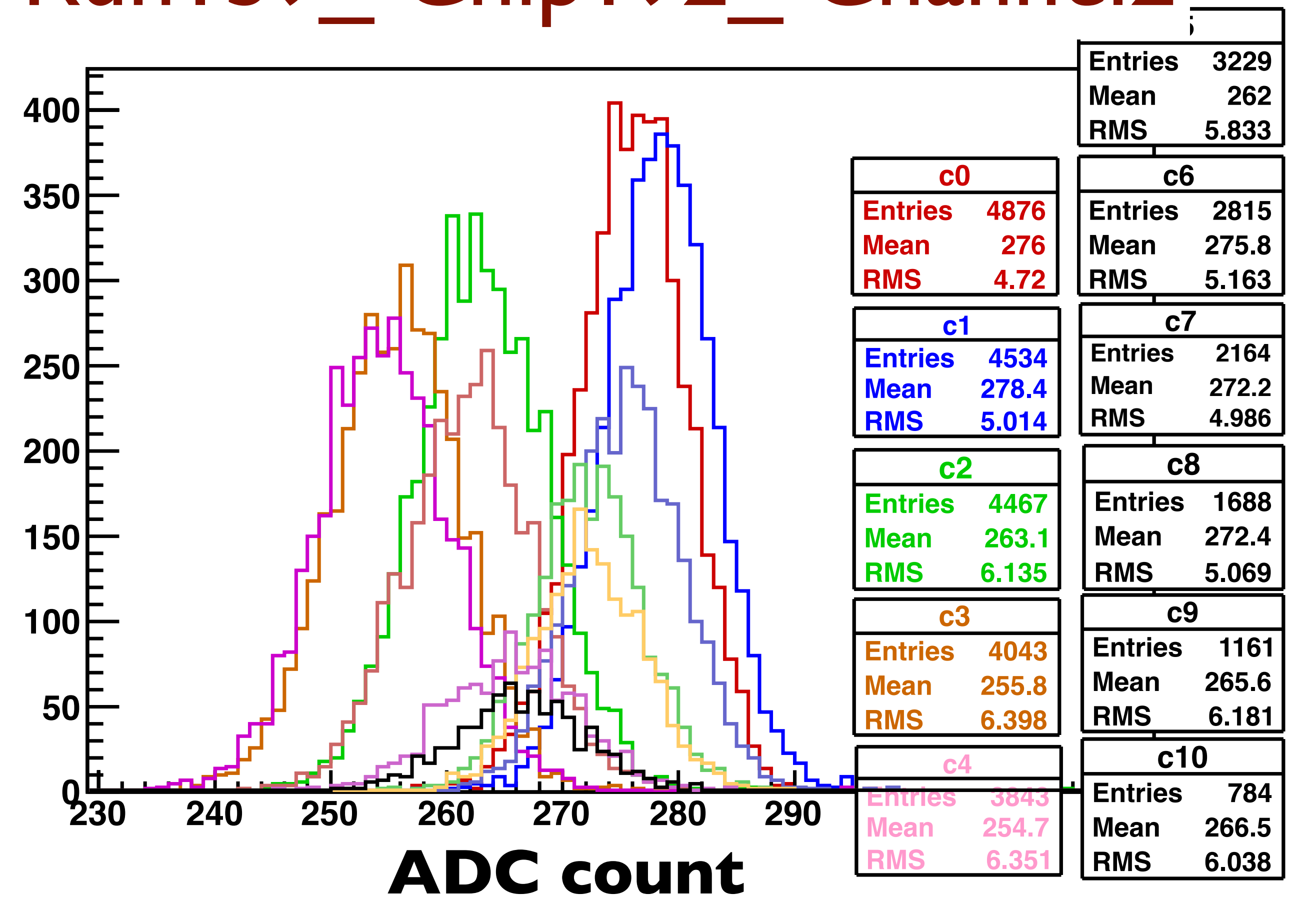
- 各チャンネルはデータ記録用に１６個のAnalogMemoryCellを持っている。
- 少し不安定で、条件により、Pedestalが動く。

Run185_Chip192_Channel2



ピンク mean ~ 272

Run159_ Chip192_ Channel2



ピンク mean ~ 255

Problem of Analog Memory Cells

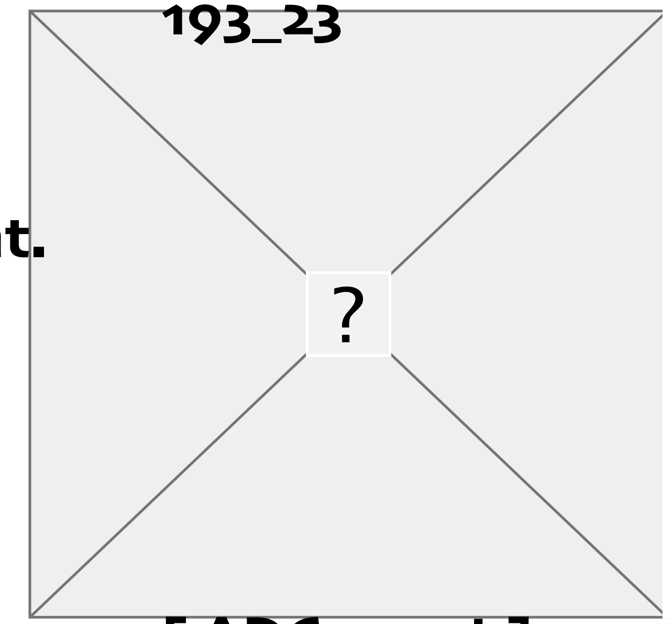
Pedestal of each memory cells

- Each channel has 16 memory cells.

- Pedestals of each memory cell are quite different.

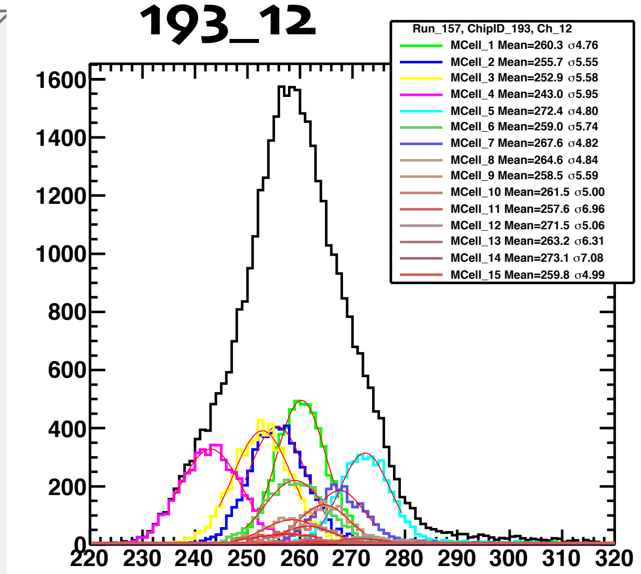
  → Need to analysis cell by cell
  or correct pedestal for each memory cell.

193_23



[ADC count]

193_12



[ADC count]

- Cell by cell analysis.

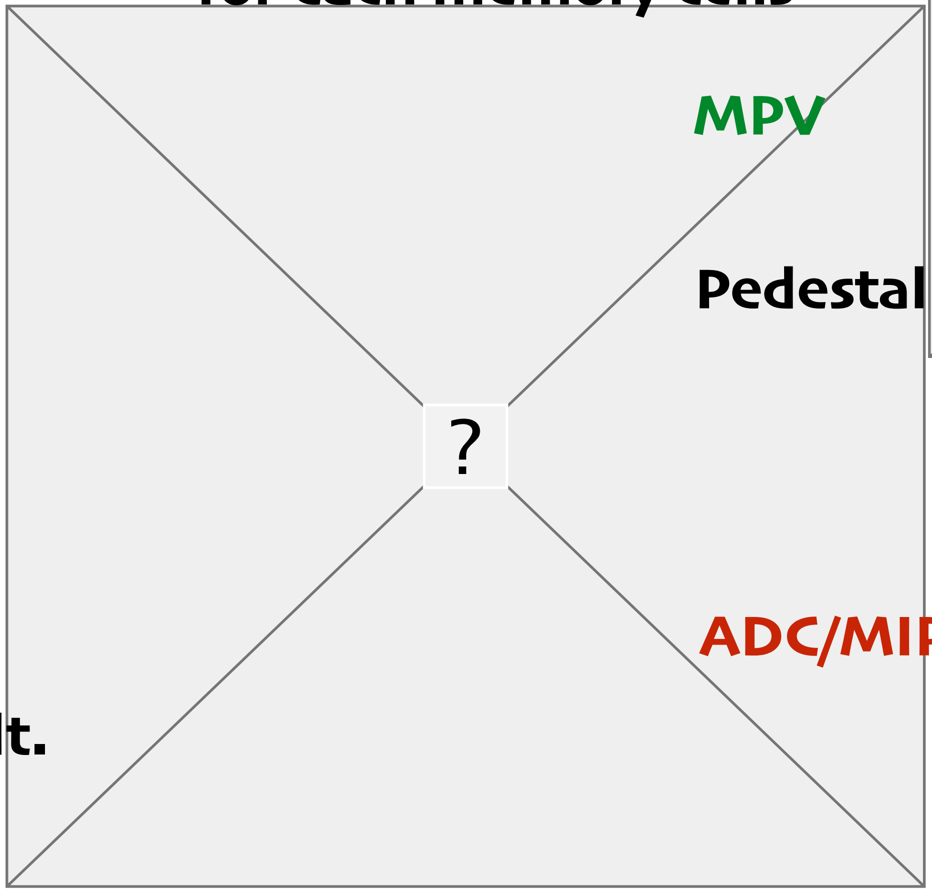
This means memory cells need to have ADC/MIP conversion factor individually.

In case we analysis cell by cell, the statistics decreases to less than about 1/15.

On latter half memory cell, It becomes more difficult to fit with langau and estimate MPV.

→ Cell by cell analysis seems to be difficult.

for each memory cells

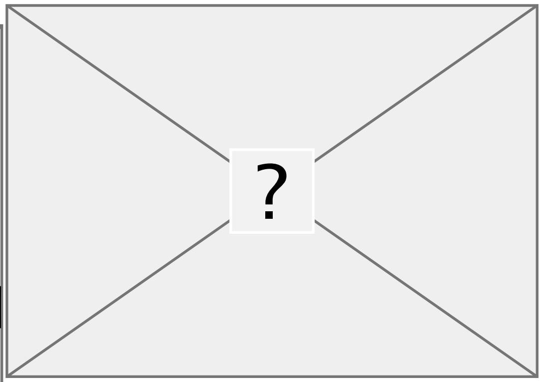


MPV

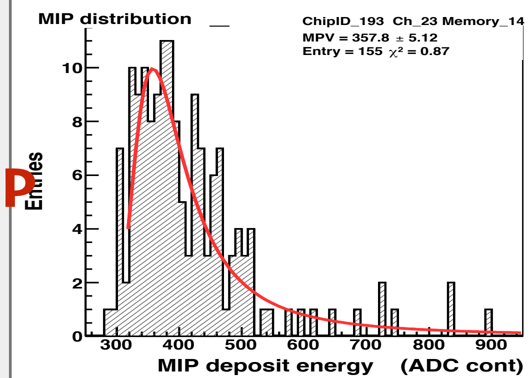
Pedestal

ADC/MIP

Memory_3



Memory_14

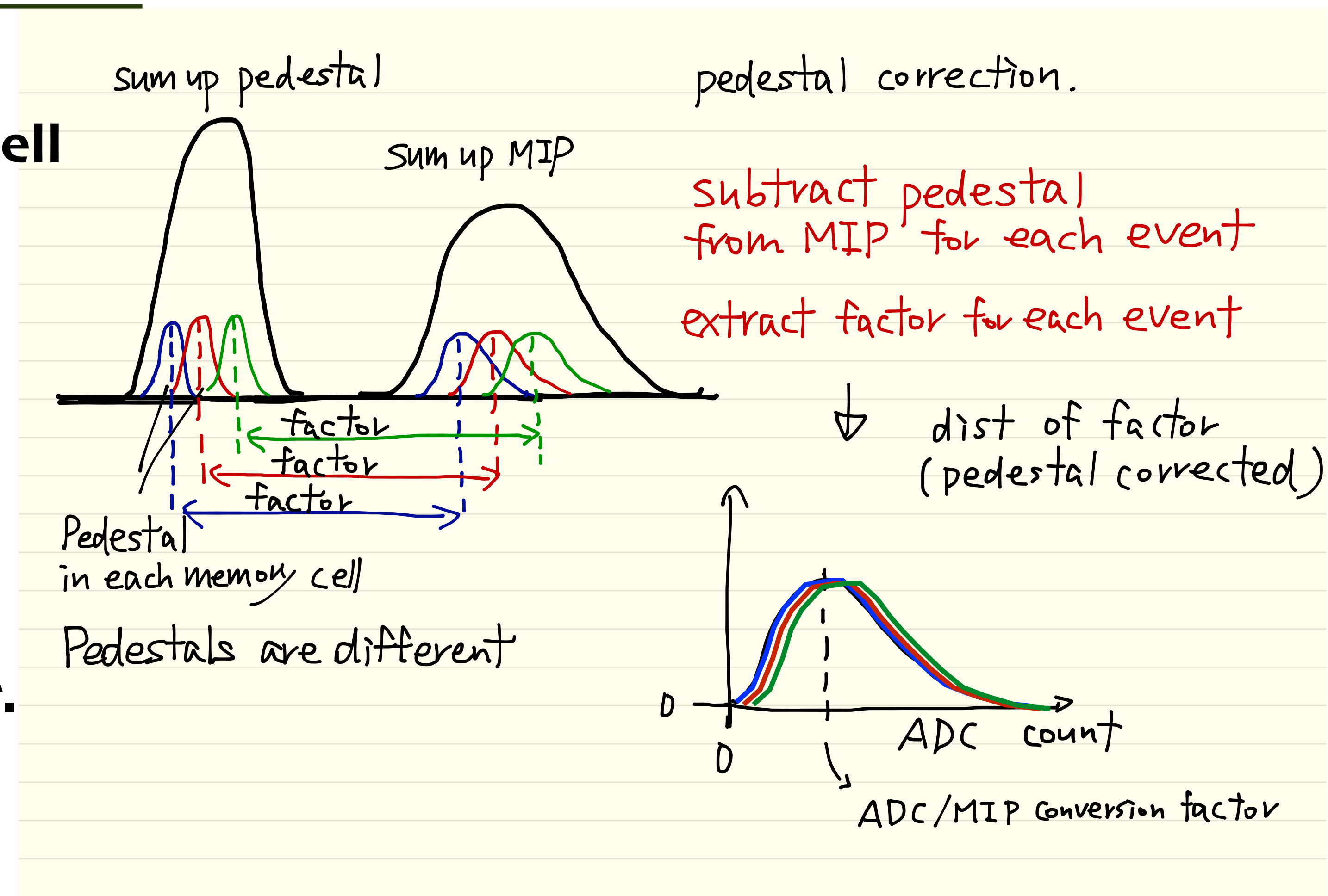


Problem of Analog Memory Cells

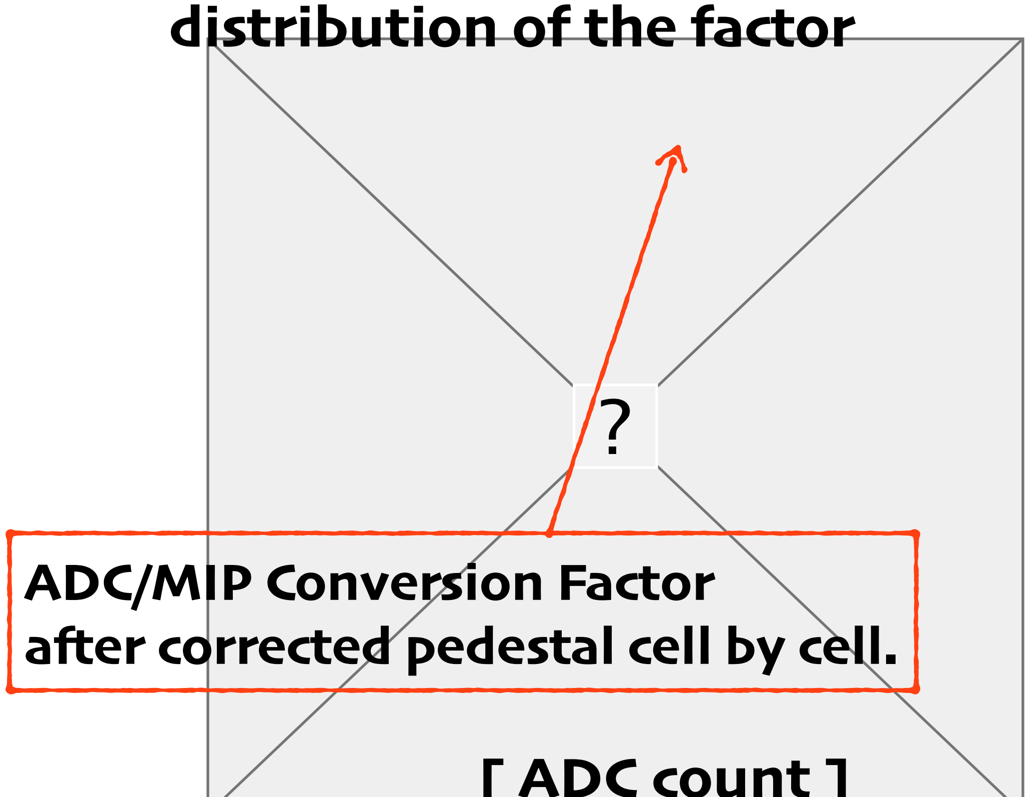
- We apply pedestal subtraction on cell by cell instead of cell by cell analysis.

  - Subtract pedestal from MIP for each event (for each memory cell), and extract factor.

  - From these factor we estimate ADC/MIP conversion factor.

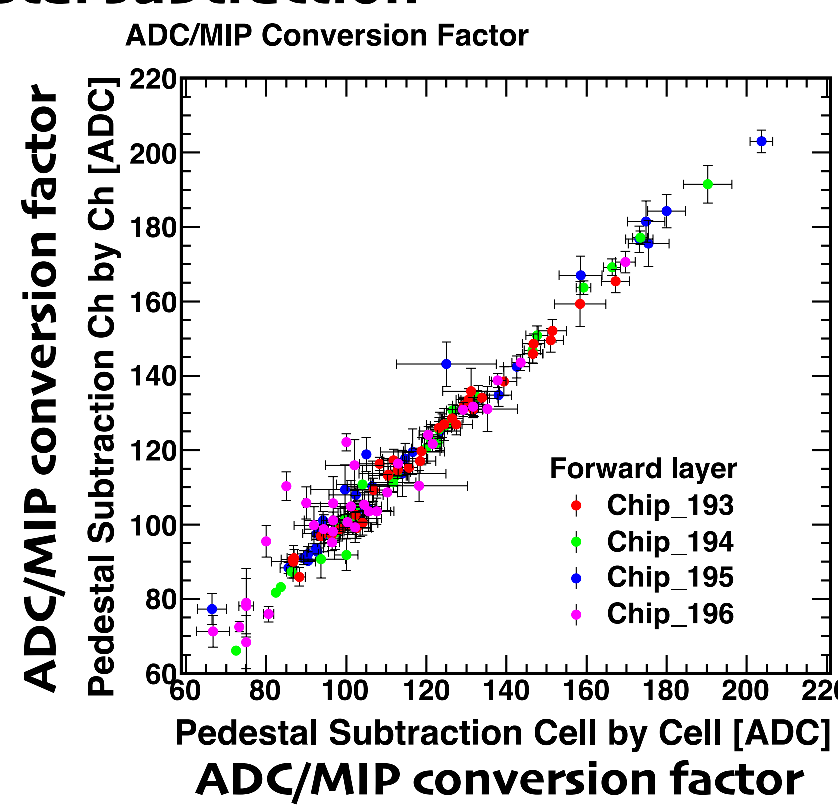


distribution of the factor

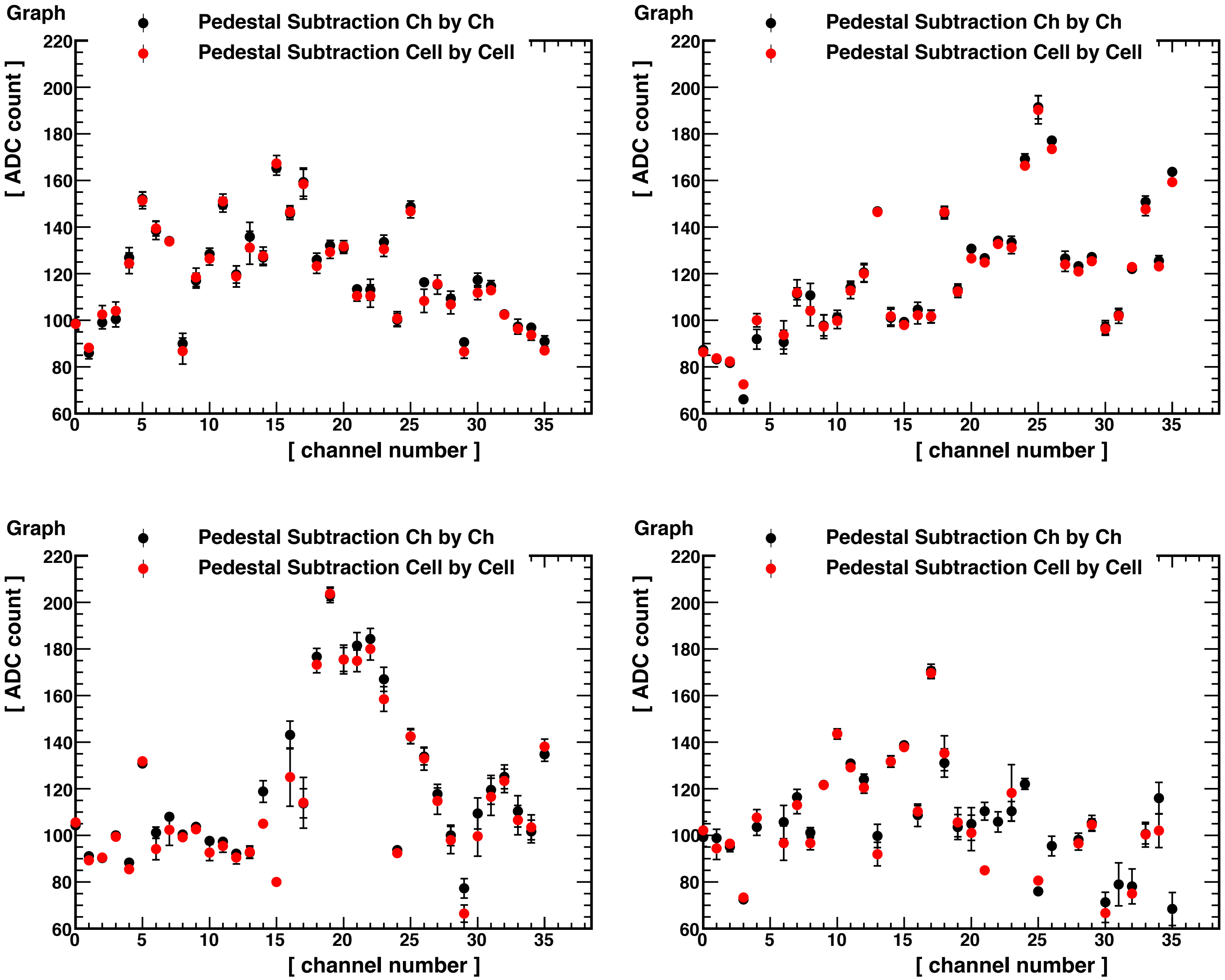


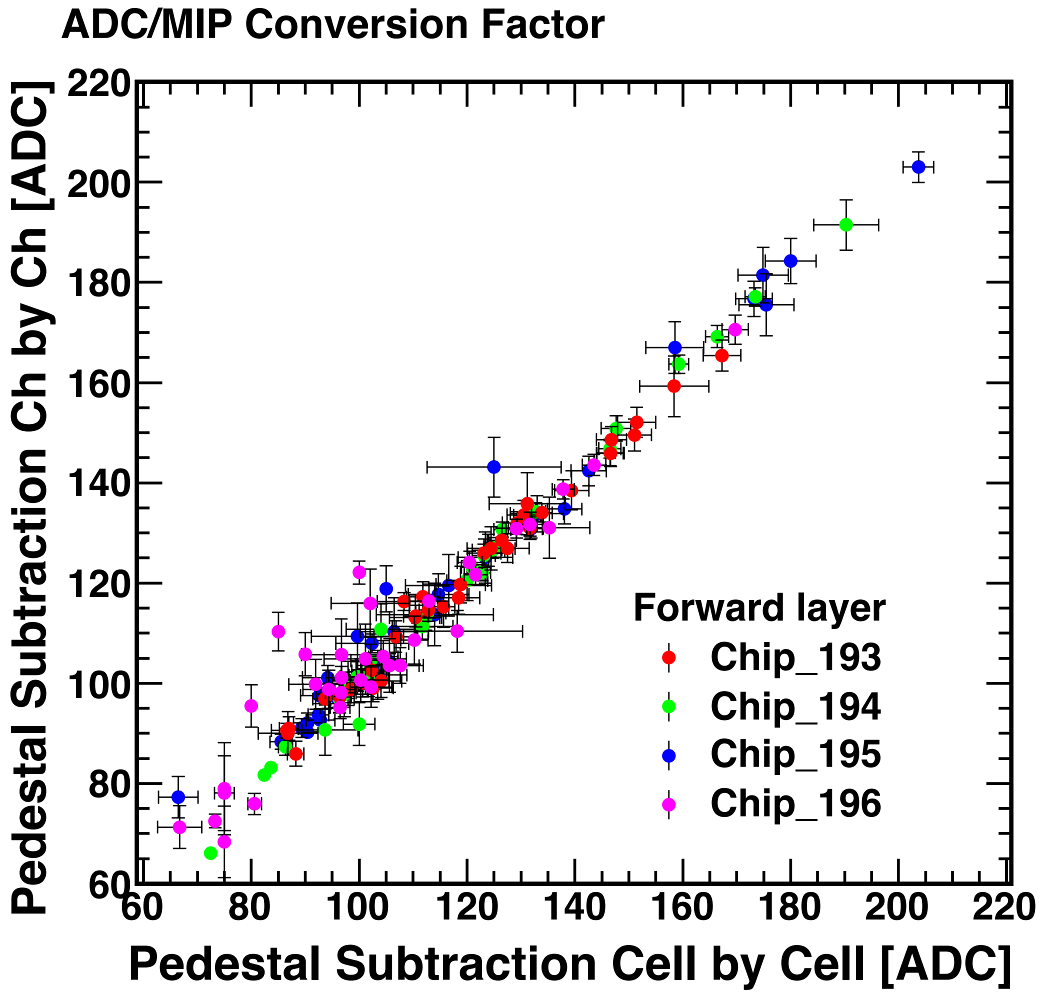
effect of pedestal subtraction

subtraction ch by ch and subtraction cell by cell match on around ± 20%

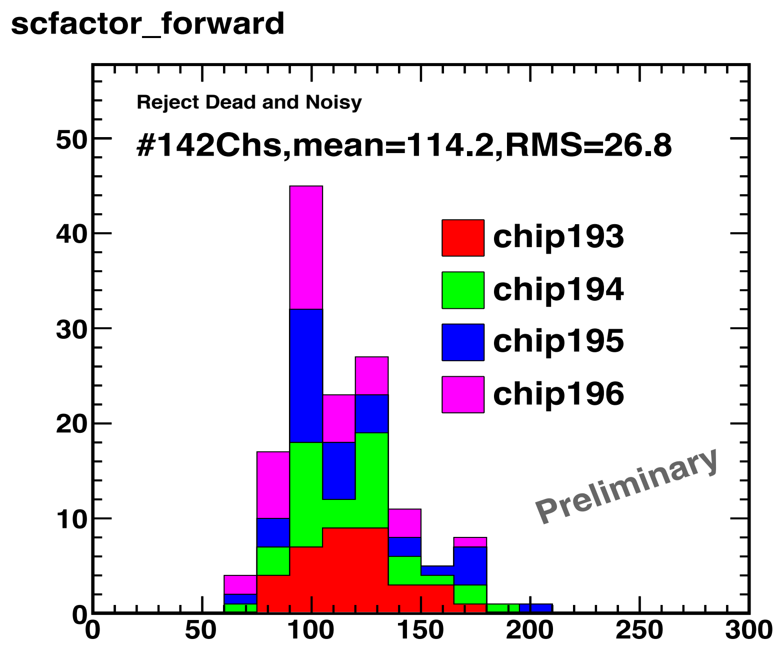


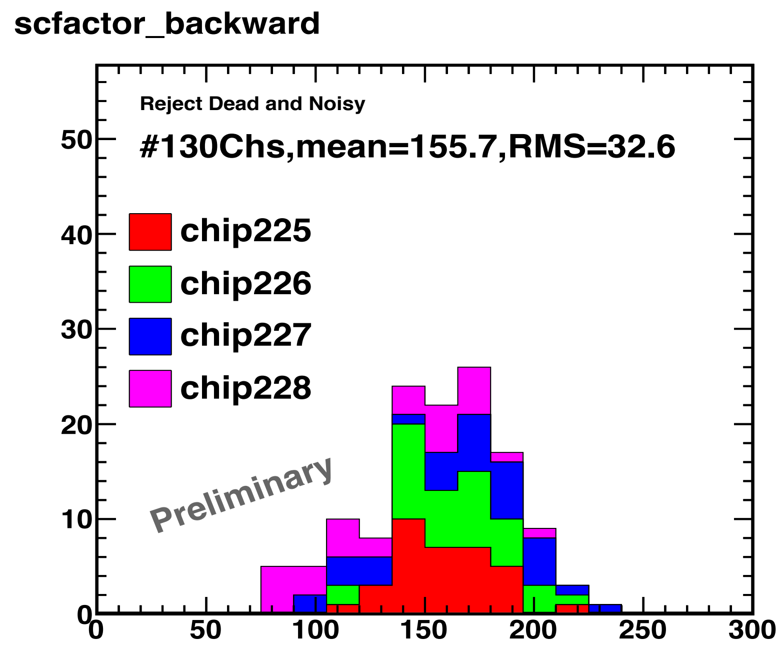
Pedestal Subtraction forward layer

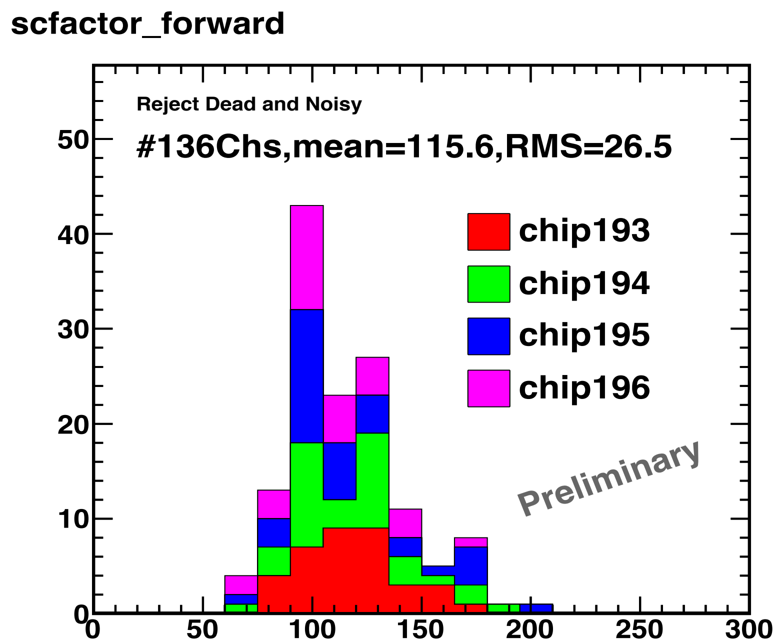


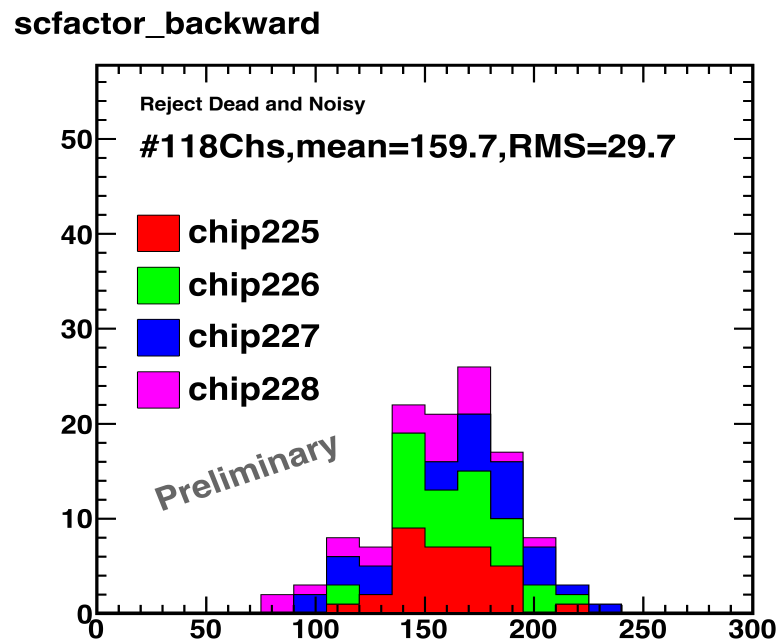


ADC/MIP factor







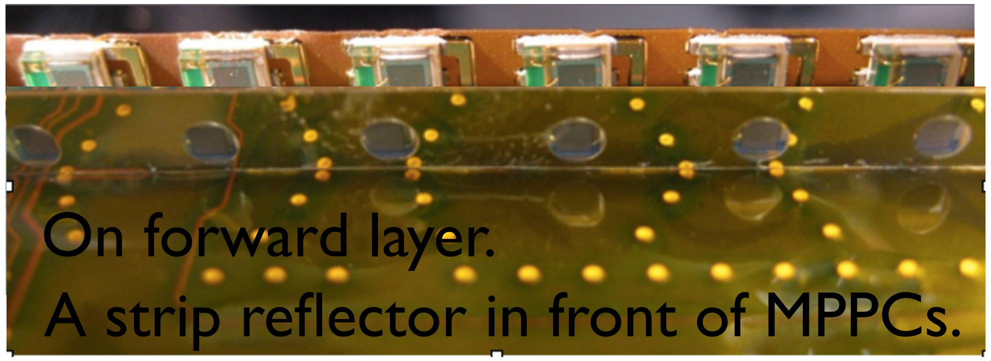


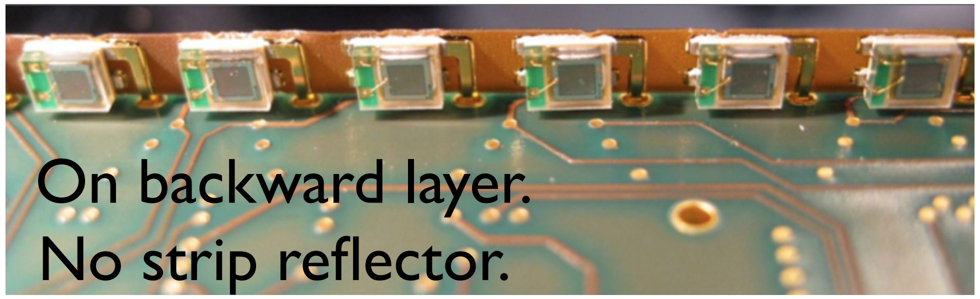
Photon Detection (Np.e./MIP)

• About photon detection.

The forward layer has a strip reflector in front of MPPCs.
The backward layer does not have it.

→ We want to confirm whether
the difference of photon detection appear.





• Reflector in front of MPPC seems not to be better?
Np.e./MIP is smaller.

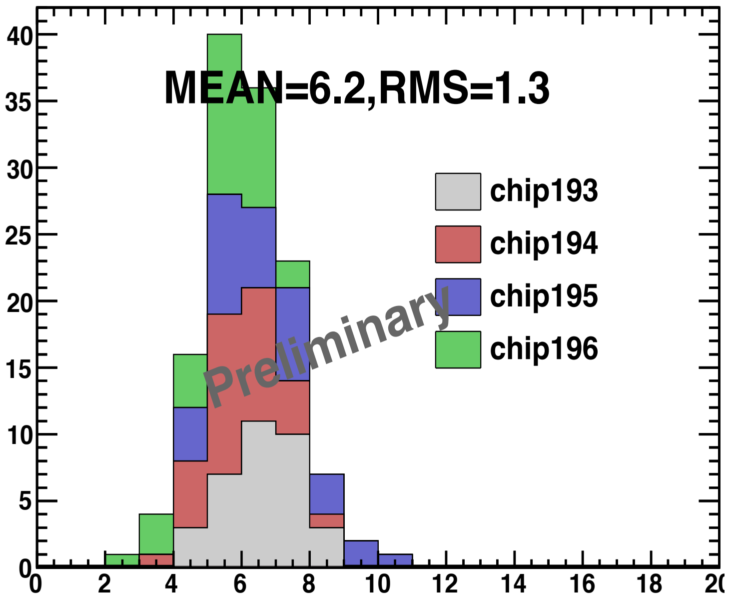
Np.e./MIP

Forward layer → mean: 6.2

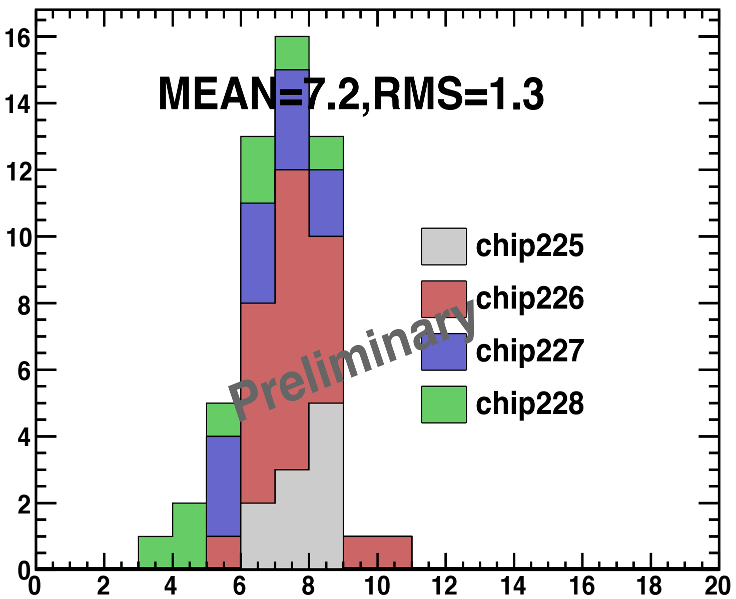
Backward layer → mean: 7.2

※we need 7p.e.
to remove thermal noise and keep response for Bhabha.

Forward layer Np.e./MIP



Backward layer Np.e.



There is the possibility that the voltage on backward is a little bit higher than forward. (gain calibration)
→ Absorption efficiency of photon rises.

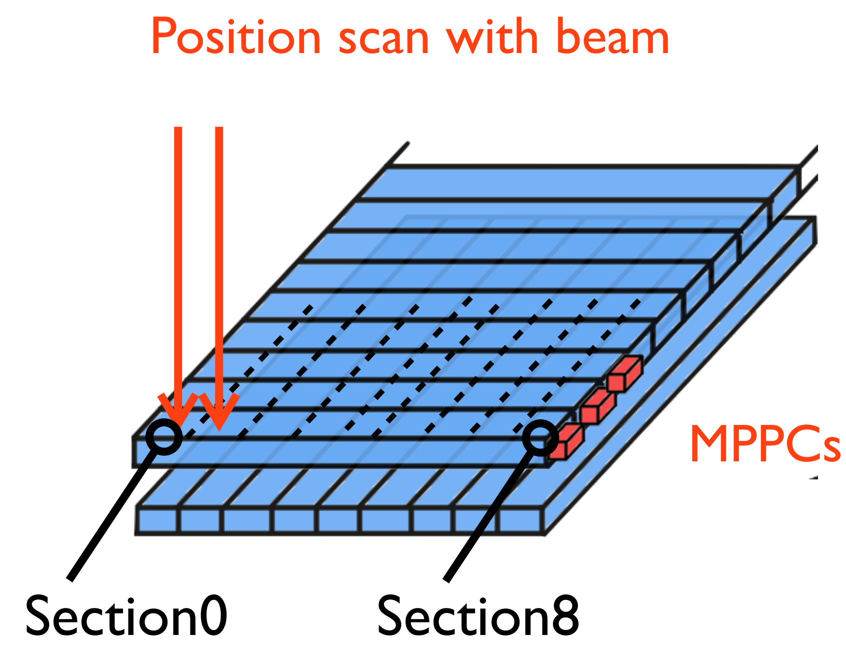
Uniformity

- About uniformity.

Changing the EBU position against beam,
we take a position scan with 5mm grid (divided 9 sections).

Confirm a uniformity of a scintillator
and in front of MPPCs.

→ Extract ADC count with 2 layer coincidence.

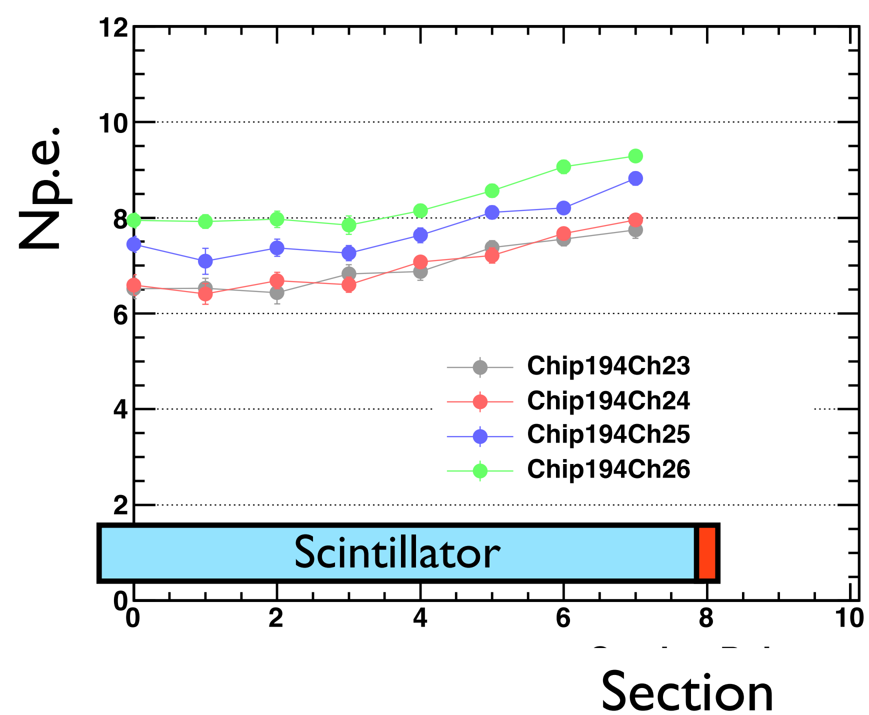


→ Photon yield is larger at in front of MPPCs.

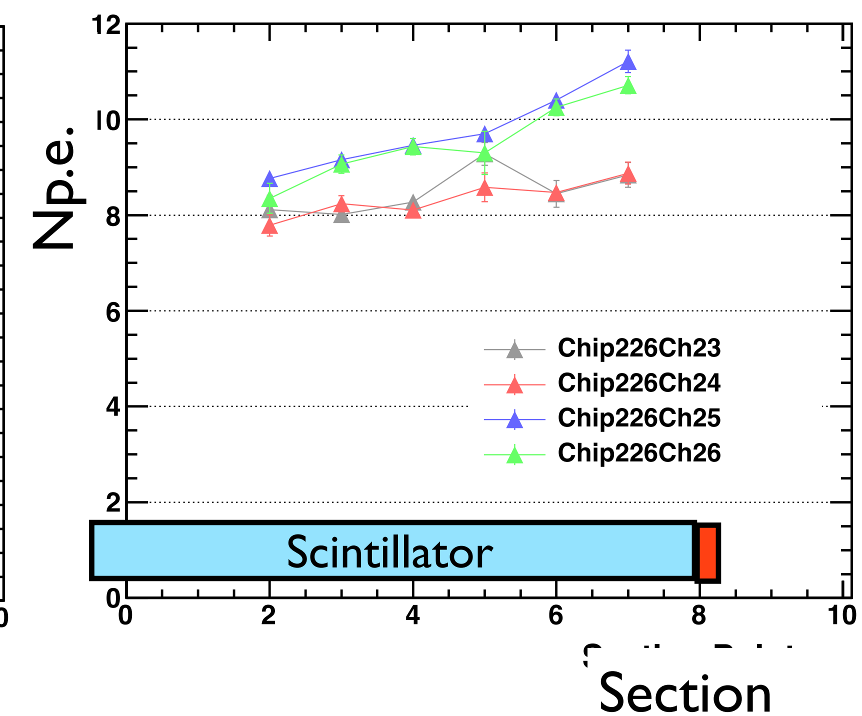
On forward layer,
the channel behind which is
corresponding to the section 8
turns off.

On backward layer,
the data is only half of 1st layer.
There is no data on section 0
and section 1.

Forward layer Np.e.



Backward layer Np.e.

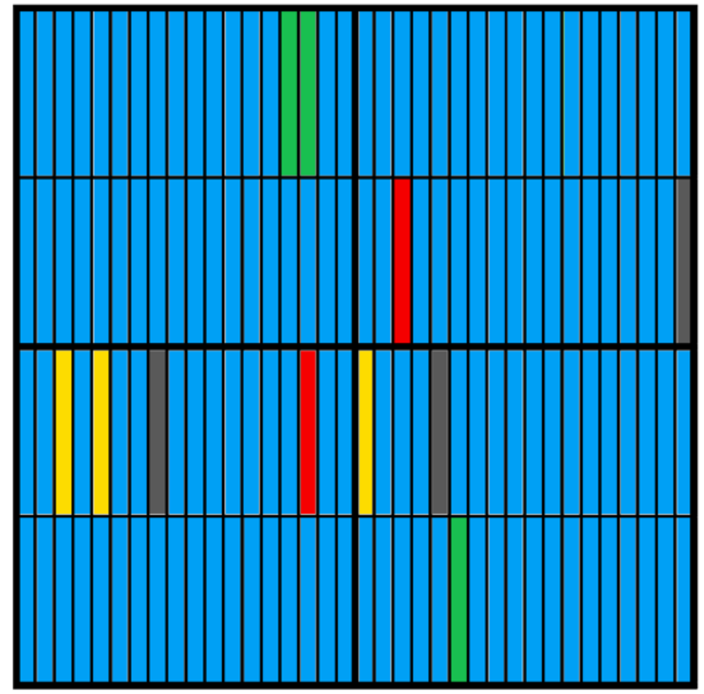


LED Gain Calibration

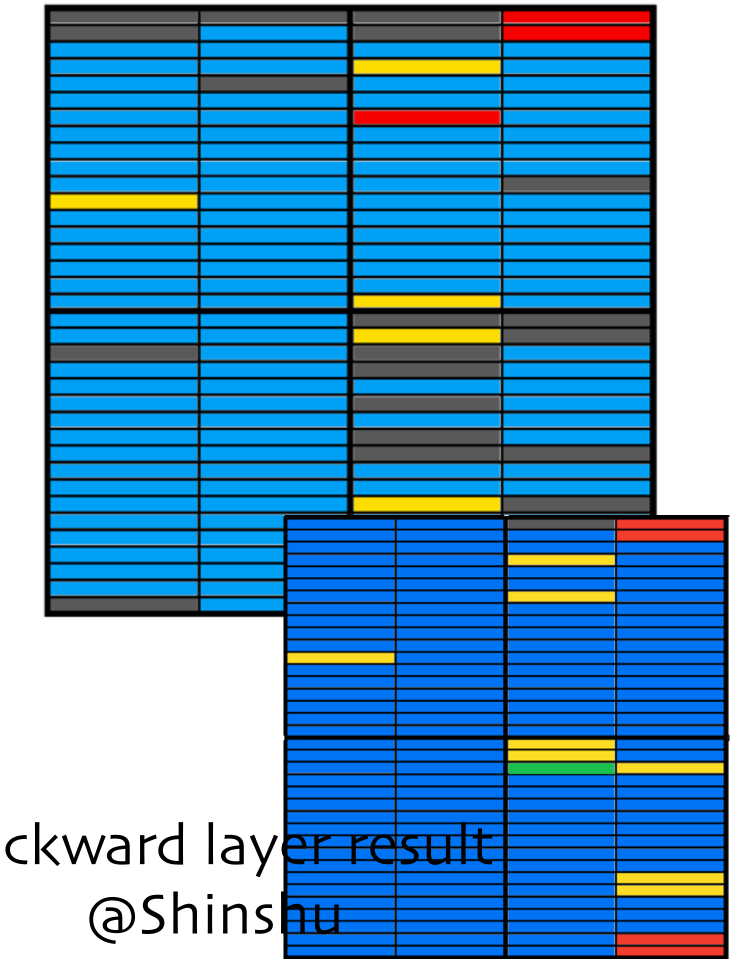
- Gain calibration result at DESY.

- good p.e. separation.
- is difficult to separate p.e.
- strange signal (noisy)
- No signal
- couldn't calibrate on time.

Forward layer result



Backward layer result



Backward layer result
@Shinshu

→ On forward over 90%channels could be calibrated.

→ On backward near 90%channels could be calibrated.

(except problematic area.)

- ADC/p.e.

ΔV = +3.0 from break down.
Same settings on both layers.

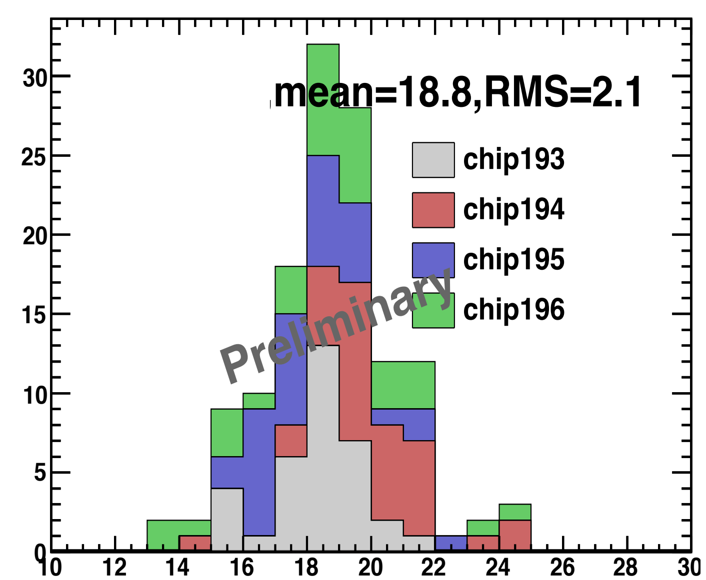
Gain (d-value).

Forward layer → mean: 18.8 RMS: 2.1

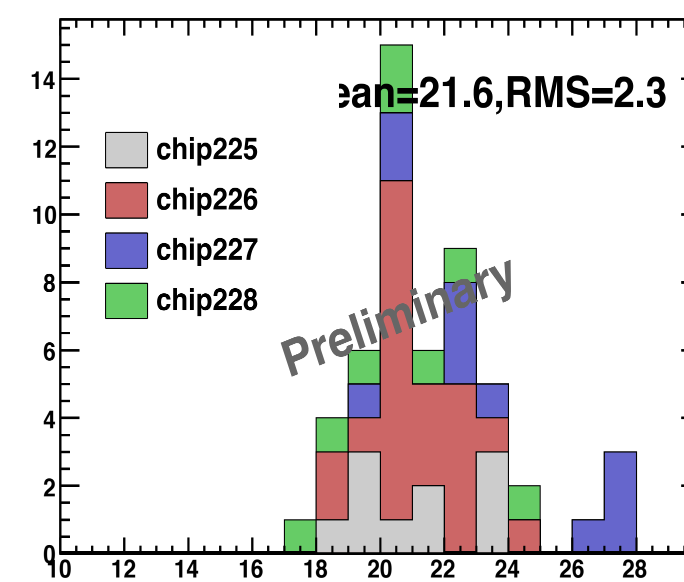
Backward layer → mean: 21.6 RMS: 2.3

* Although we set same bias voltage,
the gain seems to be little different

Forward layer d-value

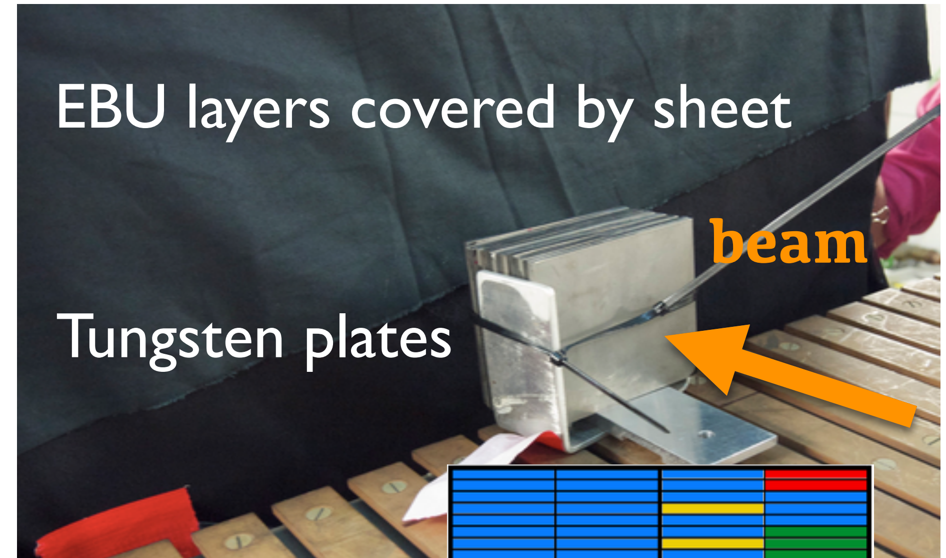


Backward layer d-value



Applying Simple SSA

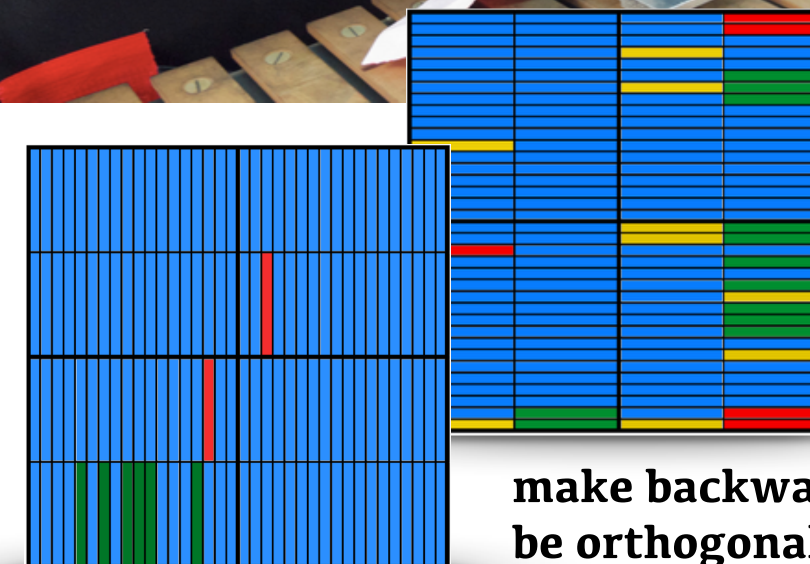
strip scintillator ECAL requires a sophisticated algorithm named SSA (Strip Splitting Algorithm)
to produce square cells and achieve high granularity 5x5mm.



- **We made shower events with Tungsten absorbers.**

  Changing the number of tungsten absorbers.

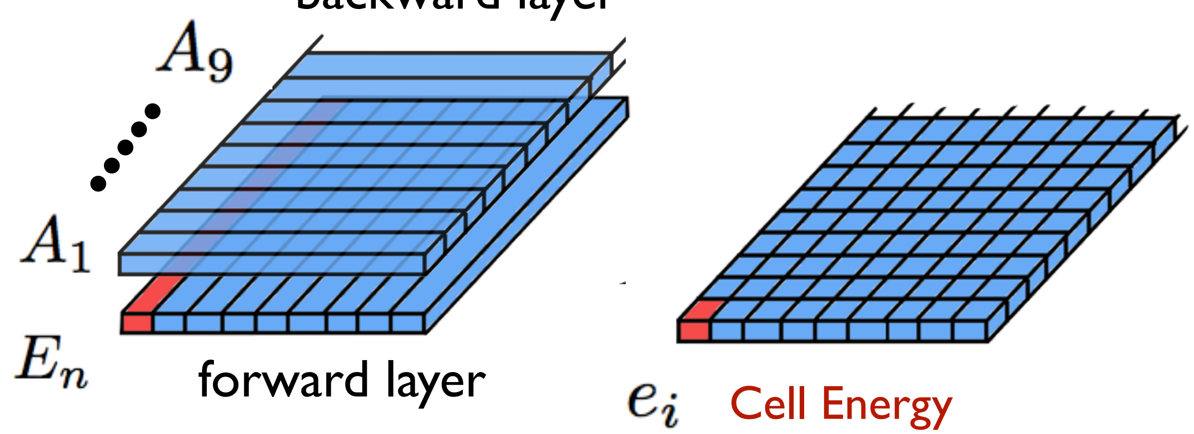
  → We try to measure the spread of EM shower like a pseudo multi layer.



make backward layer be orthogonal against forward layer.

- **Try to calculate Cell Energy by using simple SSA.**

$$e_i = E_n \cdot \frac{A_i}{\sum_{i=1}^{9} A_i}$$



Cell energy with SSA = N of MIPs of one strip on the forward layer × (N of MIPs of one strip on the backward layer which is corresponding to the strip on forward layer.) / (Sum of MIPs of nine strips on backward layer which is corresponding to forward layer.)

Beam Test of Scintillator ECAL Engineering Prototype

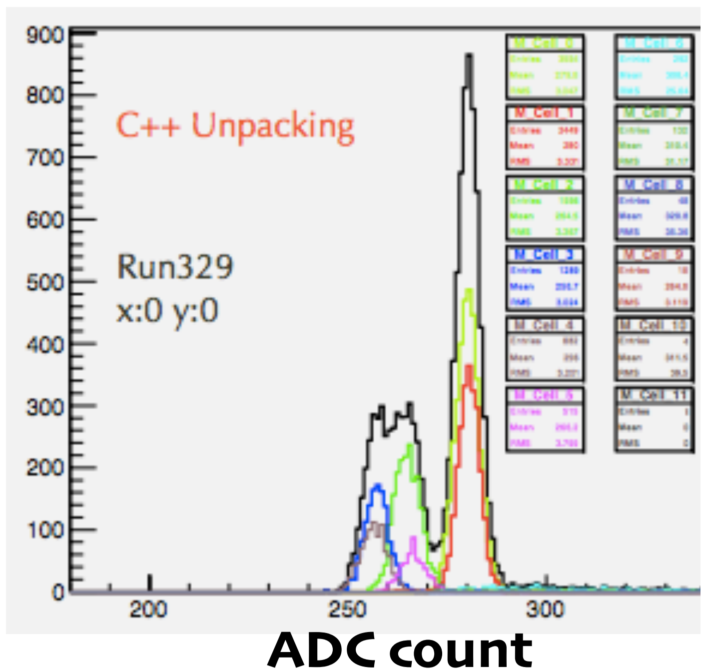
- CALICE group has developed the electronics "EBU"(scintillator ECAL Base Unit) which a readout chip is embedded at, based on analog HCAL electronics "HBU".

- SPIROC ASIC is used for readout and it has 16 memory cells at each channels to store data.

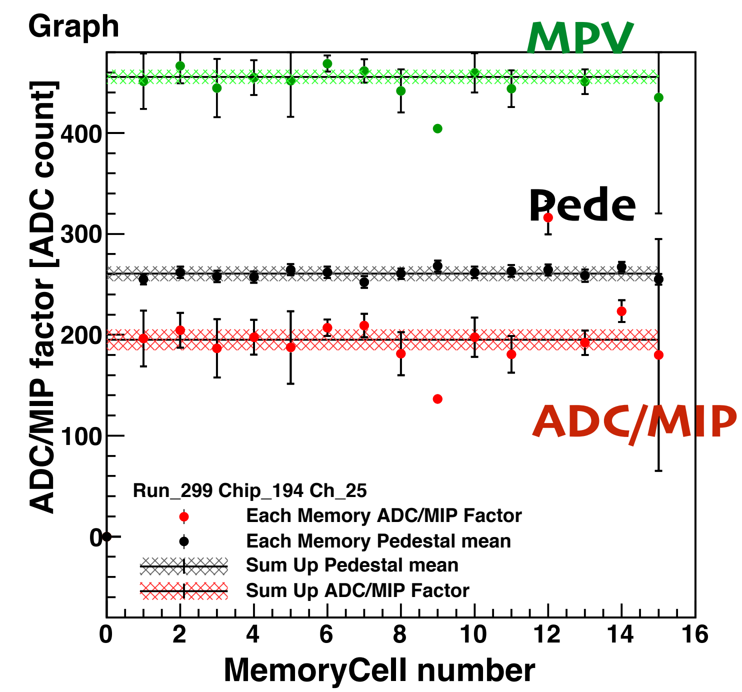
- We CALICE group tested this EBU engineering prototype and found out these memory sells are not stable (and bug of program).

Pedestal distribution →
at each memory cells
on one channel.
(analysis by Lloyd)

memory number
0,1,2....15



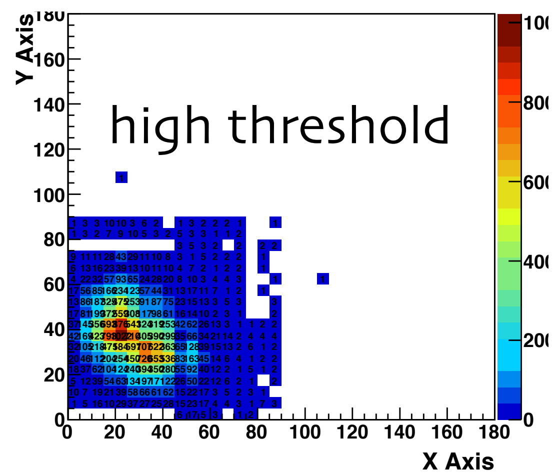
- Actually we need to analysis cell by cell. but because statistical reduce, we use a sum-up value.



- Also we tried testing synchronization with analog HCAL layer for next step.

Hit rate →
Hit concentrate on diagonal area.
(In case there is 4layers coincidence)

EBU



HBU