2013/12/17 Hisao SATO
(Shinshu-univ.)

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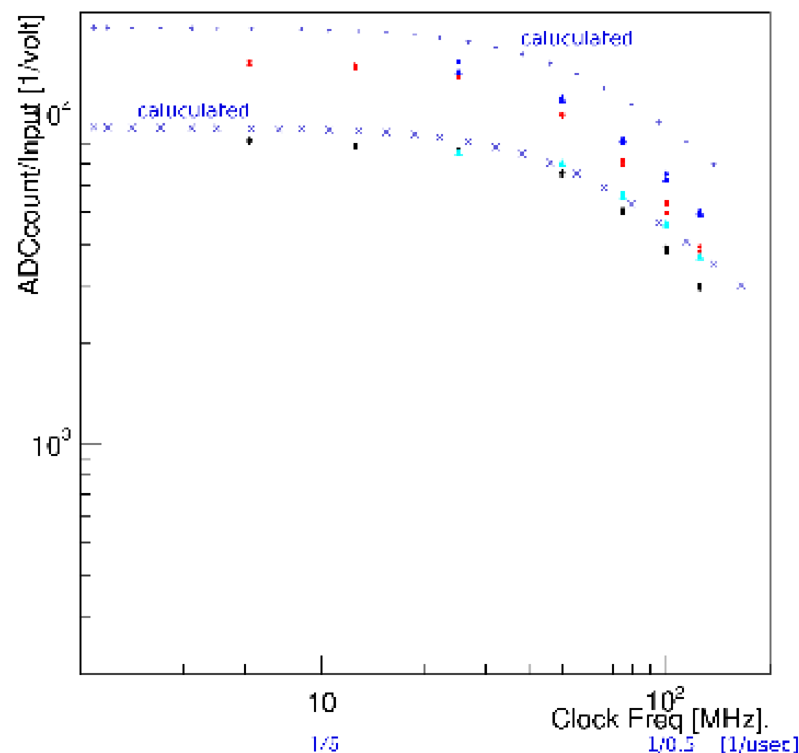
1. ASIC 3rd silicon “AFFROC” characterization

AFFROC characterization continues since Sept. last year. Gain and noise characteristics over operation clock frequency ~125MHz and at low temperature come to be well understood.

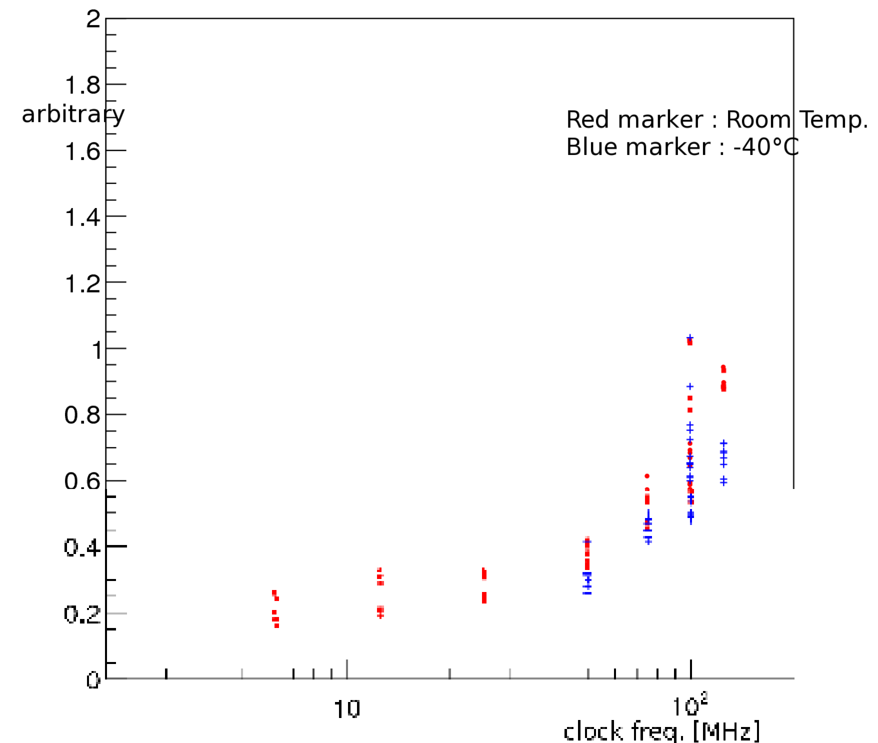
CAB7 @RT, -40℃

freq. vs gain,



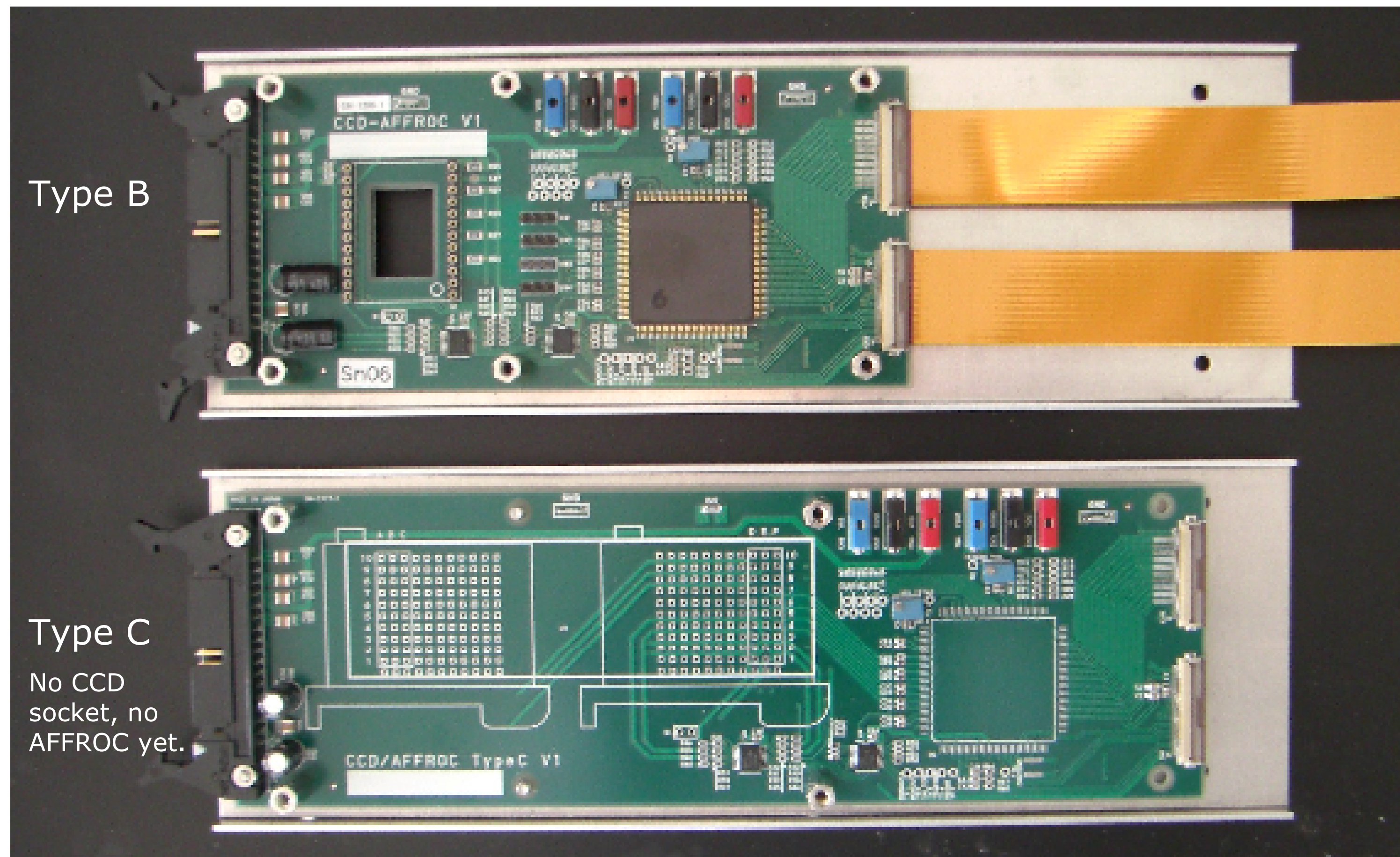
ine : Input equivalent noise

freq. vs ine noise @CAB7,T:-40



2. Preparation for the large CCD test

CCD AFFROC “type C” board is designed and fabricated for the Large CCD test. The test has not started yet.



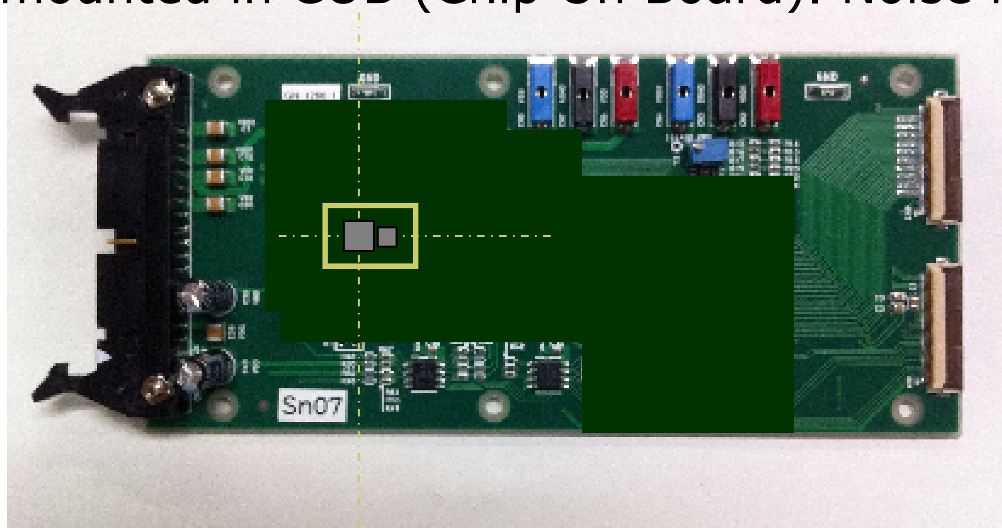
3. Preparation for CCD + ASIC COB board

Currently working on designing "type D" board, whose CCD and AFFROC are mounted in COB (Chip On Board). Noise reduction is expected.

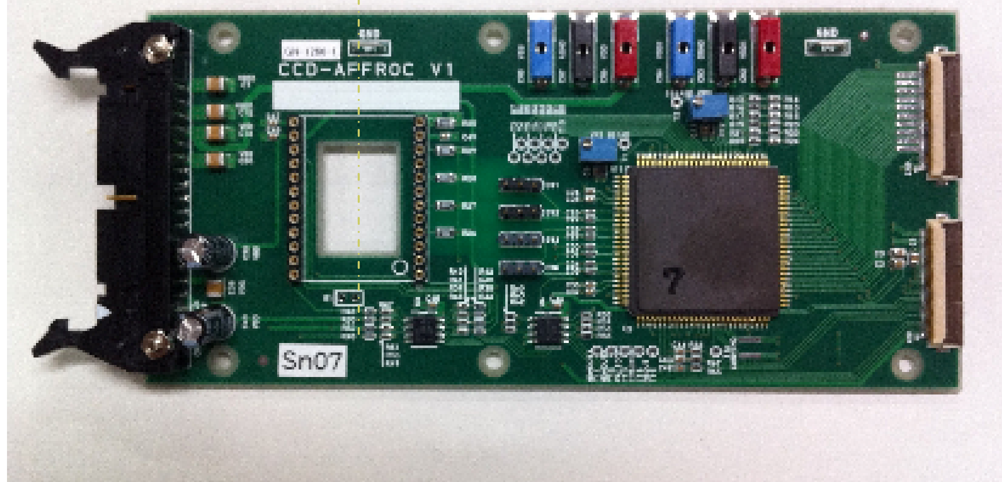
Type D will be like this.

Same size as type B,

CCD chip is located at the same position.



Type B



4. Preparation for the beam test 4.1 Readout hardware

4.1.1 Performance goal

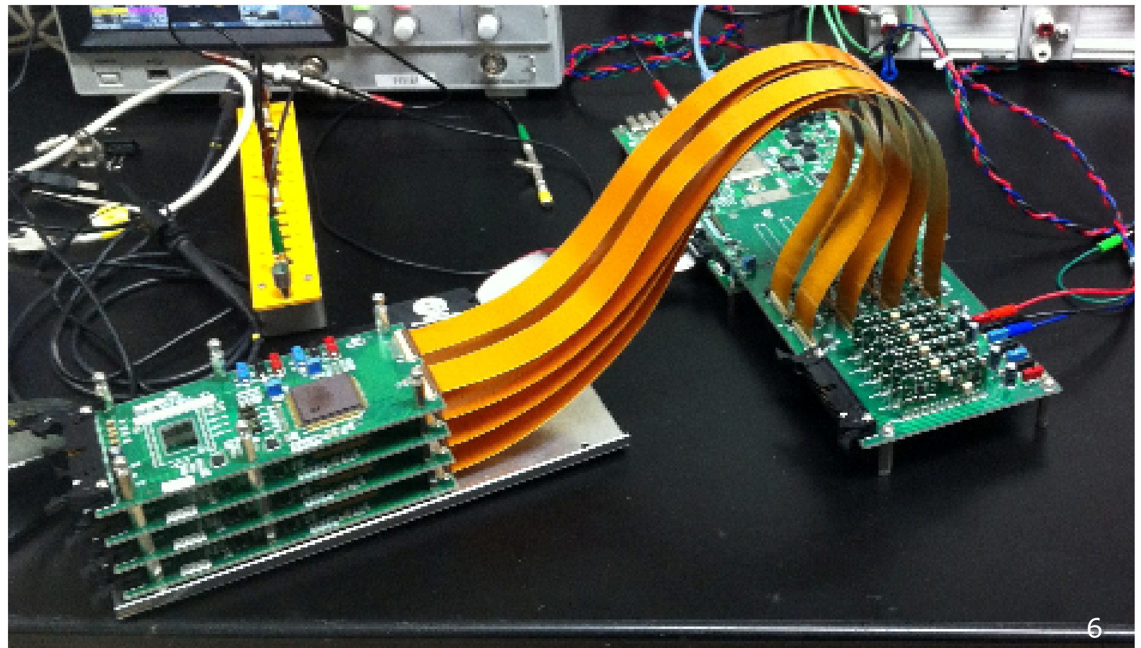
-four layer FPCCD electronics, total 16 channel readout on SEABAS2.
-2.5MHz sampling due to SiTCP performance bottleneck and CCD clock signal delay problem. (originally request 10MHz sampling)
-prepare enough hardware resources; CAB,AIB,SB2, cables, CCD clock drivers.
-FPGA design specification.
-CCD temperature measurement capability
-Synchronize to an external 6 second repetition trigger signal

Current status:

-16channel readout is not fully verified.

-FPGA document is not in good shape.

-CCD temp. measurement is been working on now.

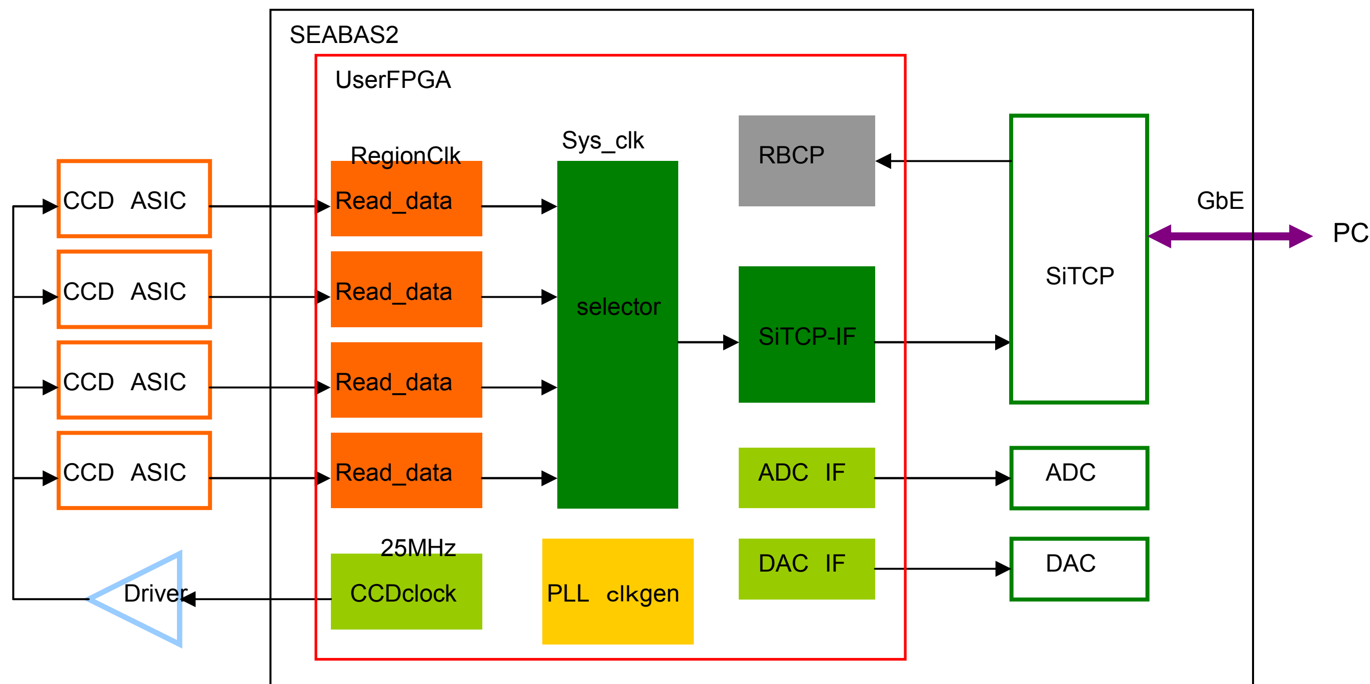


4. Preparation for the beam test 4.1 Readout hardware

4.1.2 Four CCD+ASIC support FPGA

When test boards were designed last year for ASIC test, 4 CCD layers electronics were taken into account. Then major work for beam test preparation is to implement 4 CCD+ASIC support electronics in the FPGA "uflE", shown in a diagram below. Especially a selector and a SiTCP-IF in the diagram are key modules to perform 16 channel readout.

SEABAS2 base system block diagram

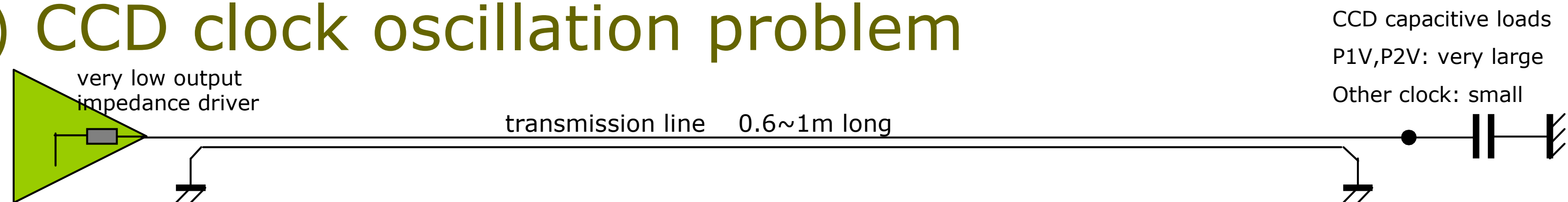


4. Preparation for the beam test 4.1 Readout hardware

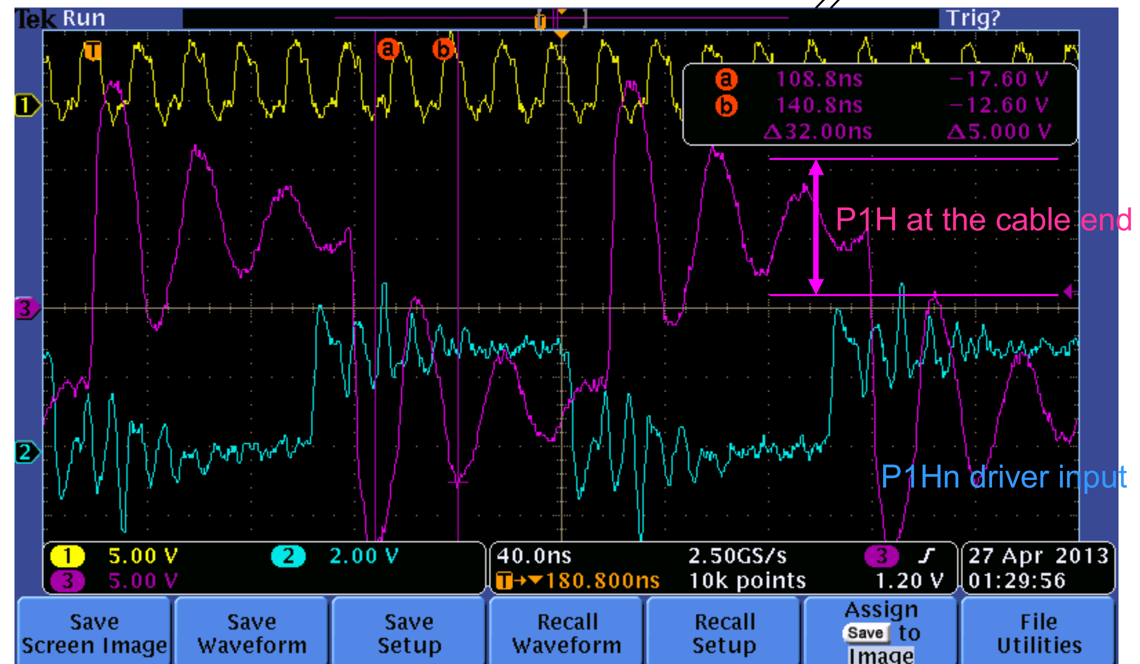
4.1.3 problems solved and remain

During debugging electronics, we discovered some problems of CCD clock signals, that affect ladder design and clock driver design next year.

1) CCD clock oscillation problem



Dumping oscillation is observed at the CCD end of the cable, peak amplitude is high, almost twice of the original clock amplitude.
A transmission line behaves ¼ λ resonator, because of low driver impedance and light load.



This is solved by change output impedance to 100Ω to match the cable.

4. Preparation for the beam test 4.1 Readout hardware

4.1.3 problems solved and remain (continue)

2) CCD vertical clock “P1V/P2V” capacitance is large.

In a critical moment of CTI test in CYRIC, we discovered that even lower impedance driver could not drive vertical clocks properly. Then we widened CCD clock pulse as a temporally fixing.

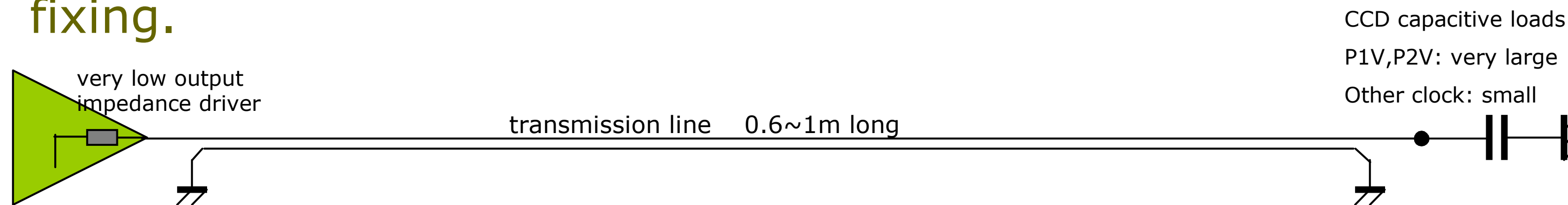


Table 4.1.3
gate capacitance (pF)
2007 CCD sample

	15um	24um
P1H,P2H	40	40
RG,SG,OG	10	10
TG	50	50
P1V,P2V	1600	550

Table4.1.3 shows gate capacitance of standard size test chip. Ratio of max cap. to min.cap. is x160. Real Vertex CCD is x10~40 larger than test chip. P1V,P2V capacitance becomes larger. Ratio of max cap. to min.cap. becomes ~x6,000.

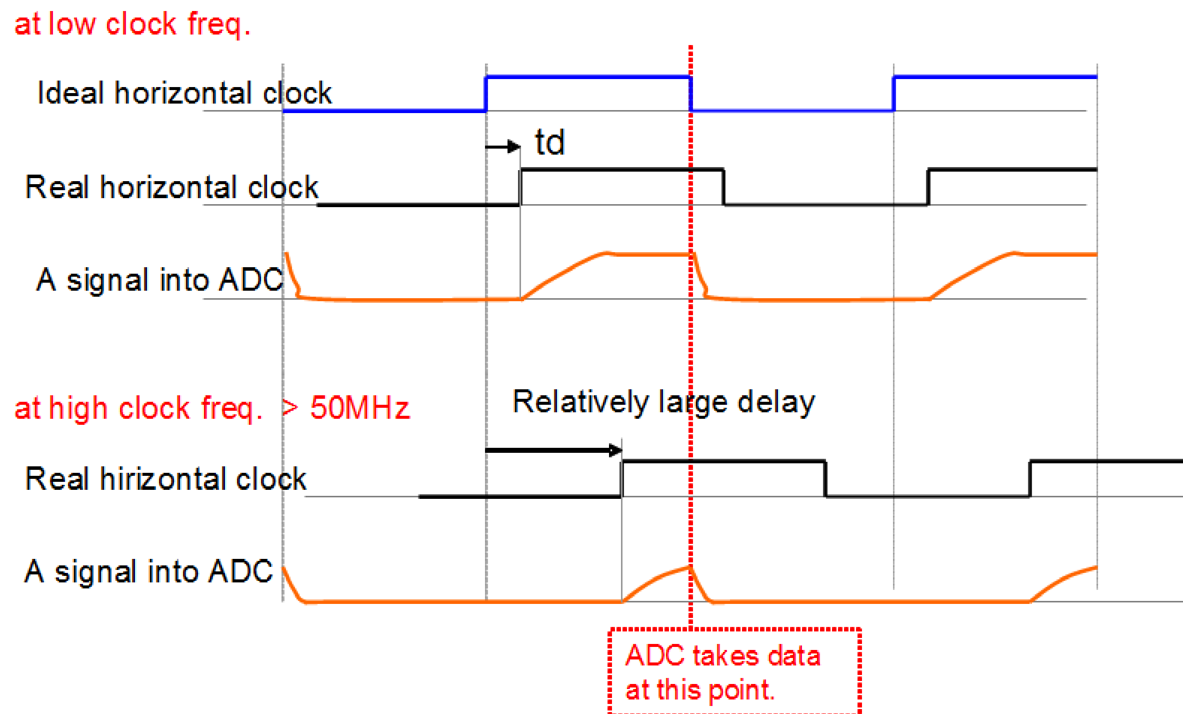
Different circuit technology may required for vertical clock driver.

4. Preparation for the beam test 4.1 Readout hardware

4.1.3 problems solved and remains (continue)

3) CCD clock driver delay:

At high frequency, above 50MHz, delay of CCD clock driver output is significant and reduce ADC gain.



CCD clock driver inputs need preceding timing in order to cancel the delay.

4. Preparation for the beam test

4.2 Readout software

Employed “DAQ-Middleware” as a base, and fortunately got Yasu-san to support implementation.

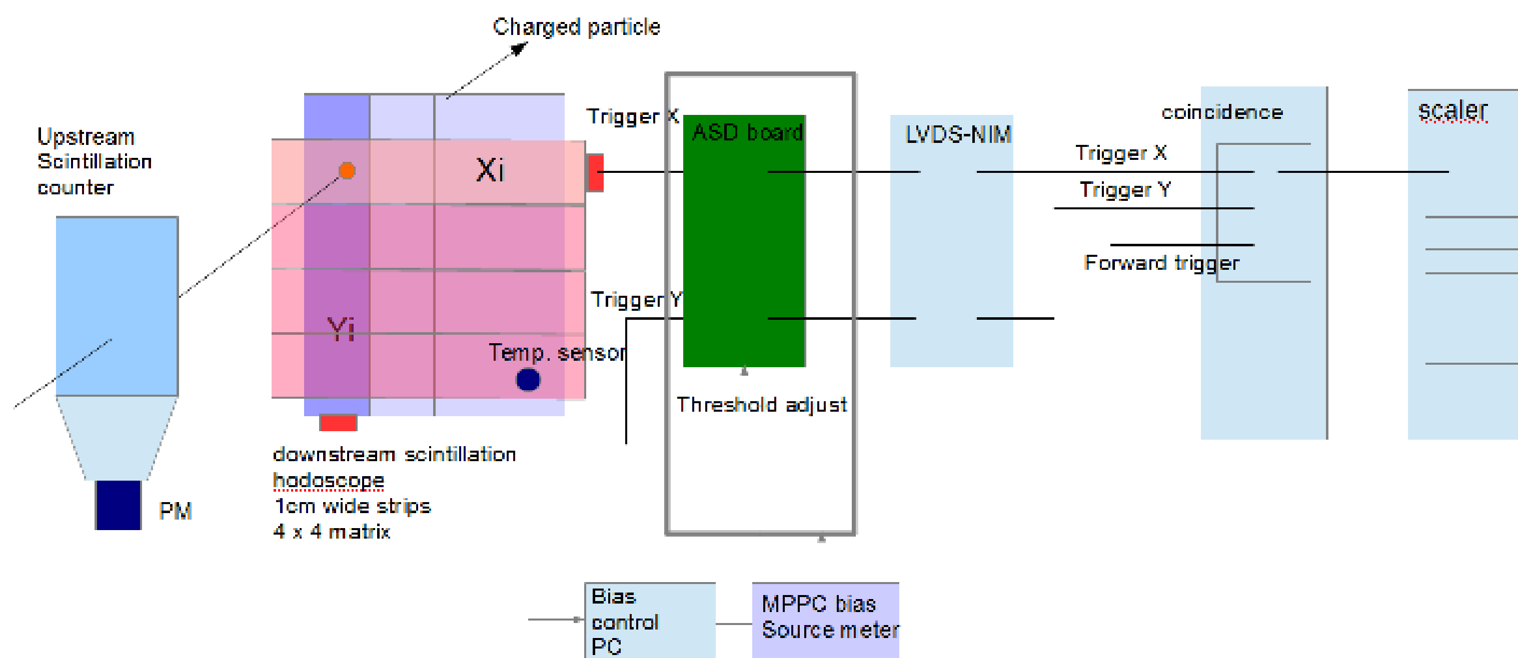
Suehara-san, Ito-san, and Mori-san implemented DAQMW-fpccd in a short period. Unfortunately Suehara-san has gone, and Mori-san has also gone back to his work. Who is to work?

DAQMW-fpccd supports single/multi channels data out. Also “Event” data structure is clearly defined for general purpose, so that it is useful for not only beam test but CTI test and Fe55/Sr90 source test.

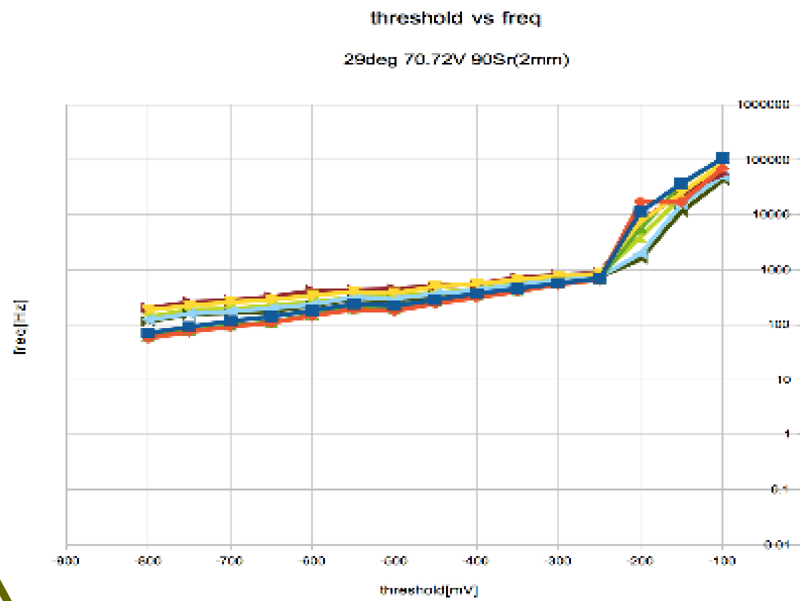
4. Preparation for the beam test

4.3 beam profile monitor

Scintillater + MPPC hodoscopes were prepared by two supporters from Shinshu university. 4+4 channel digital output from ADS board was tested and verified to work, then remaining tasks have been held. The diagram below shows a beam profile monitor.

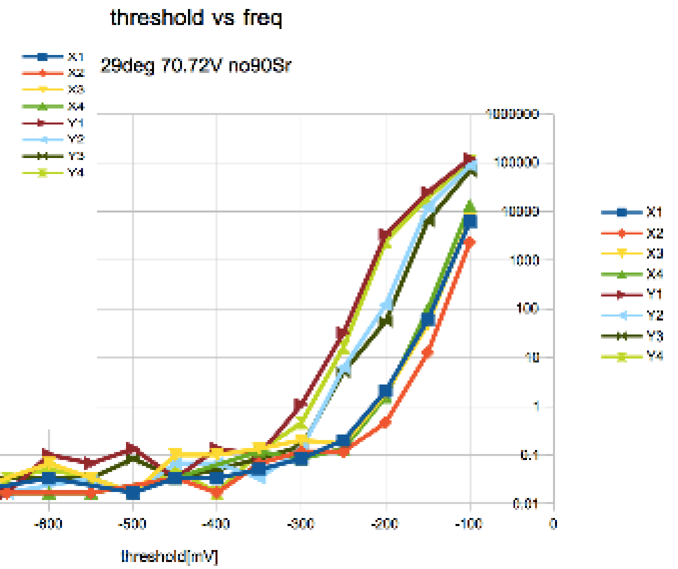


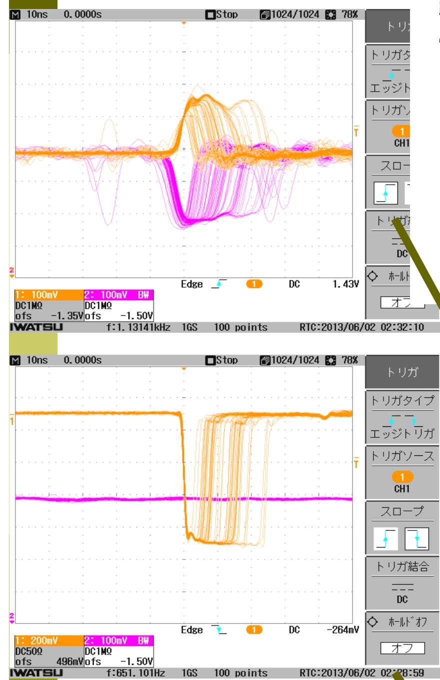
4.3 beam profile monitor (continued)



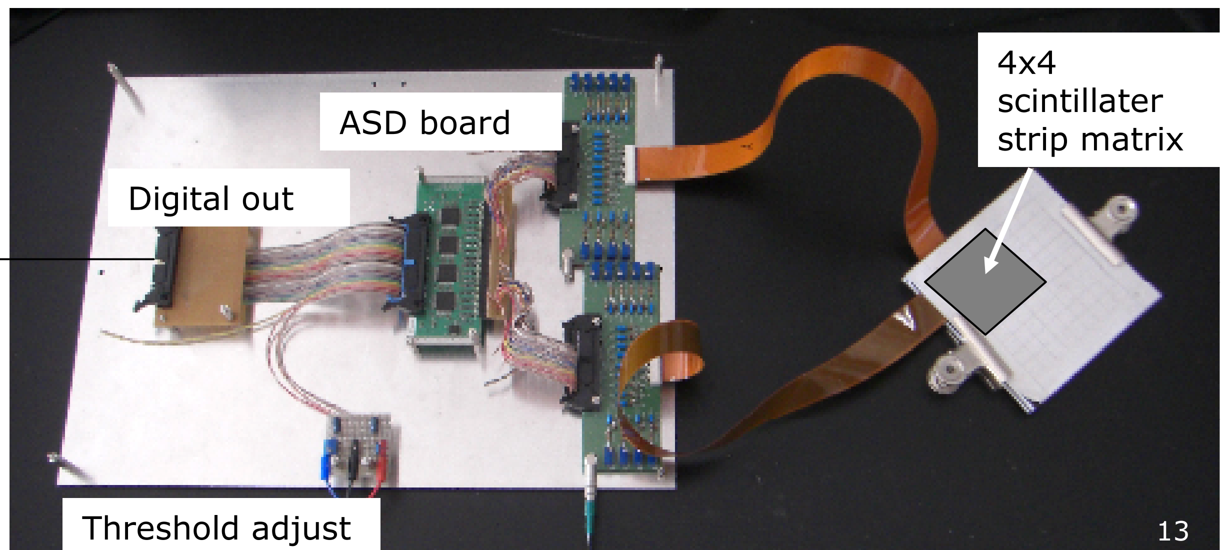
Threshold vs. count rate w/wo Sr90.

Left: w Sr90, Bottom: wo Sr90





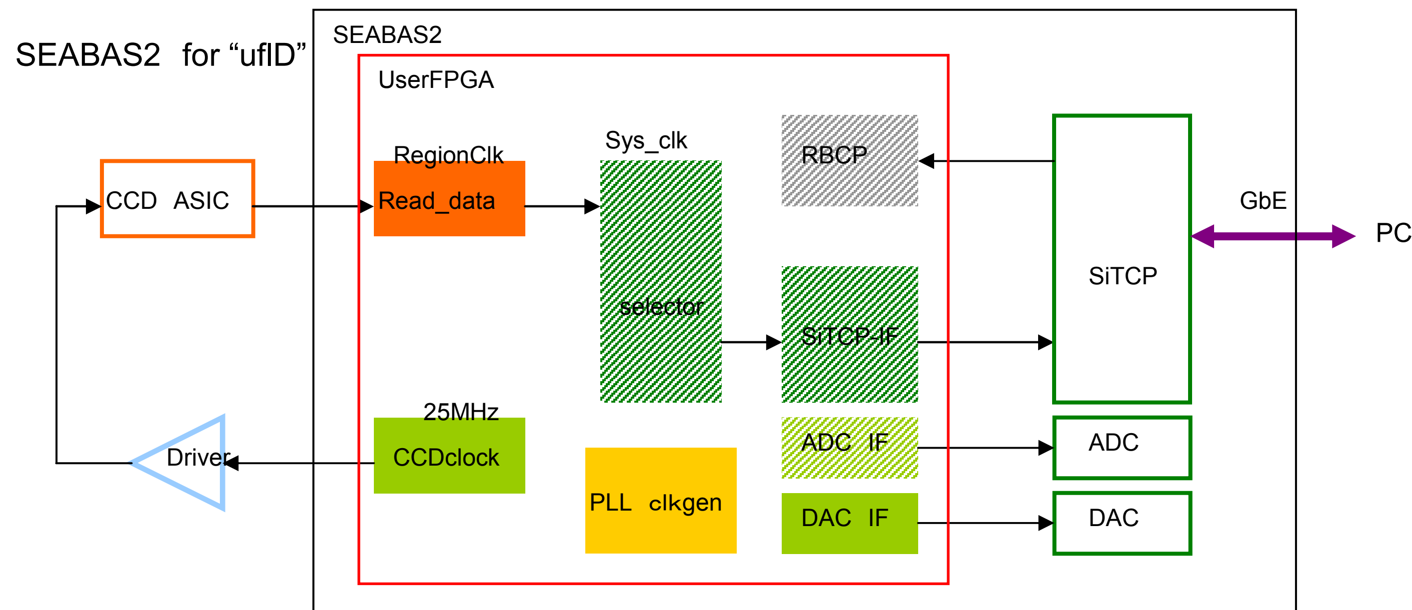
LVDS-NIM conv.



5. Preparation for Fe55/Sr90 test and CTI test

1) Better design from BEAMTEST

Many modules developed and debugged for the beam test are used for updating “uflD” (FPGA design for single CCD test). Blocks of hatched pattern in the diagram are taken from “uflE”.



2) Wide scope of DAQMW-fpccd

Event database of DAQMW-fpccd is well defined to cover all requirements of tests.

6. Summery and open issues in priority

1) 100MHz behavior of AFFROC comes to be well understood.
2) The beam test was canceled. However, work on preparation of beam test reveals some issues.
3) Followings are issues in priority

a) Above 25MHz (2.5Msampling) operation, 100MHz, 125MHz

First need to implement CCD clock timing tuning feature in the FPGA.

Minimize EMI noise to ASIC.

Then see Fe55 signal at 100MHz.

b) CCD clock signal waveform

Study CCD clock signal integrity on FFC transmission cable.

Test driving four CCDs.

Test the large size CCD.