FPCCD VTX Overview

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Outline

- FPCCD sensor R&D
- Beam tests
  - J-PARC
  - CYRIC
- Readout electronics
  - ASIC
  - Peripheral circuit
  - Electronics for beam/bench test
- CO2 cooling for VTX
- FY2014 plan

FPCCD sensor R&D

FY	Sensor
2004	Fully depleted CCD, 24um pixel
2005	Fully depleted CCD, 24um pixel
2006	Fully depleted CCD, 24um pixel
2007	1st FPCCD: small size (6mm^2),12um pixel
2008	2nd FPCCD: small size, 12um pixel (modified output amp)
2009	3rd FPCCD: small size, 12, 9.6, 8, 6um pixel
2010	4th FPCCD: small size, 12, 9.6, 8, 6um pixel (modified process) Thin wafer:50um
2011	Small size, 12, 9.6, 8, 6um pixel (modified process), thin wafer
2012	Small size, 6um pixel, 4ch, different H-register size Large size (12x64mm2), 6,8,12um pixel, 8ch Small size, 6um pixel, thin wafer (for beam test)
2013	Small size, 5um pixel ? Large size, thin wafer ?

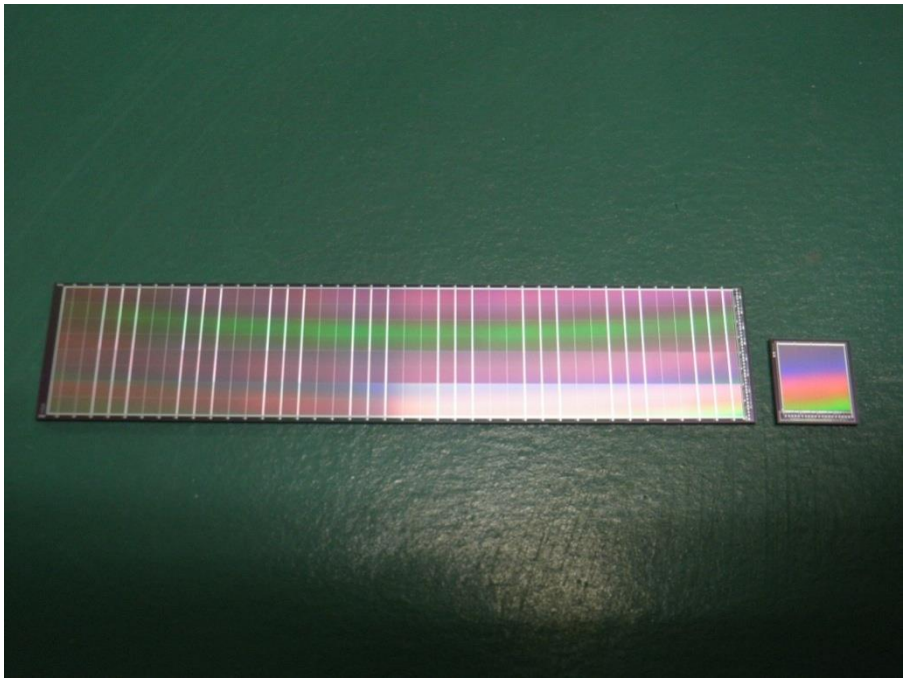
FPCCD sensor R&D

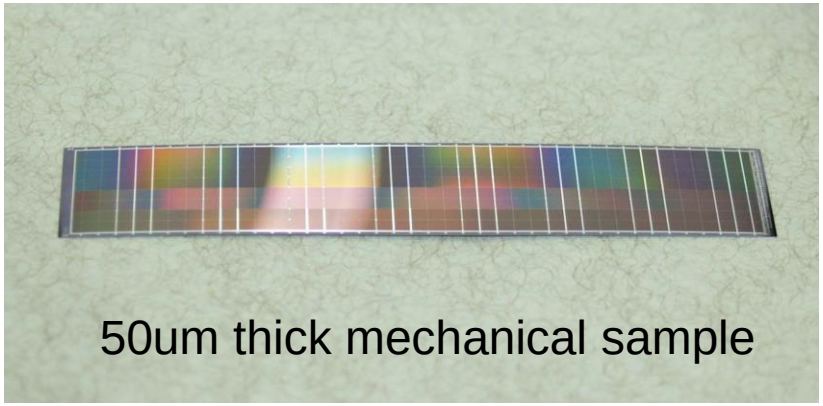
- Original plan for sensor R&D in FY2013
  - Large size thin wafer
  - Small size 5um pixel
- Achievement
  - Large size FPCCD
    - Same format as 2012 large prototype
    - Mechanical prototypes of thin wafer
    - Working prototypes of thin wafer (bare chip)
    - Working prototypes of thick wafer (bare chip)
  - Small size FPCCD
    - Packaged prototypes with 6um pixel for radiation damage test (Same format as 2012 small prototype)

FPCCD sensor R&D

- Test of sensors using beta/X-ray source
  - Basic study of the sensors using checking source is very important
  - But we did not have enough time/manpower due to preparation for beam tests and others
  - The following sensor characterization has to be done soon for both small and large prototypes
    - Dark current as a function of temperature/pixel-size/irradiation
    - Energy resolution for 5.9 keV X-ray
    - Charge transfer inefficiency as a function of various parameters
    - S/N for beta ray
    - Charge spread for charged track
    - Full-well capacity
    - Noise characteristics of bare chip system
  - Improvement of DAQ system might be necessary for efficient study of these characteristics

FPCCD sensors





50um thick mechanical sample

Beam tests

- Beam test at J-PARC 1GeV beam line
  - Purpose: study of spatial resolution
  - Machine time was scheduled in June
  - Preparation for the beam test
    - Thinned (t=50um) wafer
    - DAQ system for the beam test
    - etc.
  - Canceled due to the accident at J-PARC
  - There is possibility to do it after October 2014

Beam tests

- Neutron damage test at CYRIC
  - CCD sample was irradiated by neutron beam at CYRIC of Tohoku University
  - Detail will be reported by Ito-san

ASIC R&D

- Original plan for R&D of ASIC and peripheral circuit
  - 2nd AFFROC prototype, if necessary
  - Start R&D for peripheral circuit, such as
    - Multiplexer (SER-DES) ASIC
    - Clock driver ASIC
    - Data compression circuit
- Achievement
  - No progress

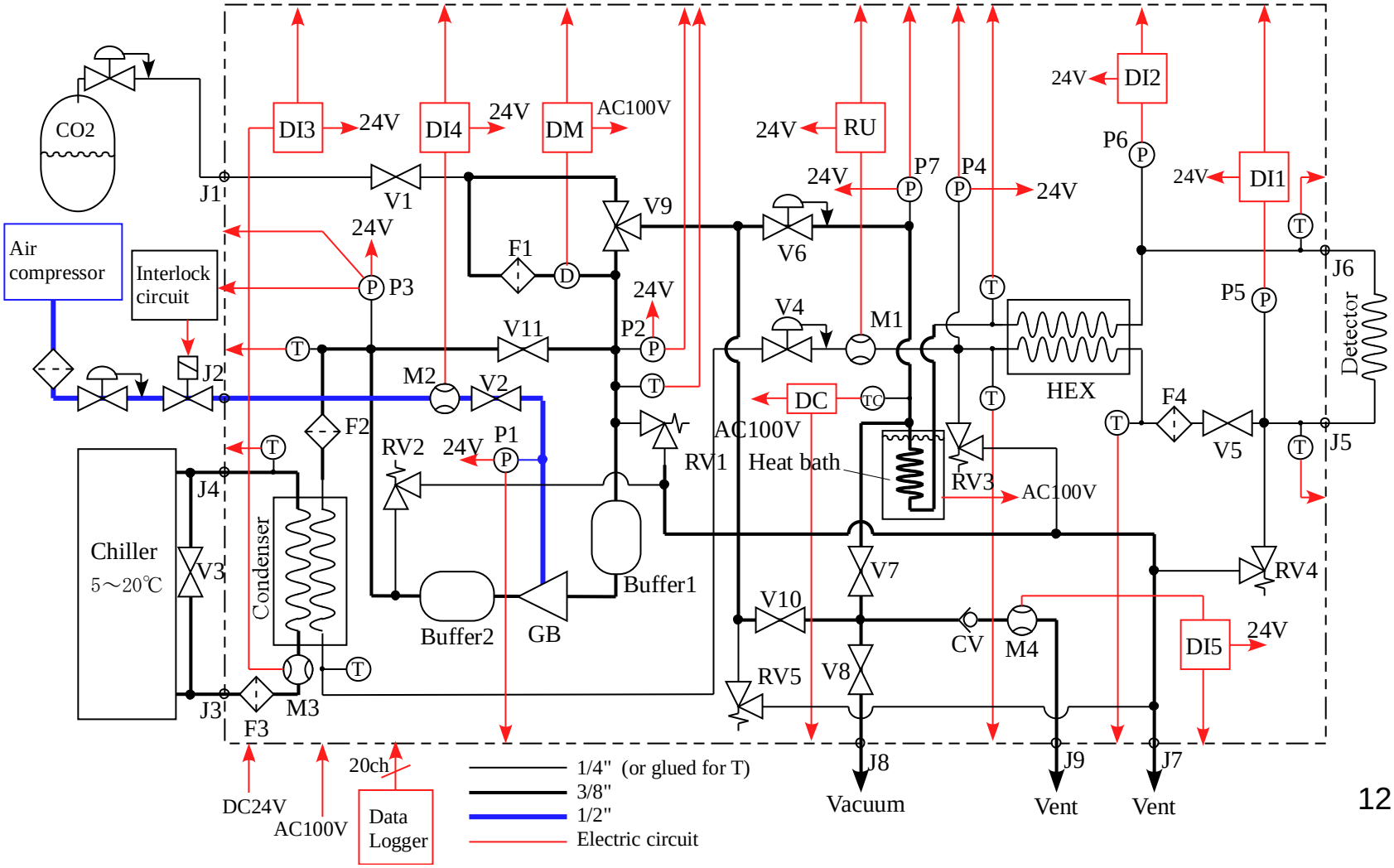
Readout electronics

- Electronics for beam/bench test
  - Study of readout system of CCD-AFFROC board (CAB) and SEABAS2
  - Data acquisition system for the beam test
  - Test board for bare chips
  - Detail will be reported by Sato-san

Cooling system for VTX

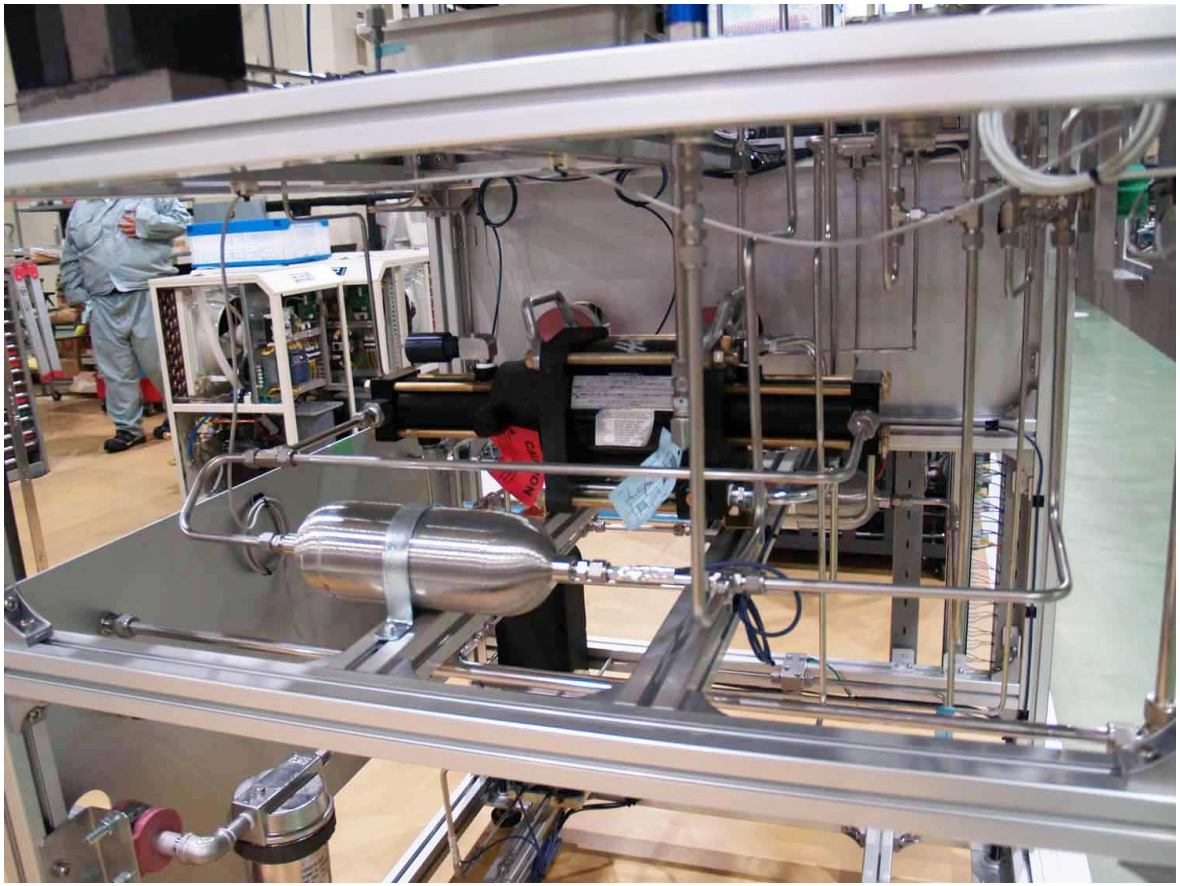
- R&D of 2-phase CO2 cooling is being carried out for FPCCD VTX (and TPC)
- A prototype of circulating cooling system has been constructed
  - Cooling temperature: between −40℃ and +15℃
  - The system was constructed 2013 spring
  - But it took a long time for safety inspection by KEK high-pressure gas committee
  - The system has just become ready for test on December 6th

Cooling system for VTX



Cooling system for VTX

- Prototype of 2-phase CO2 cooling system under construction

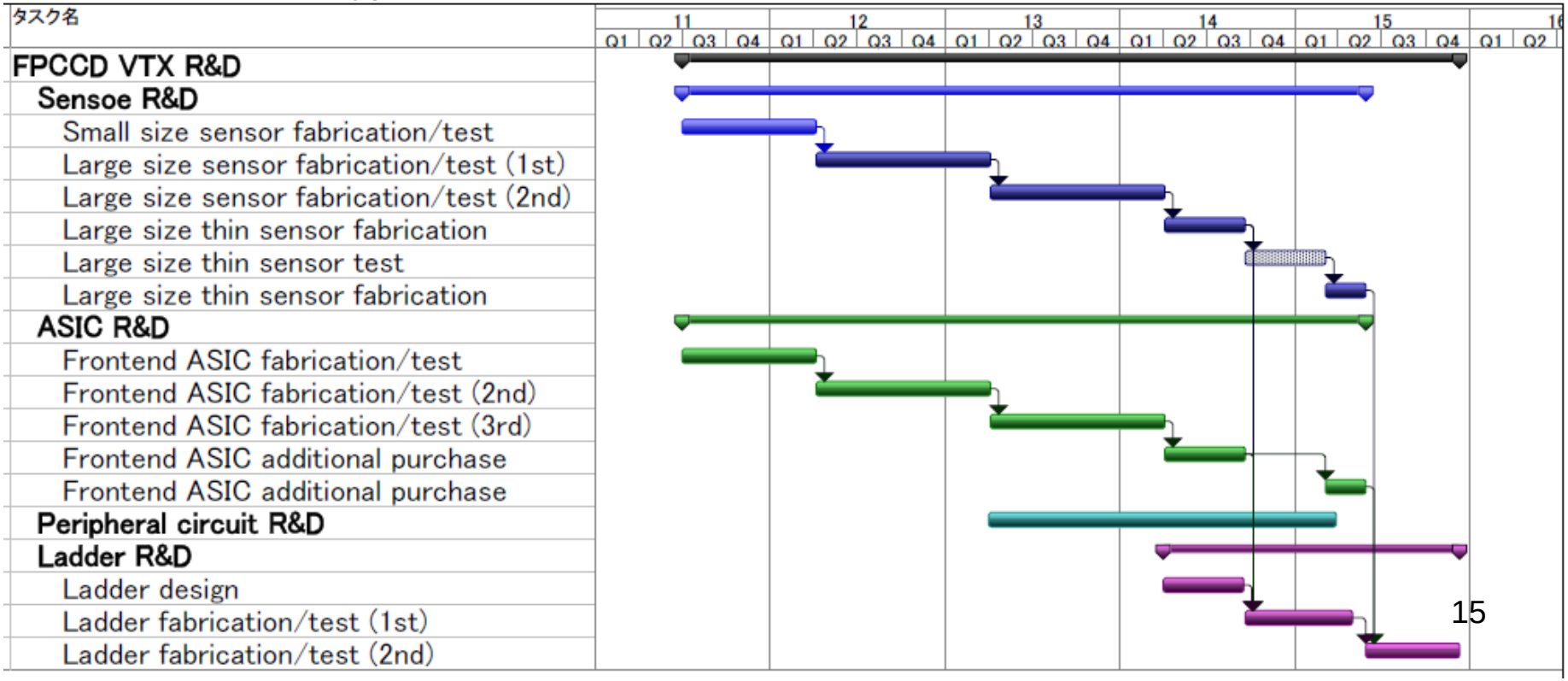


FY2014 plan

- Neutron damage tests
  - 2nd neutron damage test at CYRIC
- Beam test
  - Beam test at J-PARC, if possible
- FPCCD prototypes
  - 2nd large prototype (?)
  - Small prototype with 5um pixels (?)
- Readout electronics
  - Start R&D for peripheral circuit
- Ladder R&D
  - Mechanical structure
  - Bare chip test board with ladder size

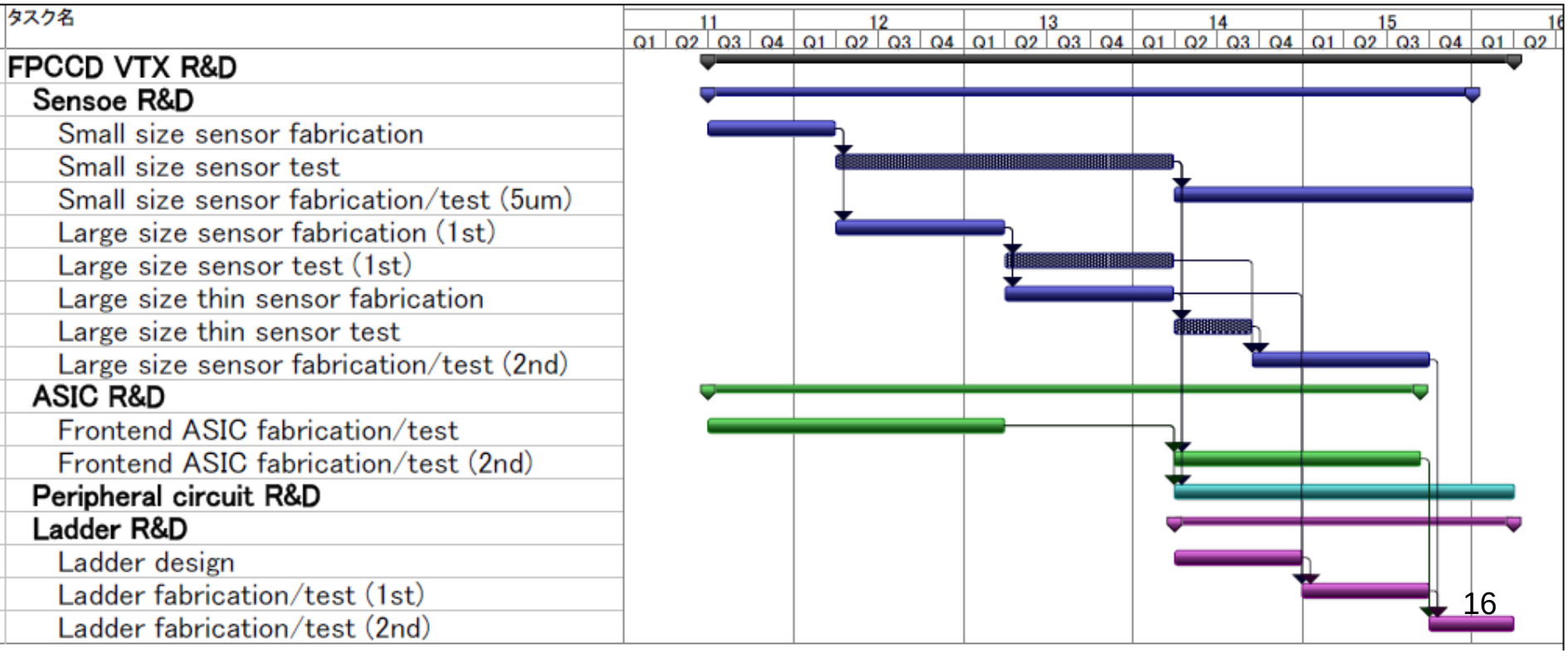
Long-term plan

- Original plan for JSPS funding
  - Goal
    - Prototype sensor of 1cmx6cm size, ~5um pixel size
    - Prototype front-end ASIC for the prototype sensor
    - Prototype ladder with CCDs and ASICs



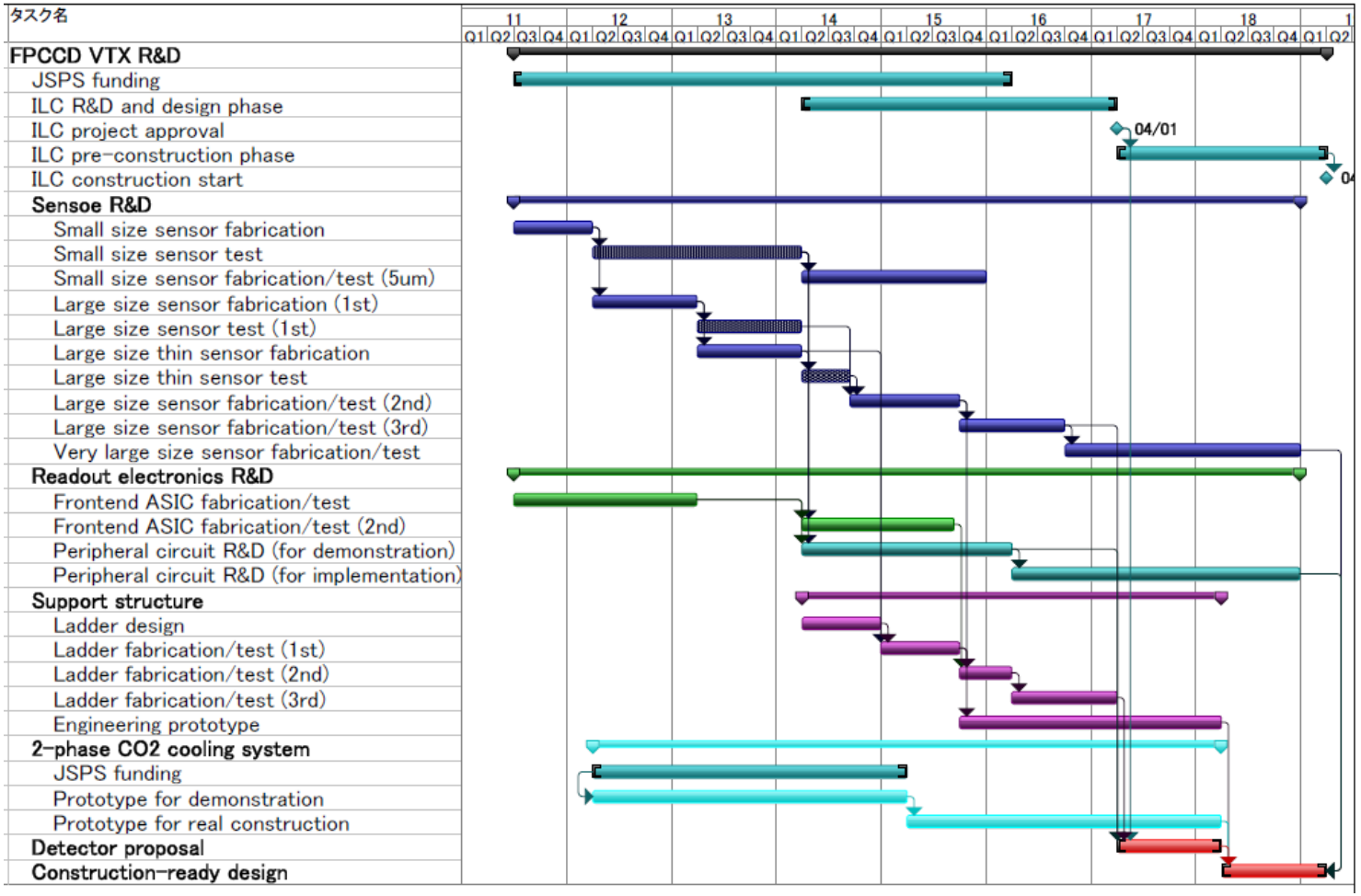
Long-term plan

- Modified plan for JSPS funding
  - Goal is same
  - Timeline has been modified



Long-term plan

- Longer term plan for next 5 years
  - We assume we will start construction of ILC in 5 years (ILC project approval in 3 years)
  - 2014~2016: R&D and design phase
  - 2017~2018: Pre-construction phase



Backup slides

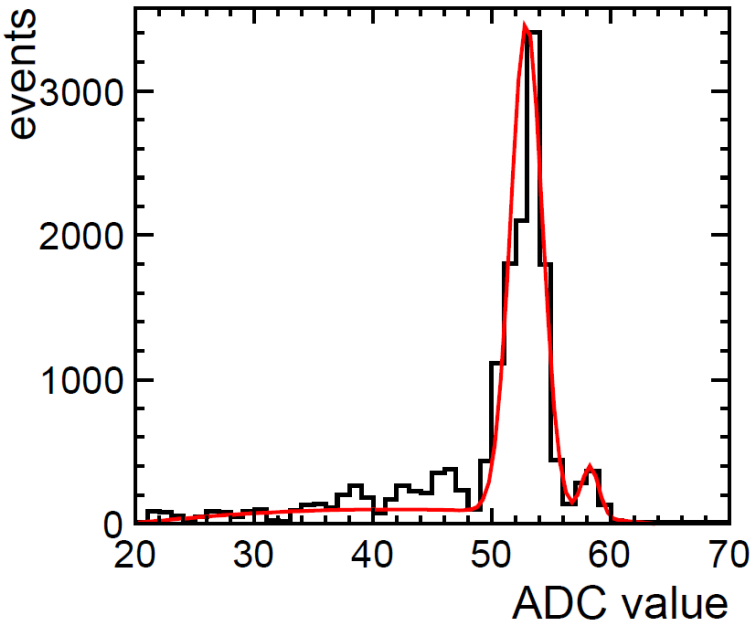
R&D goal

- FPCCD sensors
  - Pixel size; 6um → 5um (?)
  - Chip size;1cmx6.5cm
  - Speed >10Mpix/s
  - F.W.C. > 10000 e(?)
  - Power <10mW/ch
  - Rad. Tolerance >$1x10^{13}e/cm^2$ (=$1x10^{12}/cm^2/y$ x 3y x safety factor 3)
- Readout ASIC
  - Speed > 10Mpix/s
  - Power < 6mW/ch
  - Noise < 30 electrons
- Peripheral circuit
  - Clock driver
  - Data suppression
  - Etc.
- Engineering R&D
  - Over-all design
  - Low-mass ladder
  - Cooling system (~-40℃)
  - Support structure

  ➔ Engineering prototype

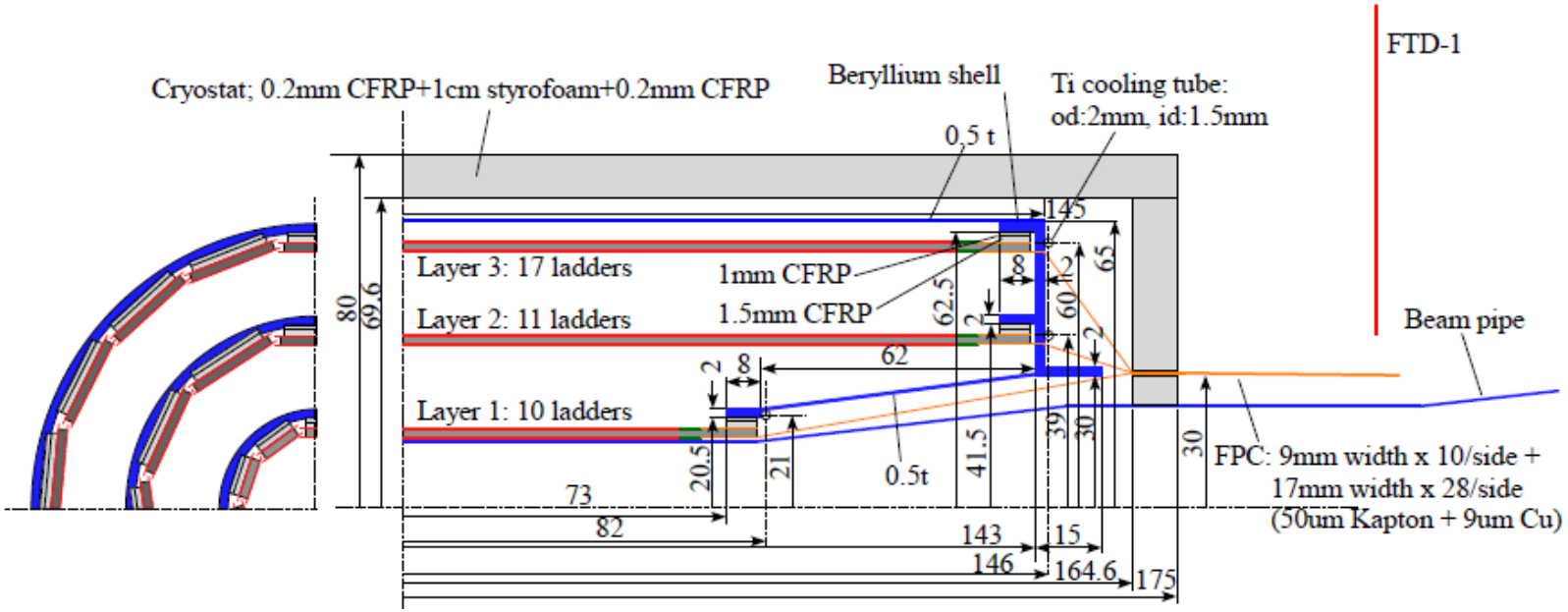
R&D status

- 6um pixel works if horizontal register is 6x12um^2 or larger
- Full-well capacity (~5000e) is still to be improved (>10000e)
- Large prototype works!
- Beautiful Fe55 X-ray spectrum is obtained using an FPCCD of 12um pixel at 2.5Mpix/s speed
- Test of FPCCDs of 6um pixels using new readout electronics (new CCD board with new FE ASIC (AFFROC-1)+ SEABAS2-board) on going



Vertex detector for ILD

- Structure
  - Barrel part only: |z|=62.5/125 mm
  - Double-sided layer x3
  - R=16~60mm
  - |cosθ|<0.97
- Minimization of material budget of ladders is a big challenge
  - 0.3%X0/ladder = 0.15%X0/layer



FPCCD VTX for ILD

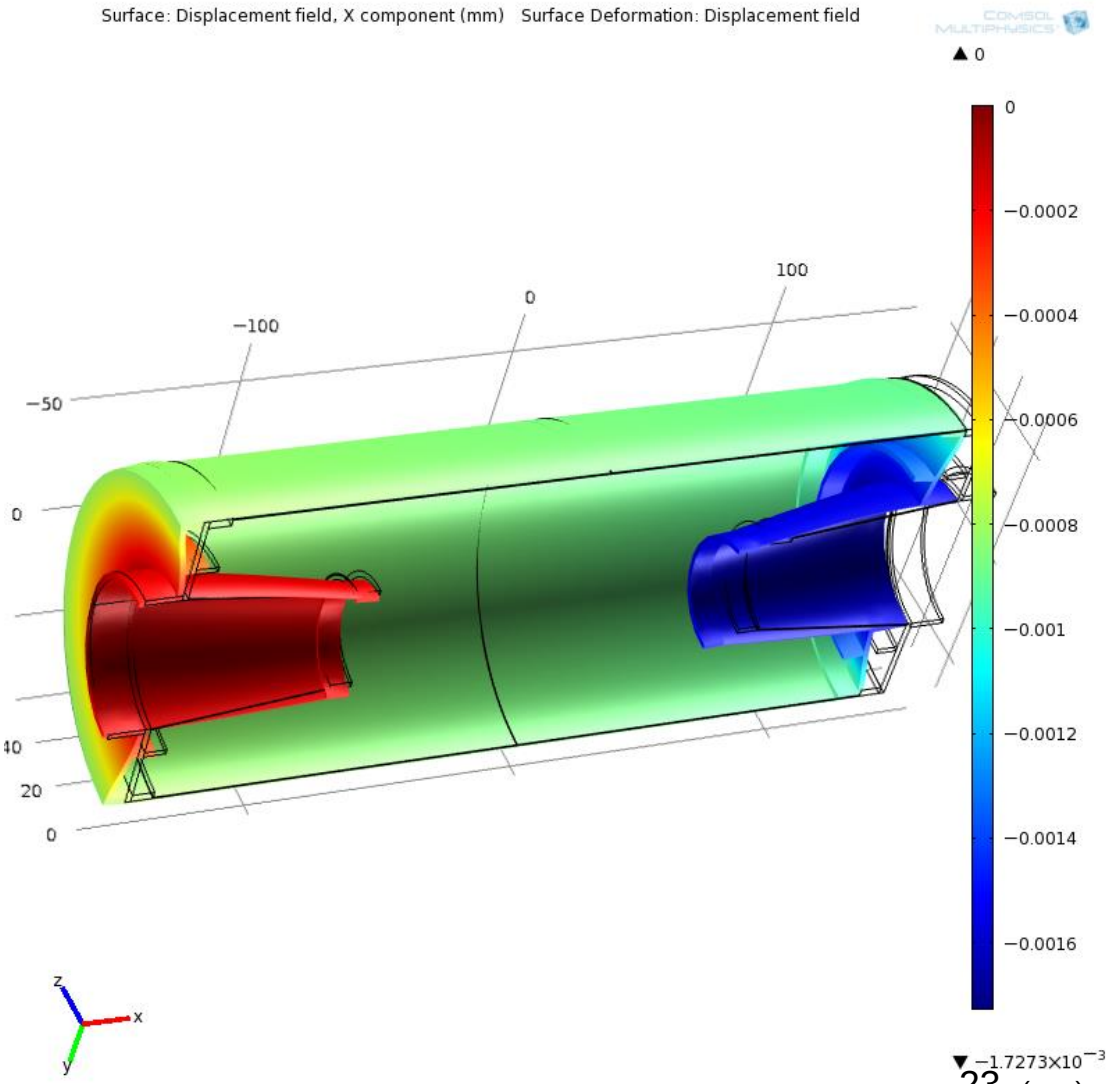
- Pixel size
  - 5um for inner two layers
  - 10um for outer four layers (previously 5um)

	Pixel size (in)	Pixel size (out)	# of ch /chip (in)	# of ch /chip (out)	# of ch (total)	Power consumption
Old design	5 um	5 um	28	56	7392	111 W
New design	5 um	10 um	15	15	2280	34 W

- Power consumption
  - ~40W for on-chip amp and ASICs inside cryostat
  - ~400W for clock drivers and data processing circuits outside the cryostat
  - ~?? W for the aluminum gate line on CCD

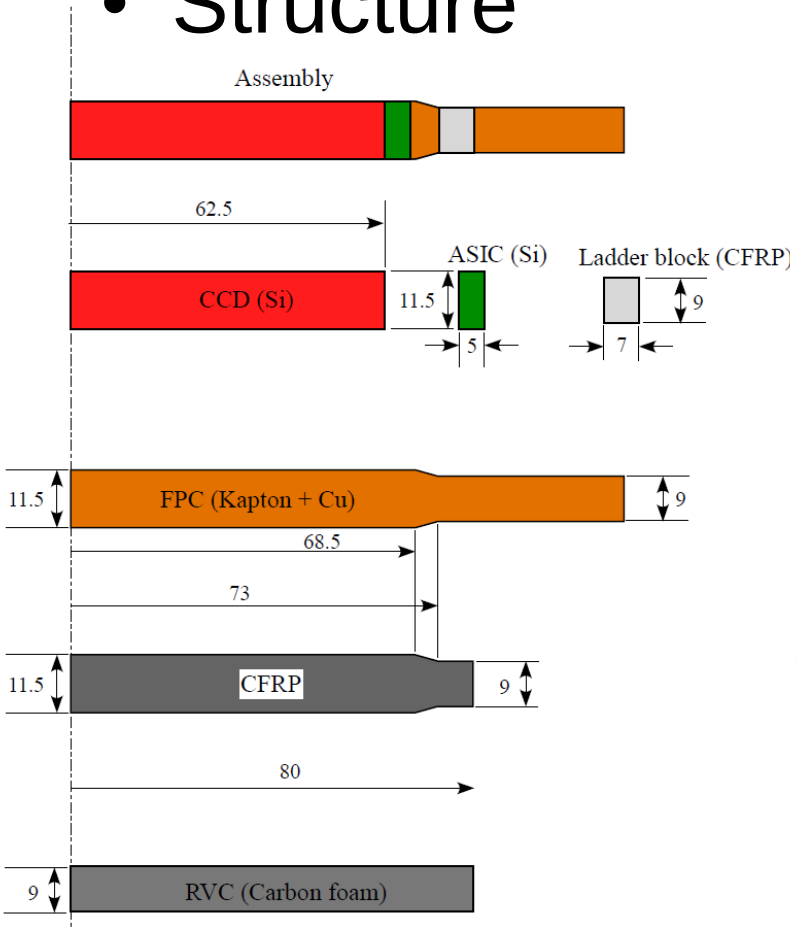
Beryllium support shell

- FEA calculation of deformation
  - 1kgf is applied in z-direction
  - Maximum deformation is less than 2μm
  - Total weight is less than 500g → max force caused by the friction at the kinematic mount would be less than 500gf

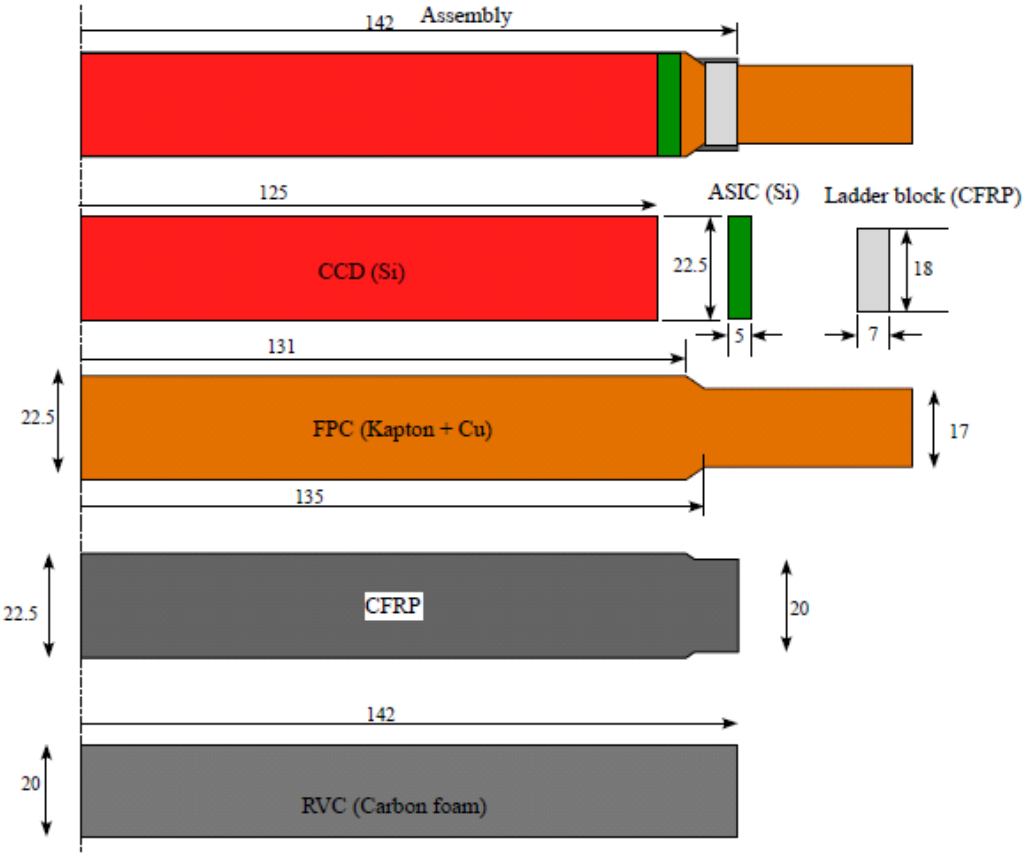


Ladder

- Structure



Layer-1



Layer-2,3

Cooling system

- Cooling tube
  - Titanium tube 2mm o.d. and 1.5mm i.d. is attached to the VTX endplate near the endplate annuli
- The return line of the cooling tube is also used for the cooling of the junction box
- 4 tubes/side run along the beam pipe between the vertex detector and the end of the inner support tube