

Plans at LAL – Visit to SKKU

Responsable du groupe
Roman Pöschl

Physics studies

J. Rouëné, F. Richard, D.
Zerwas, M.S. Amjad,
E. Kou

Detector R&D

Tests Ecal
Ecal: J. Rouëné (→ Summer
2014),
T. Frisson (¶2013)

Integration Ecal:
J. Bonis (SDTM),
A. Thiebault (SDTM)
P. Cornebise (SERDI)

Integration ILD:
C. Bourgeois (SDTM),
A. Gonnin (SDTM)

Algorithms and beam Test analysis

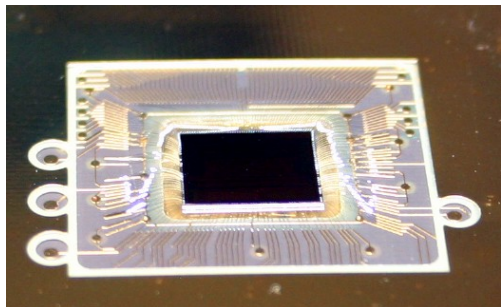
N. van der Kolk
(with LLR until Sept. 2014),
B Kegl

Request for P2IO postdoc

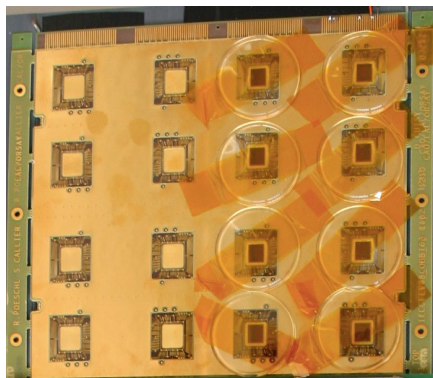
Detector R&D

- LAL Contributions -

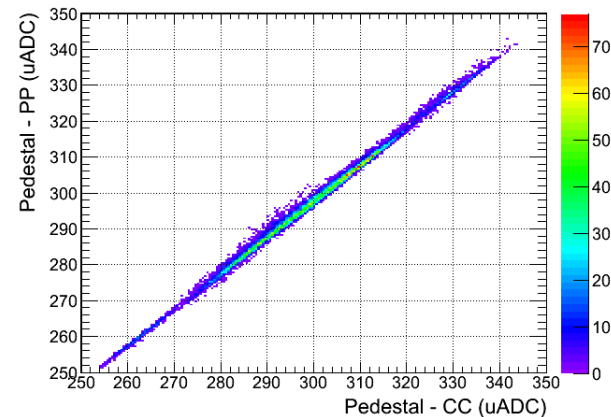
Realisation and tests of front end electronics for the Ecal



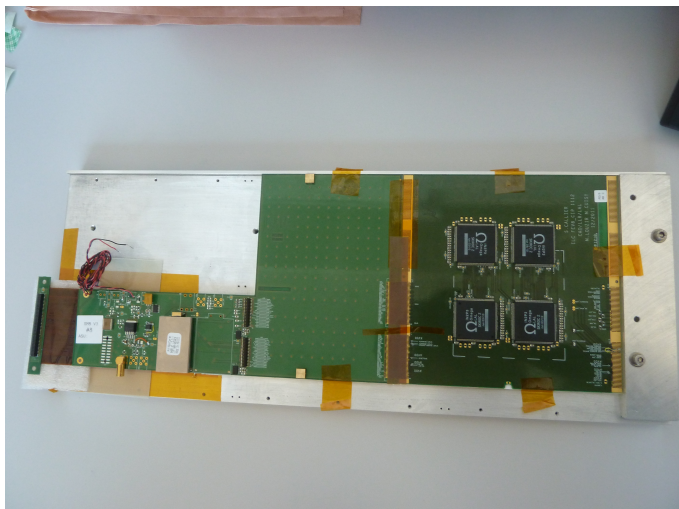
SKIROC chip as part of series of chips for highly granular calorimeters



Flat PCB,
The « impossible »
becomes real



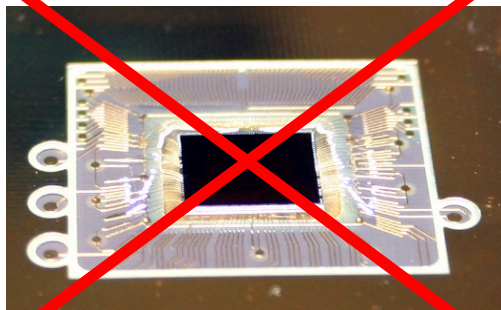
Characterisation on electronics
Tests of power pulsing
Test beam analysis (see also later)



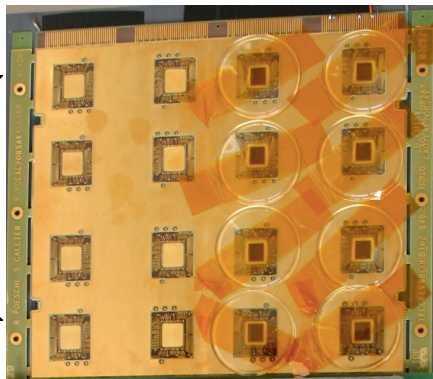
Assembly of layers for beam test

Detector R&D

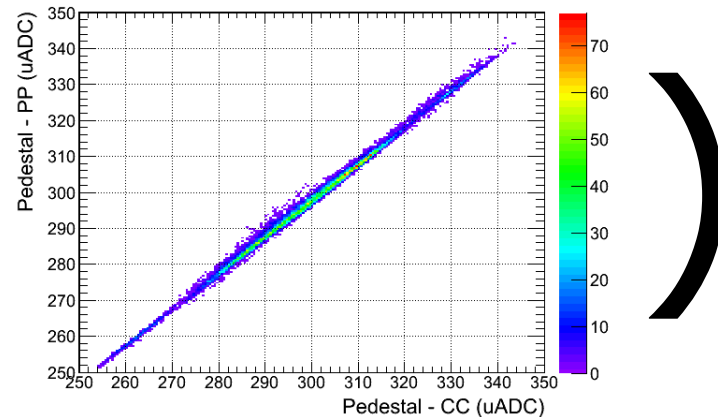
- LAL Plans -



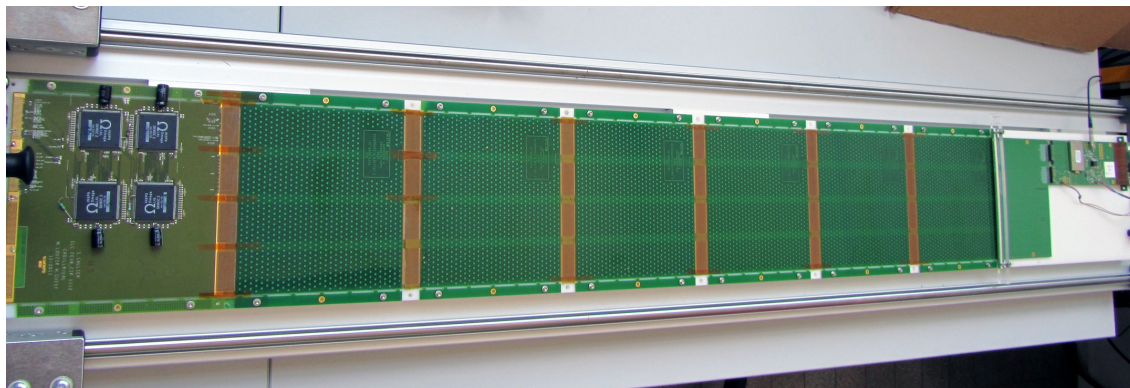
OMEGA is own institute
 No clear way how to
 Continue collaboration



Will follow up as much
 as possible (see also later)



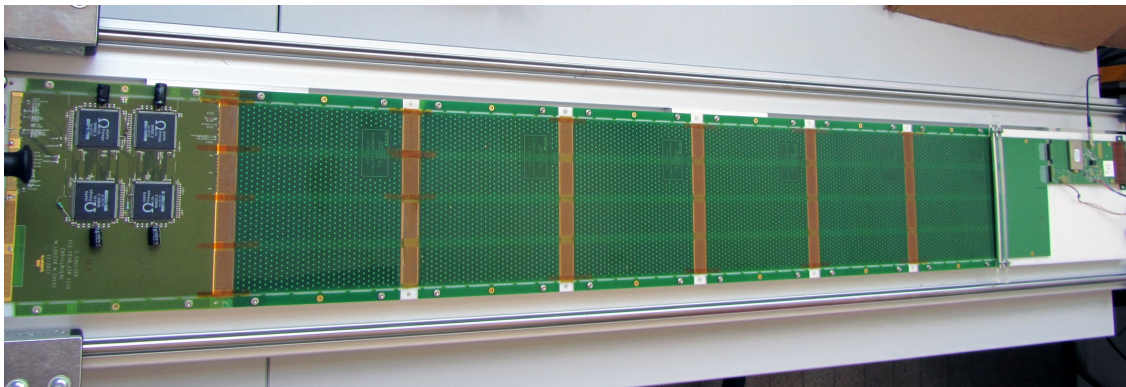
Will finish 2008, 2012 papers
 Power pulsing analysis
 Beyond ??????



Towards long layer ...

Detector R&D

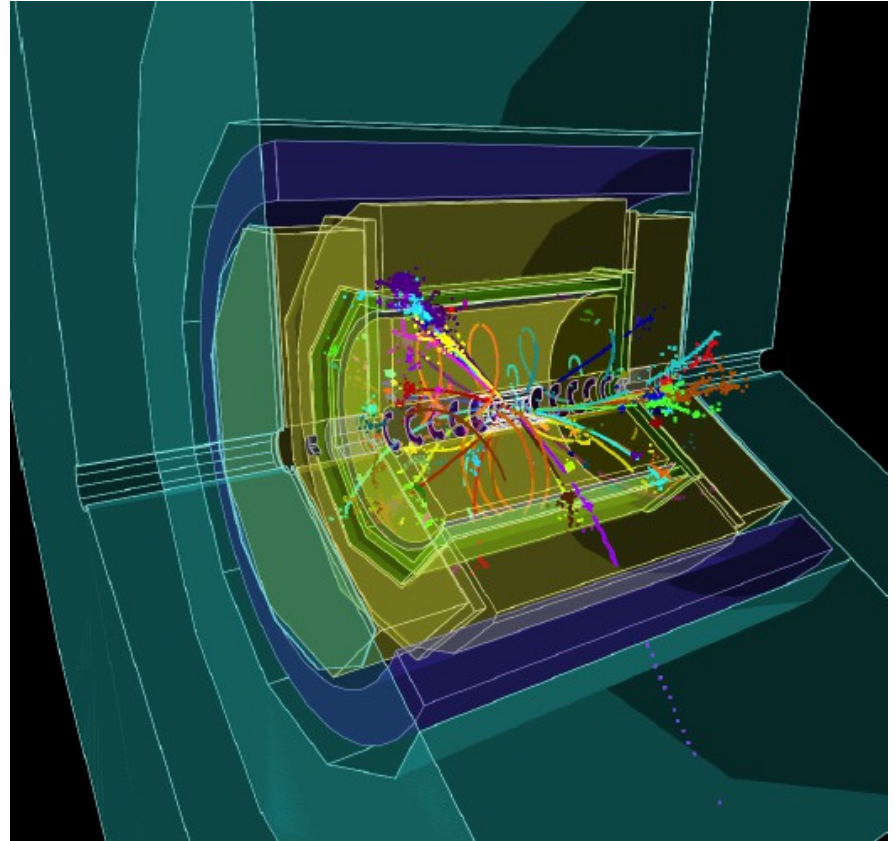
- Towards long/real layers -



- Study of long slab signals (Winter 2013/2014)
- Revision of interconnection according to PCB specs
- Automatic measurement/recording across interconnections
Completion of measurement station in Spring 2014
- Evaluation of mechanical stress during ASU positioning in H/U structure
Order of a sensor device to measure pressure during positioning
Tolerances of PCB dimensions, wafer dimensions
=> Set of specifications for automatised procedure
answers until spring 2014
Application of results for assembly of long slab, scrutinisation of assembly tools
(including monitoring of elements) at LAL to assemble long slabs
=> Full robotic system, semi-robotic system, in-house assembly or outsourcing ?
First proposal until end of 2014

Visit to SKKU

1-6 November 2013
Funding through FKPPPL



Reminder FEV_COB



- Interface board with Chip On Board
- Assures compact calorimeter

- Not trivial specs

Ultrathin : 9 layers with thickness of about 1.2mm

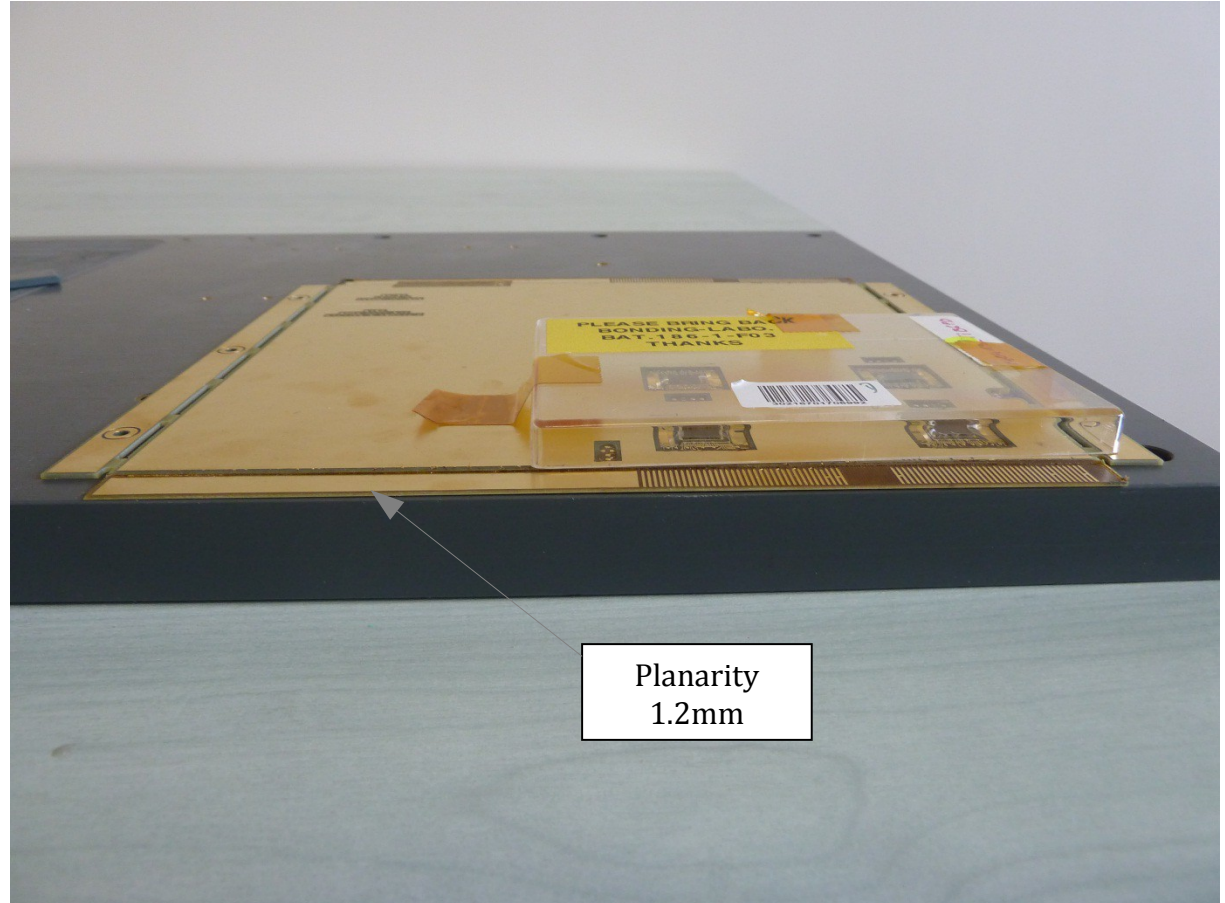
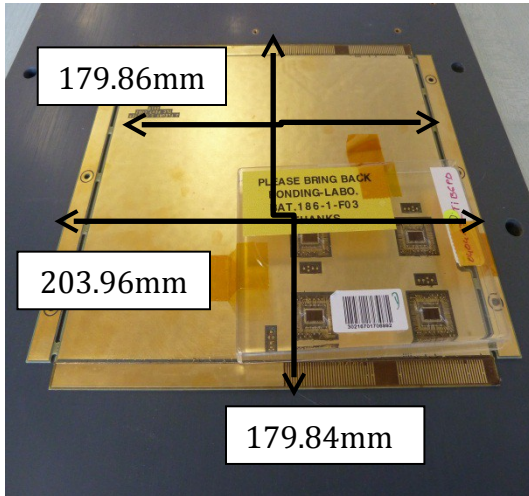
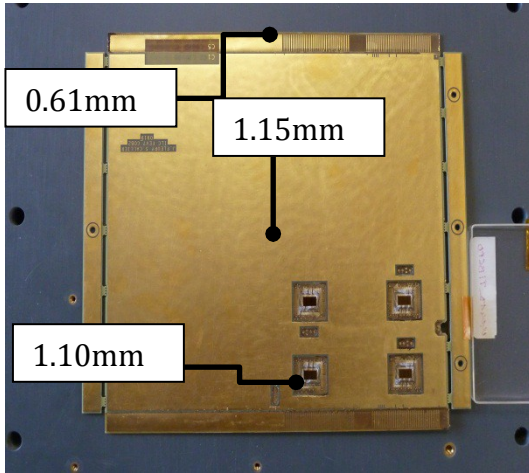
Deviation of total planarity of about 0.5 mm (3mm is industrial standard)

However it's now there in a first version

- Design and routing OMEGA/LAL
- Fabrication end of 2012
- Metrology at LAL
- Chips mounted beginning of 2013 by CERN bonding lab
- First tests in summer 2013 at LAL
See Annecy meeting
Characterisation continues as much as possible
Roeune/Callier (R.P.)

FEV7_COB – Test production by EOS

... under supervision of SKKU at Suwon



- Very promising from mechanical point of view
(Better than anything we have ever found in Europe)
- Could not be tested since it came somewhat late

Meeting at SKKU

- ANME lab of SKKU is accelerator group for medical applications
Recent realisations: Compact cyclotron, plan for short LC for computer tomography
- Prof. Chai has "history" in particle physics (PHENIX) and wants to keep competence for detector instrumentation in his group
Contact since 2009, introduced to CALICE by Henri Videau
Internship of Korean students at OMEGA
- 2 1/2 days of meetings/industrial contacts
 - Presentation of SKKU projects, Cyclotron visit
 - 1/2 day of CALICE i.e. Ecal seminar
 - General discussions on next steps

Many thanks to Seung-hyun and Ho-Seung for the efficient meeting
- Visit to HSDGT company for PCB production
Solid company but not very specialised for high tech i.e. multilayer PCBs
Still will send them our files

Meeting with EOS company

- EOS company specialised for thin multilayer PCBs
PCB producer for Missile, space, aerospace and medical applications
Capability of mass production
See brochure
- First visit to EOS company by R.P. in November 2011
Arranged by SKKU
Delivery of FEV7_COB in April 2012
- 1 afternoon meeting on 5/11/13 at SKKU
- EOS represented by
[Eun Duck Oh](#) General Manager Quality and Engineering
[Alex Kim](#) Assistant General Manager Overseas Sales Dpt.
- ECAL represented by Stephane Callier and R.P.
- Lot of detailed technical discussion between mainly
Stephane and Mr. Oh

CAO/LAL/ORSAY

Experiment : ILC

Board : FEV8_COB

PCB FEV8_COB is made of the assembly of the 2 pcs number 1210 and 1213 with electrical connection of GND

Assembly process :

After manufacturing, both board should be assembled together with an adhesive conductive tape or a conductive glue under specific operation conditions (low temperature, limited pressure on boards) to avoid any board bending.

=> GND copper plane of layer C2 of PCB 1210 and copper plane of layer Top2 of PCB 1213 will be electrically connected.

Top layer of PCB is connected to GND.

06/07/2012

D.CUISY +33 1 64 46 85 36

- EOS understood the step from a 4 chip board to a 16 chip board

- Discussion emerged around fabrication process
2 piece board -> 1 piece board
(see demonstration)

- EOS will produce also 2 piece Board but expressed confidence that they can produce the board in one piece
Would relax mechanical stress during curing

Btw.: EOS able to realise cold pressing of PCBs

Cooperation with EOS

R. POESCHL S. CALLIER ILC FEV8_COB 1210 CAO/LAL/ORSAY D. CUISY 0164468536

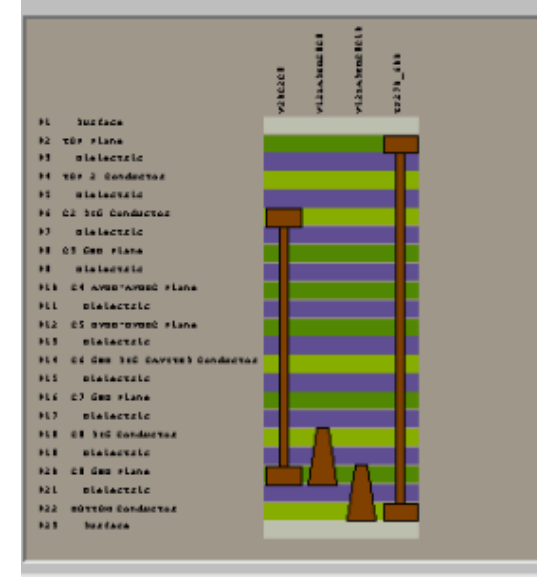
Layout Cross Section

	Subclass Name	Type	Thickness (MM)	Dielectric Constant	Loss Tangent	Shield	Width (MM)	Impedance (ohm)	Coupling Type	Spacing (MM)	DWZ0 (ohm)
1		SURFACE		1	0						
2	TOP	PLANE	0.02	1	0						
3		DIELECTRIC	0.16	4.5	0.035						
4	TOP 2	CONDUCTOR	0.02	4.5	0.035		0.120	55.168	NONE		
5		DIELECTRIC	0.1	4.5	0.035						
6	C2 SIG	CONDUCTOR	0.035	1	0.035		0.120	37.674	EDGE	0.180	70.934
7		DIELECTRIC	0.06	4.5	0.035						
8	C3 GND	PLANE	0.014	1	0.035						
9		DIELECTRIC	0.075	4.5	0.035						
10	C4 AVDD-AVDDC	PLANE	0.014	1	0.035						
11		DIELECTRIC	0.06	4.5	0.035						
12	C5 DVDD-DVDDC	PLANE	0.035	1	0.035						
13		DIELECTRIC	0.12	4.5	0.035						
14	C6 GND SIG CAVITES	CONDUCTOR	0.035	1	0.035		0.120	33.626	EDGE	0.180	65.645
15		DIELECTRIC	0.06	4.5	0.035						
16	C7 GND	PLANE	0.014	1	0.035						
17		DIELECTRIC	0.075	4.5	0.035						
18	C8 SIG	CONDUCTOR	0.014	1	0.035		0.120	29.324	NONE		
19		DIELECTRIC	0.06	4.5	0.035						
20	C9 GND	PLANE	0.035	1	0.035						
21		DIELECTRIC	0.06	4.5	0.035						
22	BOTTOM	CONDUCTOR	0.04	1	0		0.120	44.724	NONE		
23		SURFACE		1	0						

Total Thickness: 1.106 MM
 Layer Type: ALL
 Material: ALL
 Field to Set: Thickness
 Value to Set:
 Update Fields

Show Single Impedance
 Show Diff Impedance

OK Apply Cancel Refresh Materials > Help



- Discussion of details of layer arrangements and drilling holes
- Questions on specifications
 - Main spec formulated: Maximum deviation from planarity 0.5mm
 - Let EOS propose reasonable thickness of board under this constraint

Next steps:

- Stephane will revise layout of FEV_COB PCB to provide proper alimentation of ASICs
- Layout will be validated by Specification Control Team of EOS
 - > Will propose modifications if necessary
- Production of FEV_COB PCB

EOS Conclusion

Concluding remark by EOS Engineer

“We will make you a perfect board”

Well, let's hope for the best