ILC ECAL activities at Tokyo

Komamiya-lab (Dept. of Physics):

on **silicon ECAL**:

Sachio KOMAMIYA,
Daniel JEANS,
Yoshio KAMIYA,
Shion CHEN,
Chihiro KOZAKAI

(also: Ultra Cold Neutron experiments, ATLAS, Shintake monitor@ATF2)

<u>activities</u>

Silicon sensor electrical measurements
SiECAL optimisation simulation studies
Physics proto testbeam data analysis

Ootani-lab (ICEPP):

on **scintillator ECAL**:

Wataru OOTANI,
Sei IEKI (“seconded” from Satoru Yamashita's lab)

(also: MEG experiment)

Scintillator strip optimisation
MPPC development

Near-term plans for SiECAL side

Hardware (led by Yoshio Kamiya):

Measure radiation tolerance to sensors to neutrons
- Suitable reactor identified in Japan (good for baby chip)

I-V, C-V, cosmic/source signal before and after radiation

Issues/questions
- Would like to read sensor signals with full DAQ system
  - (by-products:
    - learn how to use system,
    - develop into cosmic/beam ASU calibration system)
  - Need help from Fr to get pieces

In parallel, look for PCB producer for FeVx
- Which version?
- Maybe start with conservative design,
  - later investigate more aggressive one?
- Need design files from Omega / LLR
- To instrument the PCB, need some SKIROC ASICs

Near-term plans for SiECAL side

Optimisation/Software (led by Daniel)

2-particle separation (photon-photon, photon-pion)
- ILD simulation – different ECAL models
- CALICE data & simulation

- Using PandoraPFA (started) and GARLIC (planned)

GARLIC photon finding algorithm development
- have some ideas for improvements

Questions:
- define “default” ECAL
  - (maybe wait for re-baselined ILD models before doing too much)
- which parameters to change

- is our current cross-talk modeling good enough?
- What is realistic/expected intra-channel xtalk level?

Other more general ideas/questions

If statement of interest for hosting ILC arrives (and it may arrive soon),
we should have some procedure by which groups can join us,
and a list of open work packages we can ask them to choose from

This procedure will also help us to better organise our effort

We may want to be more proactive about inviting groups
University, lab seminars
for now, focus on Japan/Korea/China and Europe?
(at least while there are 2 detectors...)

Need detailed cost model for silicon:
silicon cost proportional to # wafers, not silicon area
-> cost-efficient detector length is quantised

Should we set up some external review of project at this stage?

Proposals for more realistic (pessimistic?) ILD ECAL simulation and digitisation

Daniel Jeans, October 2013
with input from many others, thanks!

Current Mokka models probably too optimistic from a technical point of view.

Try to agree among ourselves on realistic (pessimistic) scenarios

Ensure that simulations are at a **similar level of realism:**
fairer comparisons between technologies,
more confidence in their conclusions

I consider only the internal ECAL parameters, not the overall size.
(which is an important parameter, but not related to realism of simulation)

Consider Si and Sc technologies with **same total ECAL thickness**
to avoid biasing cost of outer detector parts

Starting point: ILD_o1_v05 and ILD_o3_v05

Internal ECAL parameters.

(all dims in mm)	Si / Sc thickness	Number of W layers, thickness	Equipped PCB thickness	Cell (strip) size	Guard ring (reflector) Thickness	Total thickness
Si-DBD	0.5	20x2.4 9x4.2	0.8	~5x5	0.5	185
Si-A	0.32	17x2.4 8x4.8	2.0	~5x5	0.5	198
Si-B	0.32	13x3.15 6x6.3	3.5	~5x45	0.5	203
Sc-DBD	2.0	20x2.4 9x4.2	0.8	~5x45	0.057	227
Sc	1.0	17x2.4 8x4.8	1.2	~5x45	0.1	195

Hybrid models should use same parameters, where appropriate, and generally aim for a thickness of 200 +- 5 mm

Digitizer effects to be included:

Si-ECAL:

- 0.5 MIP cut (will have to change with thinner silicon)

Sc-ECAL:

- non-uniformity, attenuation length 500mm
- Convert to # photo-electrons (7/MIP), poisson smear
- MPPC saturation, effective pixel number = 10000
- Cut at 0.5 MIP

Cross-checks: (small dedicated simulation studies)

- Effects of:
  - Realistic noise rate
  - Calibration/saturation uncertainty
  - Cross-talk in ASIC/pads/strips
  - Use measured strip non-uniformity