Si-W ECAL : 2014 goals

- **1.1 Test of HPK sensors (baby wafers, without GR…)**

  IV, CV = f(T, RH) + laser (square event) + radiation

- **1.2 Test of FEV9 : clock lines**

  Assembly of a fake long slab (w/o chips)

- **1.3 Test of FEV9 & chips**

  Tests of simgle chips before soldering, soldering, test of whole board

  => need software ! (configuration management, automatic scans, …)

- **1.4 Integration tooling & missing parts (coper sheet, HV kapton) & procedures for short SLABs « U »**

- **1.5 Production of ~8 SLABs**

- **1.6 Study of long slabs + production of 1 or 2 long SLABs**

  Only instrumented at both ends (cost)

Si-W ECAL what is missing ?

- Software developement
- Manpower for PCB design : adapter board, fake FEV9 (extender for long slab), …
- New assembly tooling (improved reliability)
- Manpower for testing
  - Hundreds of chips to test stand alone
  - Boards
  - Slabs
  - Detector
- Manpower for test benches
  - Build up
  - Maintenance
- Mecanics for integration into the C-W structure (cable&DIF holders, slab alignment, ….)
- Project tools (repository, EDMS, …)
  - On going

Si-W ECAL what should be looked at ?

- HV distribution & control
  - eg. HPK miniature HV generator
- LV distribution & control
  - eg. TDK miniature regulators and DC-DC converters
- SKIROC2x, SKIROC3, OTHER (kpix, QIE)?
- DCS : temprature, …
- Interated DAQ (at least DIF & top of module boards)
  - On going
- Software
  - Data base, configuration & connectivity data base
  - Scalable SW
  - Embedded SW ? (automated procedures in local boards ? Vectorisation of data, …)
- Serigraphy (deposit of glue for wafers)
- Automation in general : toward industrialization
- Ageing, robustness tests

Discussion

- DAQ
- Next sensor design
- Sharing of harware (existing or not)
- Sharing of technical tasks
- Results of sensors measurements
- …

DAQ

- Was acceptable for test beams (LDA)
- Most (85%) of problems are due to connectors & power-on issues or improper use of the system
- Good progress on sept./oct. with GDCC : bugs expunged (until new ones are found)
  - Very few packet loss
  - Current setup OK : several (6?) slabs configured easily (once connectors & power-on correct) => Franck's job of the week (2 faulty kapton, 1 hdmi suspected)
- Could make the system available for collaboration

- ISSUE1: not have a lot of part in hands (only 3 GDCCs) : need additional production (& time for testing!)
- ISSUE 2: adapter board not designed yet (use old ones but limits FEV9)
- ISSUE 3: ageing of solder on DIF : 70% need to be reworked (diagnostic from external company)
- ISSUE 4: time for "hotline" & maintenance, travels on site (Japan)
- ISSUE 5: DIF FW needs some adaptation for SPIROC (add functionalities)

FEV9

- Received!
- Has holes for laser & bonding of GR
- 2 partitions of 8 chips, can be reduced to 4 chips or 1 chip
- NOT fully compatible with adapter board used for FEV8
- Wafer footprint for 2010 design (before laser dicing)