AHCAL electronics.

Status Module Production an Power Pulsing

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AHCAL main meeting
DESY, Dec. 10th, 2013

HELMHOLTZ
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U·H
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CALICE
Calorimeter for ILC

AIDA

DESY

Outline

> Introduction

> Hardware Status

- AHCAL
- SM_HBU
- ScECAL

> Power Pulsing

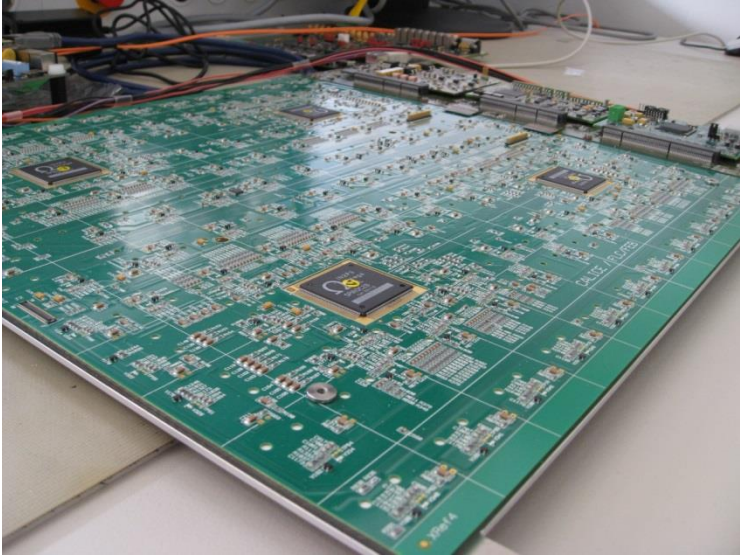> Conclusion
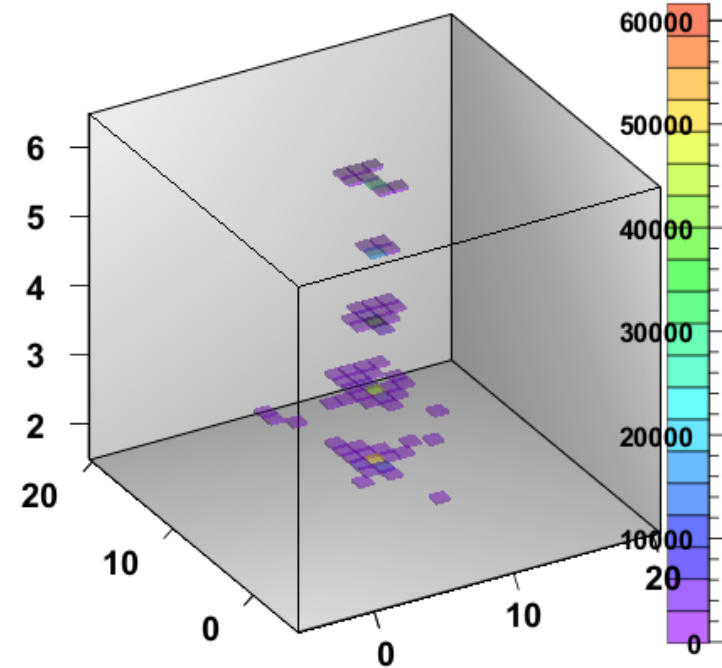
*Shower in 5 AHCAL layers
(DESY testbeam)*

Hardware Status

> HBU2: (two production runs): 14 boards. (tiles?)

- Next HBU order requires redesign: New LED type!

> CIB, POWER and CALIB: 20 boards.

> Flexleads (2 types, a lot in use): 14 boards (each type)

> EBU vertical: 4 boards

> EBU horizontal: 4 boards **(new: completed)**

> SM_HBU: 2 boards

> Delivered complete sets (HBU2/EBU/SM_HBU + DAQ modules) to: Uni-HH, Shinshu, Mainz, NIU. One further HBU2 to Wuppertal.
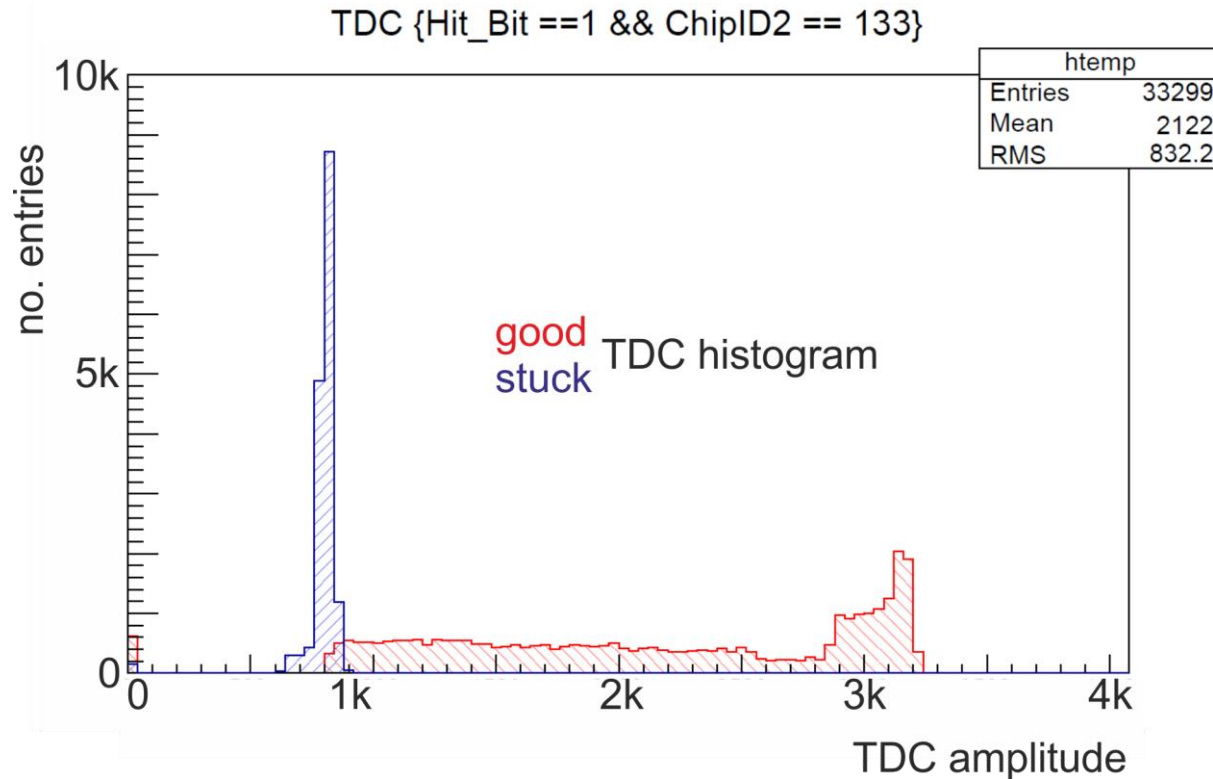
New 8 HBU2 boards

> All 8 new HBU2s have been tested and work fine.

> Problem: Significant spread of board dimensions within the 8 boards. Landmarks differ up to 0.4mm (0.1mm was specified).

> Problems during PCB assembly and with the steel cassettes (individual cassettes needed).

> From the discussion with PCB manufacturer: For the next order, there will be a pre-compensation process step for the inner pcb layers before the pressing operation. **This will solve the problem as it did for the first 6 HBUs**.

> **5 of the new HBU2s delivered to Uni HH.**

HBU redesign (HBU3)

> Adjust LED holes (new LEDs), balance LED positions for Uni-HH tiles

> Equalize LED drivers line lengths (TDC calibration by LEDs)

> Test: terminate SiPMs to VDDA (power pulsing). Jumper!

> Additional GND and VDDA pads next to flexfoil connectors to reduce voltage drop across slab.

> HBU Redesign till mid Feb. 2014.

  ▪ Confirmation about new LEDs and drivers (Wuppertal)

  ▪ Test of SiPM termination for power-pulsing (DESY).

Detector Power-Up Problem

TDC {Hit_Bit ==1 && ChipID2 == 133}

htemp	
Entries	33299
Mean	2122
RMS	832.2

good TDC histogram
stuck

no. entries vs TDC amplitude

> Arbitrary operating conditions in multilayer setup (very seldom in single-layer setup): Stuck TDC, spontaneous noisy channels, shifted MIP position.

> SPIROC reset does not help, only re-powering helped.

Solution for Power-Up Problem
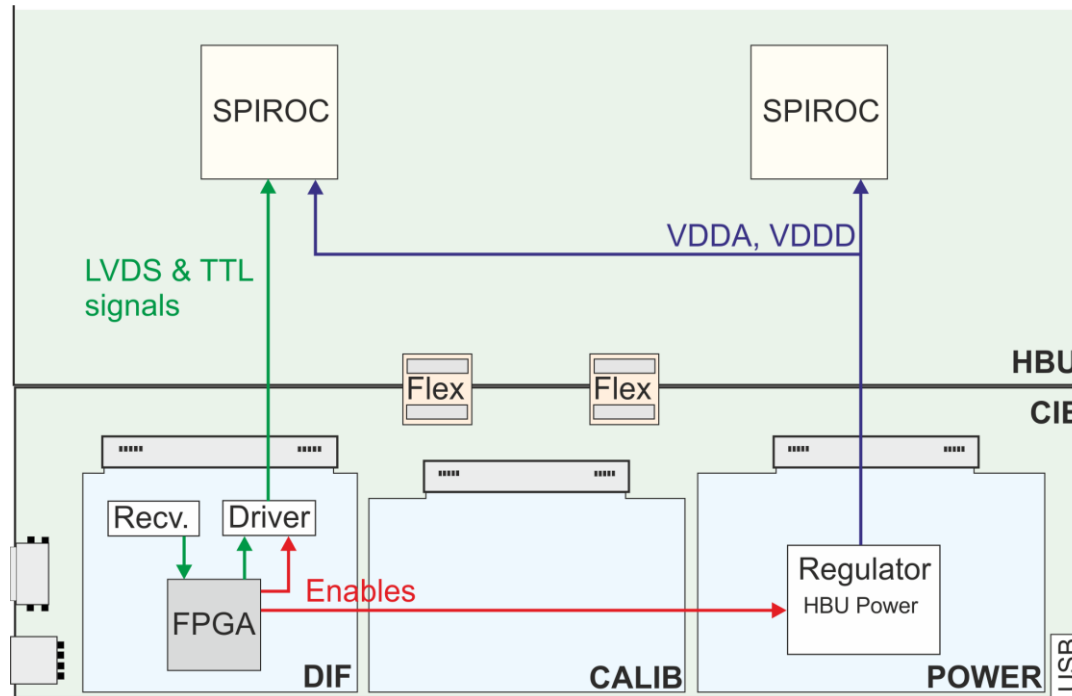
> Problem identified: After power-up and booting, the DIF FPGA sets TTL lines to SPIROCs before enabling SPIROC's power. => SPIROCs get power through protection diodes of input channels.

> New switch-on order cured the problem. Minor modification on POWER3 board needed.

Broken SPIROCs in testbeam

> During testbeam 6 out of 20 SPIROCs on three HBU2s have been damaged.

> Damage is the same for all chips: oscillating input DACs.

> SiPM pins have damaged the isolating foil and touched the steel cassette's top plate. => **Stronger foil seems to cure the problem!**

inDAC oscillation

top plate

Pins must be cut carefully
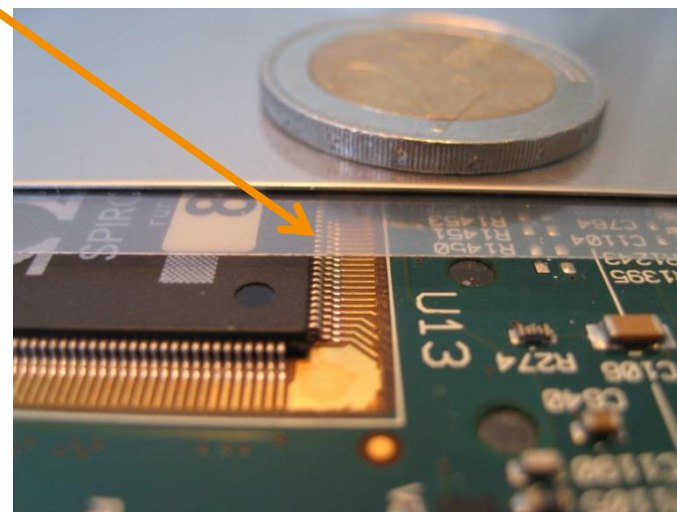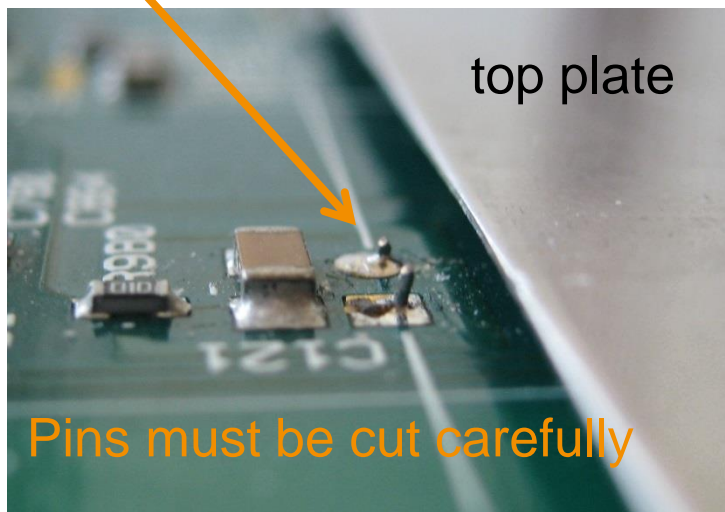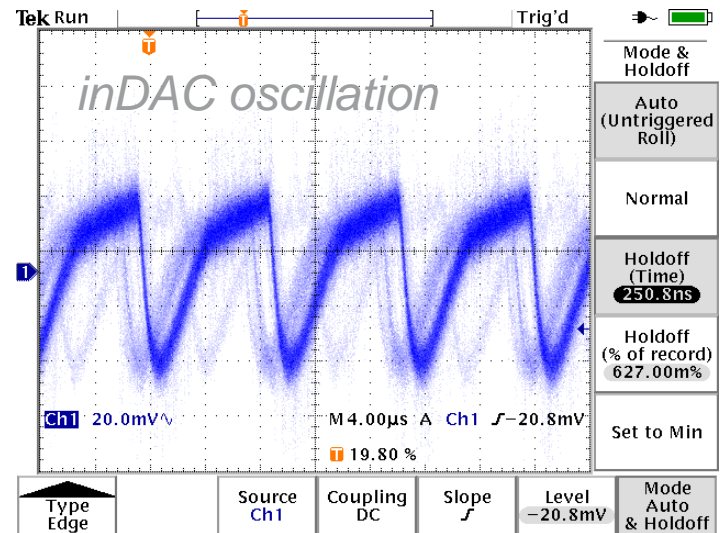
Northern Illinois University

Integrated Readout Layer

- Uses HBU2 FE
- Hamamatsu MPPC mounted on small flex circuits
- Scintillator "Megatile" with 3 x 3 cm cells optically isolated with white epoxy
- Cells have a concave dimple improve the uniformity of the response and to direct light through hole in board onto MPPC
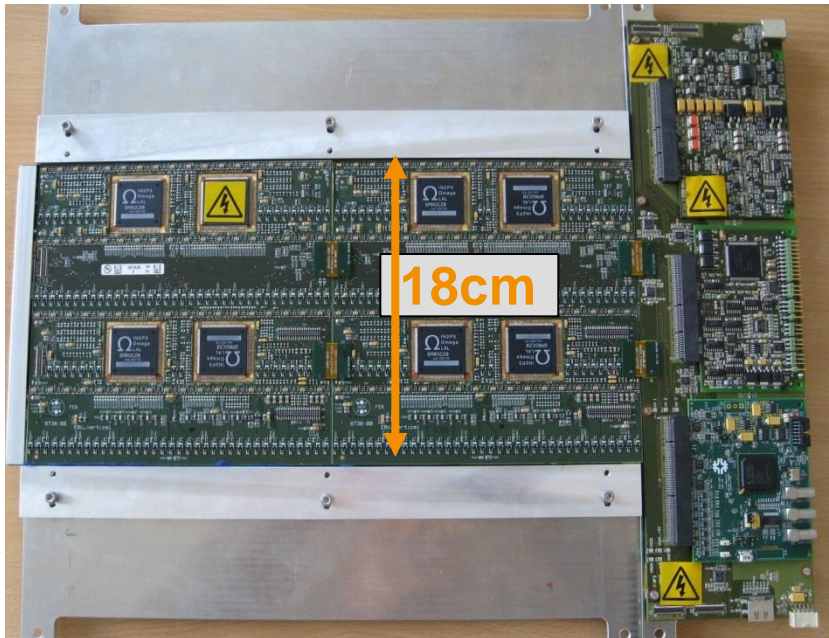**- Easier to assemble, does not need WLS optical fiber**
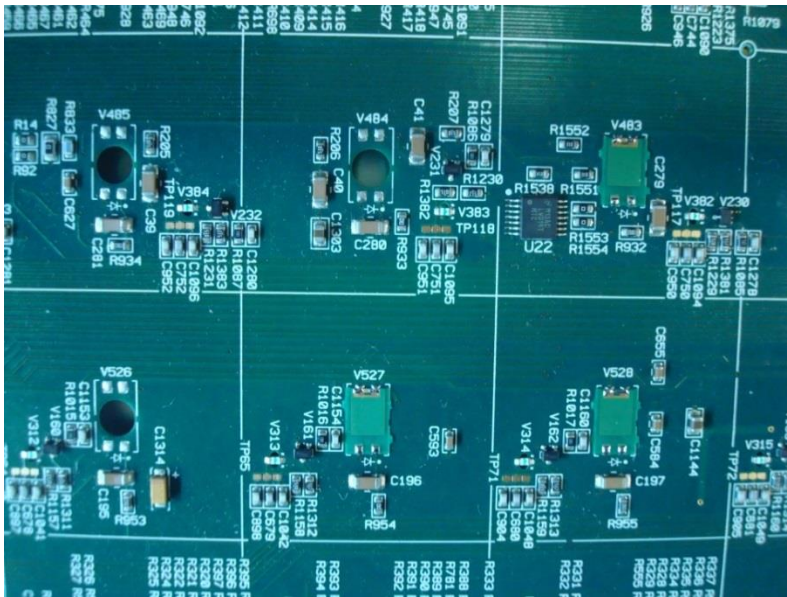
Results by Kurt Francis

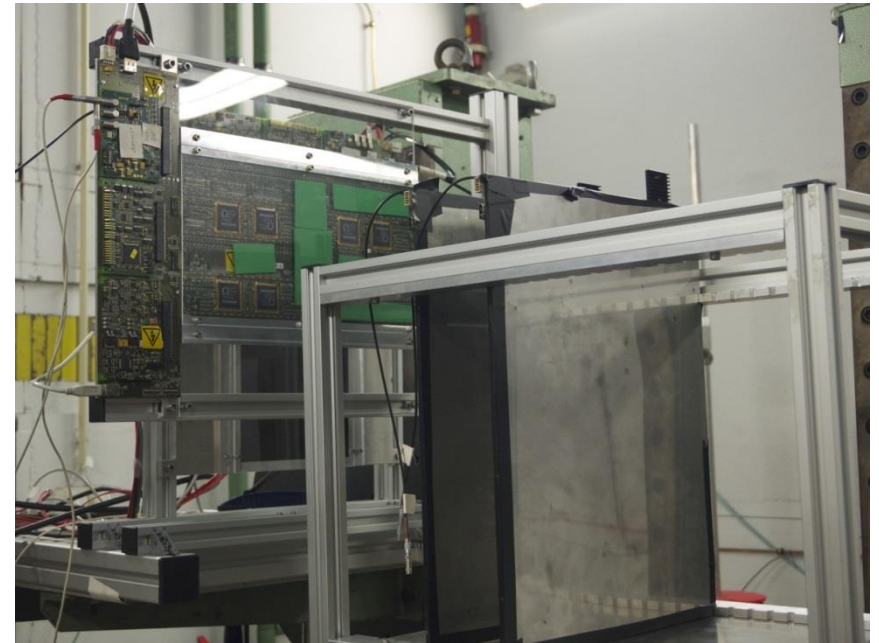First big commissioning steps accomplished. Great progress…!!
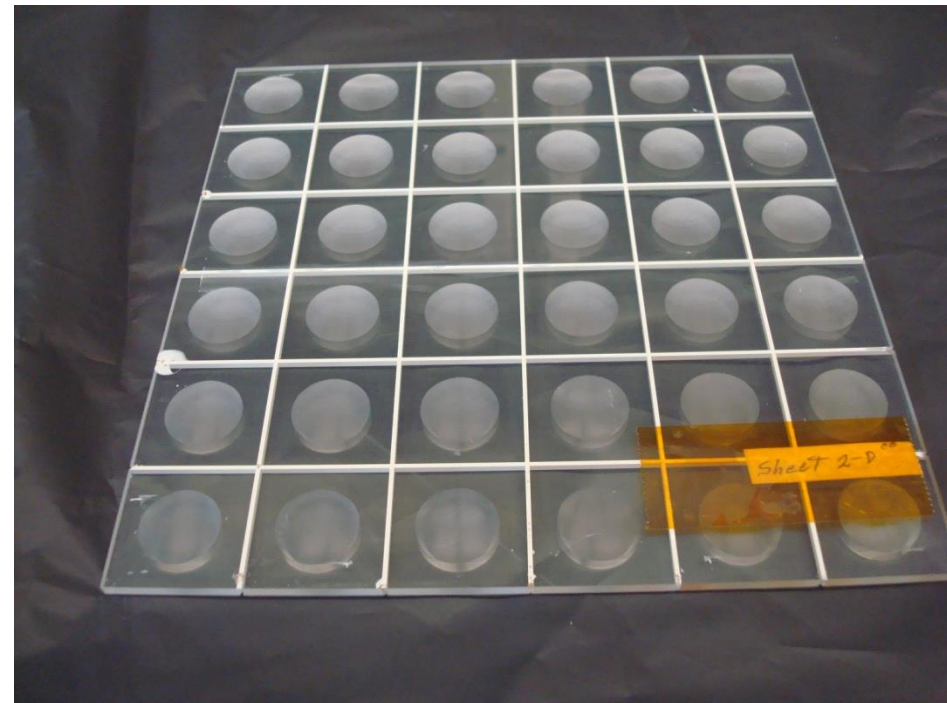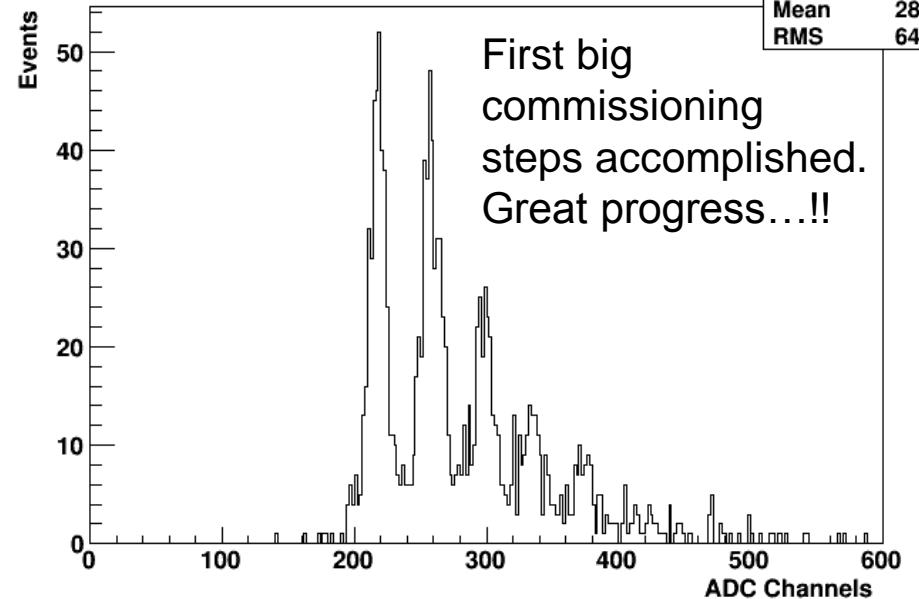
Scintillator ECAL – EBU vertical

> 4 EBU_vertical produced and tested at DESY testbeam.

> ScECAL uses the same DAQ as AHCAL => easy synchronization in testbeam.

18cm

2 Scintillator ECAL modules with HCAL DAQ interface modules.

2 ScECAL and 2 HCAL layers in DESY testbeam, operated synchronously by the HCAL DAQ.

Scintillator ECAL – EBU horizontal

> 4 EBU_horizontal produced.

> Horizontal scintillator orientation.

> Long flexleads needed at output, expected in Jan. 2014

> Survived Smoke-Test and worked (without bias/tiles) right out of the box ☺.
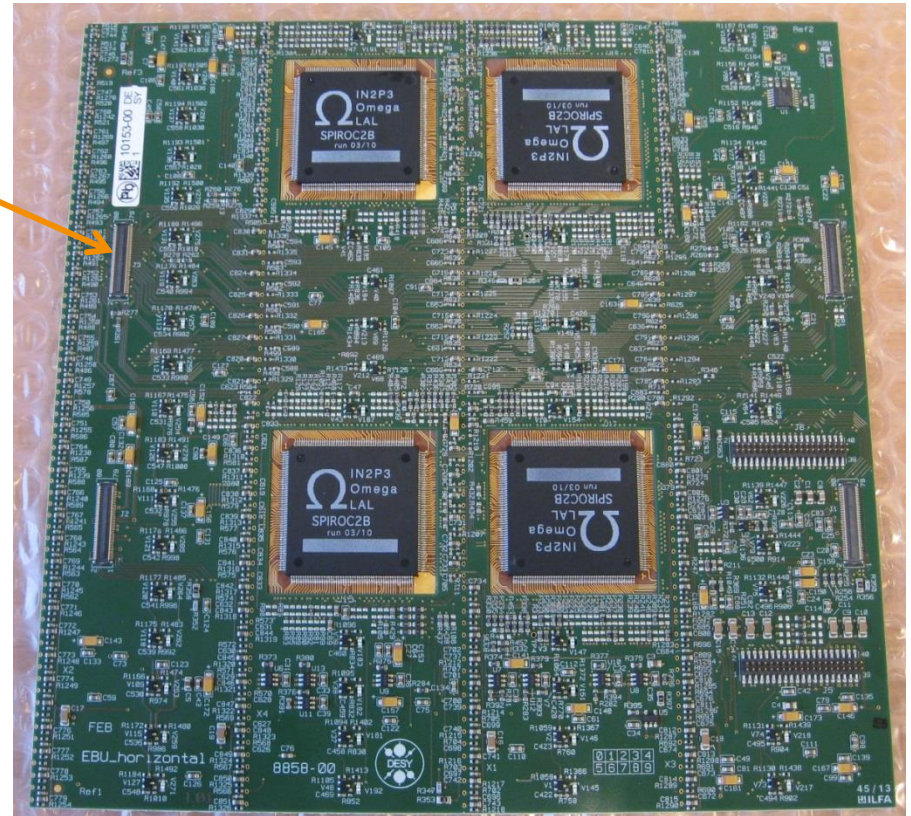
Full extension: Test of 6 HBU2s in a Row

> 6 HBU2s with 864 detector channels in lab (Sept. 2013).

> Questions: Transport of 40MHz LVDS clocks, power, LED trigger over 216cm possible without limitations of detector performance?

> First results for smallest signals (single-pixel spectra of SiPMs) prove the suitability of the setup:
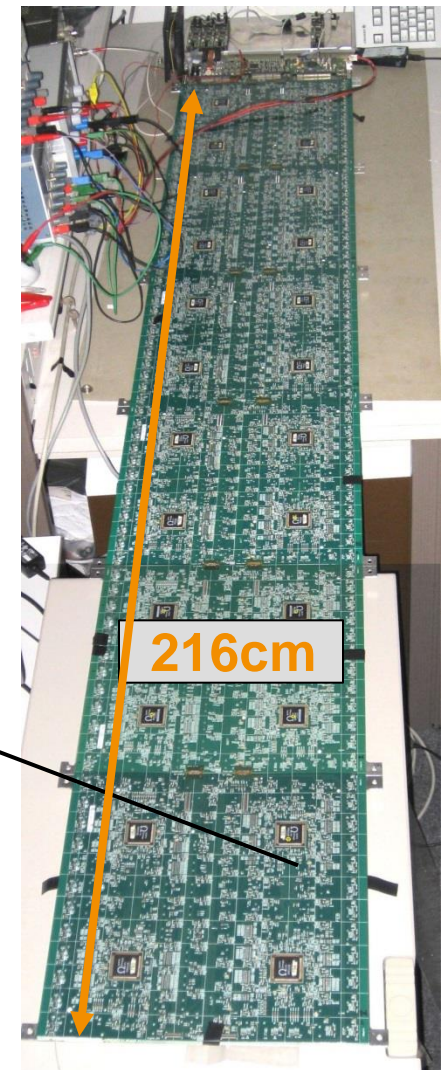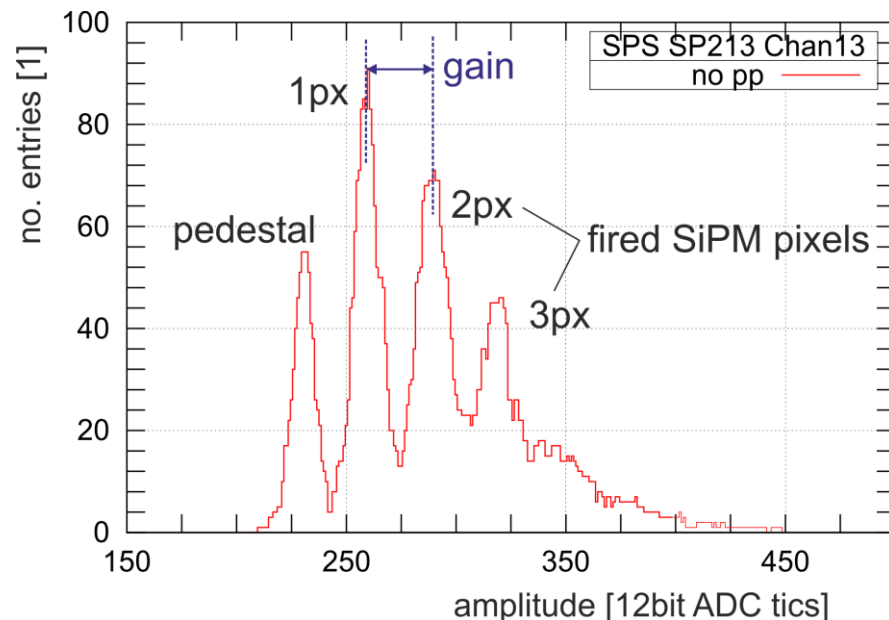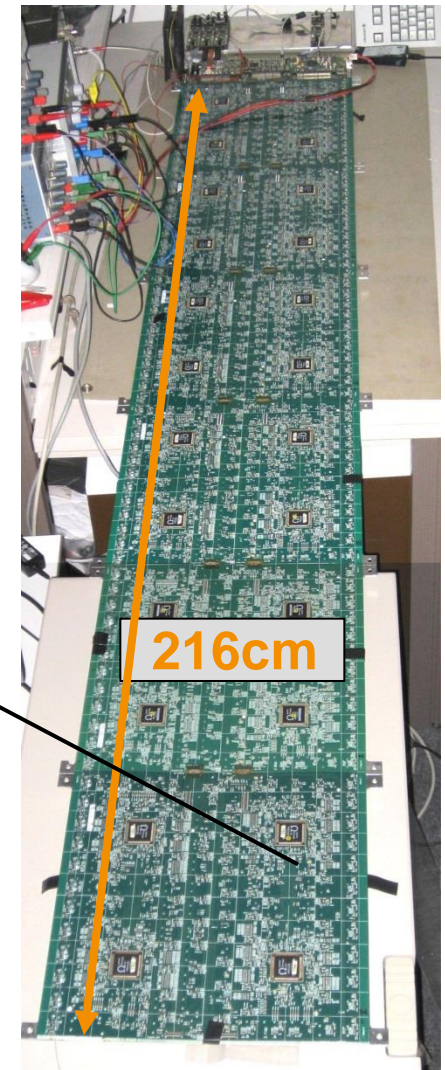
Full extension: Power Pulsing

> Switched Current: 2.75A (analog supply voltage VDDA).

> Voltage drop across 216cm (dominated by flexleads):

  - 0.18V on VDDA (19mΩ per HBU2+flexlead)

  - 0.04V on GND (4mΩ per HBU2+flexlead)

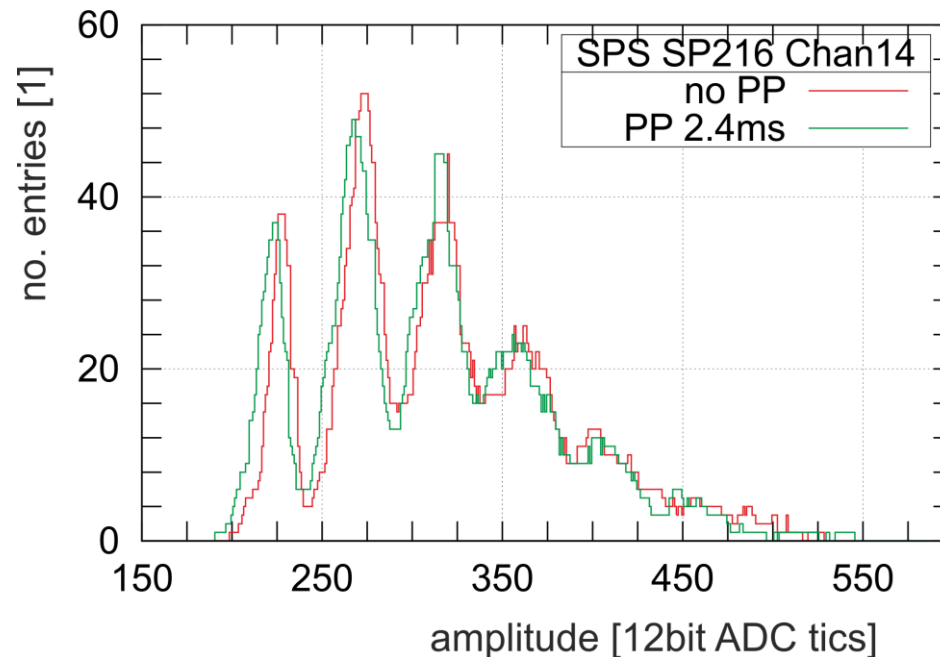> Studies ongoing, e.g. additional block capacitors:
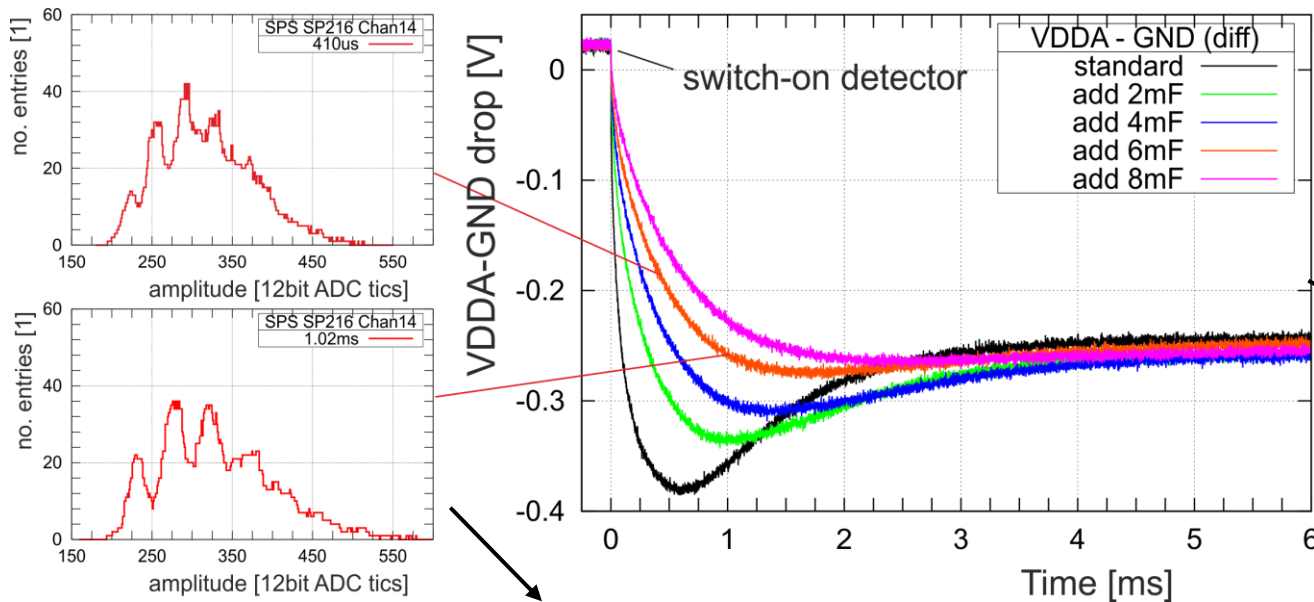
> Switch-on time T_on too small: Low gain and high noise!

Full Extension: Power Pulsing

> With 6mF: ~2ms switch-on time needed (~2% on-time). Excellent agreement w/wo power pulsing (only small pedestal shift).

> Power Pulsing works for the full extension setup!

> Trade-off between switch-on time and blocking capacitors needed.

> Studies ongoing – several ideas in discussion with LAL.

Conclusion – Next steps towards testbeam

> Power Supplies: MPOD System from Wiener: LV modules have arrived, HV modules are ~2months late and we do not get a clear date of the delivery.

> Temperature Readout of AHCAL needs improvement – task is delayed due to illness of the microcontroller developer. Next steps end Jan. 2014.

Backup Slides

Towards the next SPIROC

Topics to keep in mind …

> Pedestal shift when too many channels have a high signal.

> Memory cell dependent amplitude decay. Solved by compensation caps.

> Slow-Control configuration is problematic for long slabs.

> Feedback of channel-wise trigger thresholds on the global threshold.

> Random zero events and zero-results for the first trigger.

> Poor uniformity of the input DACs.

> Holdscan is different for HG/LG.

> Trigger threshold width increases with threshold height.

> Amplitude-to-threshold relation depends on preamp. setting and pulse shape.

> TDC: Amplitude dependent time-shifts and channel-to-channel spread.

> TDC: Result depends on which ramp is used and the memory cell.

> TDC: big chip-to-chip spread of ramp slopes.

Trigger Validation (Testbeam mode)
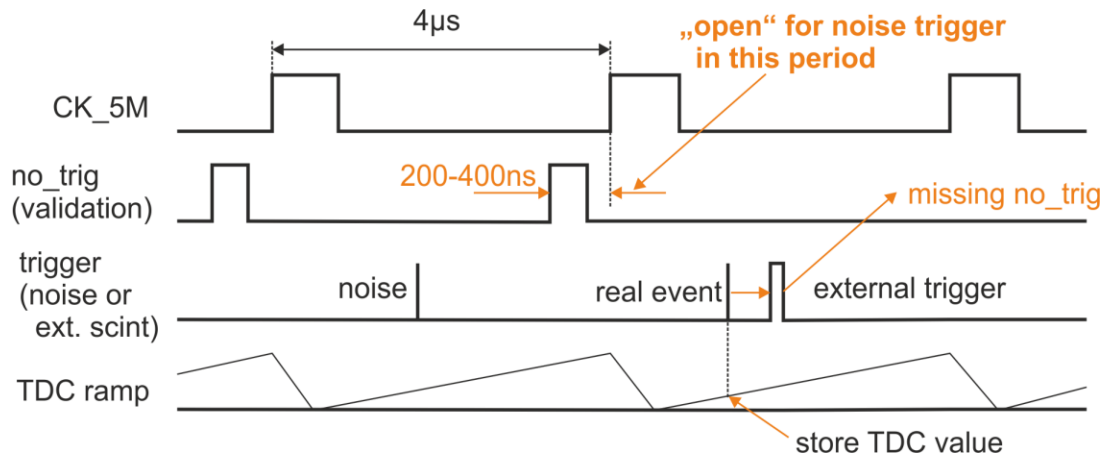
> Only stores events that are validated by an external trigger signal

> **Validation works fine**: Histogram only shows MIP events without noise/pedestal contributions.

> Problem: Validation does not work for noise hits between no_trig and rising CK_5M edge (200-400ns). **Triggers in this period should be rejected (=> dead time).**

> Now: Factor 10 noise reduction. Improve 400ns window size.
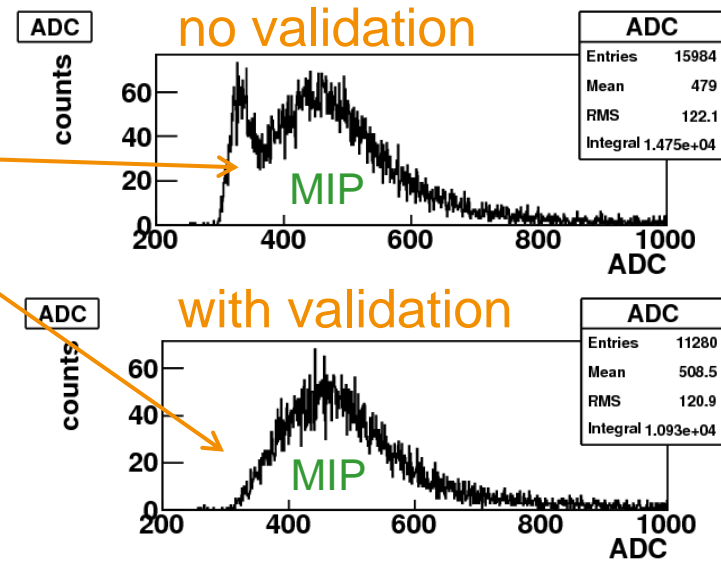
# Power and Power Pulsing (PP)

> Aim: Switch on as short as possible before data taking starts (initial idea: 20µs).

> Results with charge injection show a decreased amplitude response with PP.

> Single-Pixel Spectra measurements show a reduced amplitude with PP.

> Aimed power dissipation of 20µW per channel not reached yet.
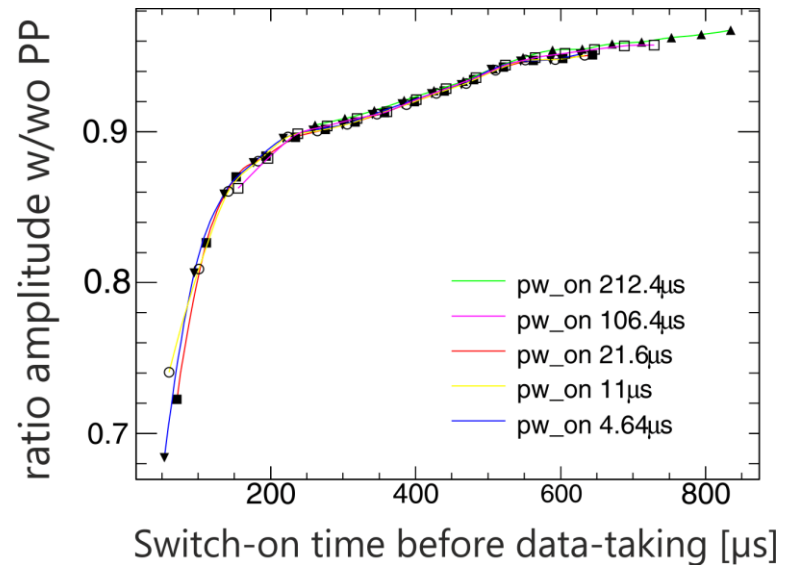
TDC Calibration – CERN Module

> Calibration of all 16 SPIROC2b ASICs of the CERN Testbeam-module with charge injection.

> Chip-to_chip spread of the TDC ramp slopes: Calibration necessary: TDC (time measurement!).
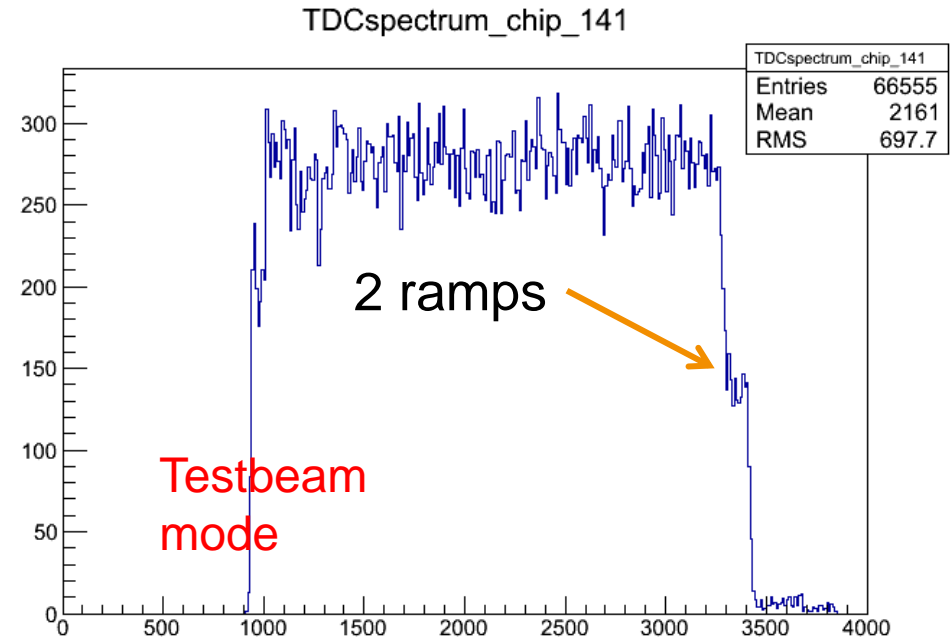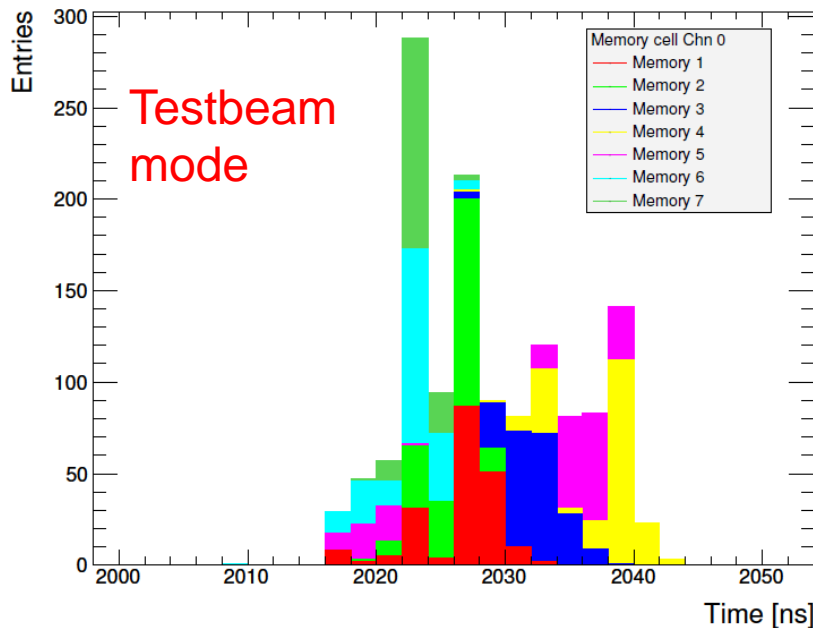

SPIROC2b chip-to-chip spread of the TDC ramp Slopes.
~1.6ns/TDC bin
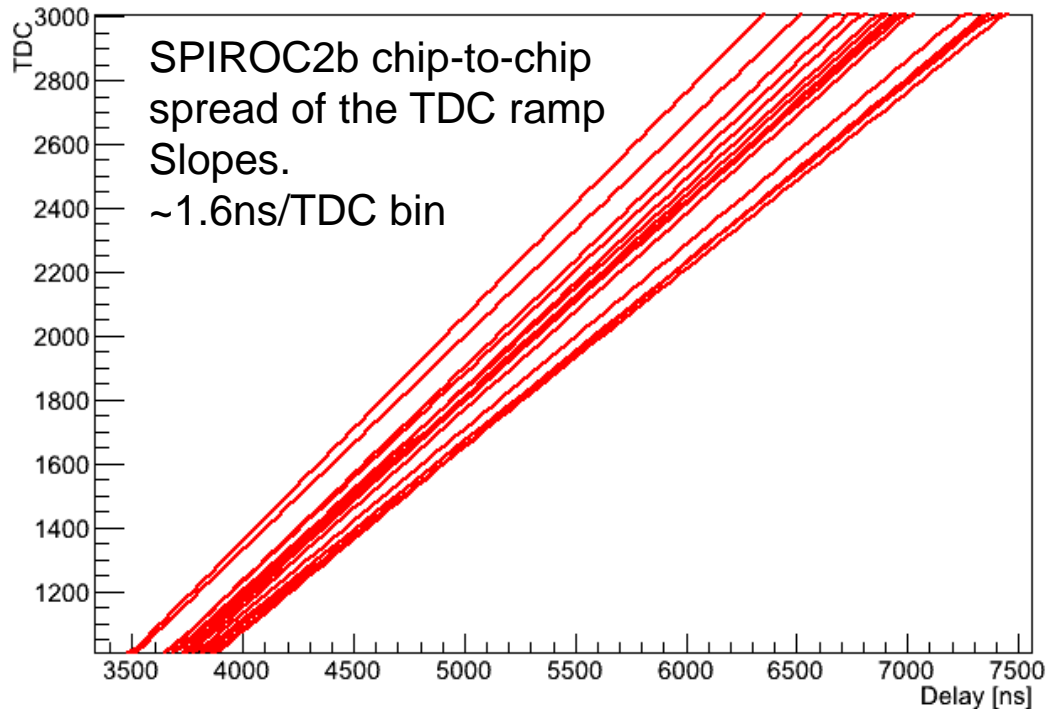
TDC: Time Walk and Channel-to-Channel Spread
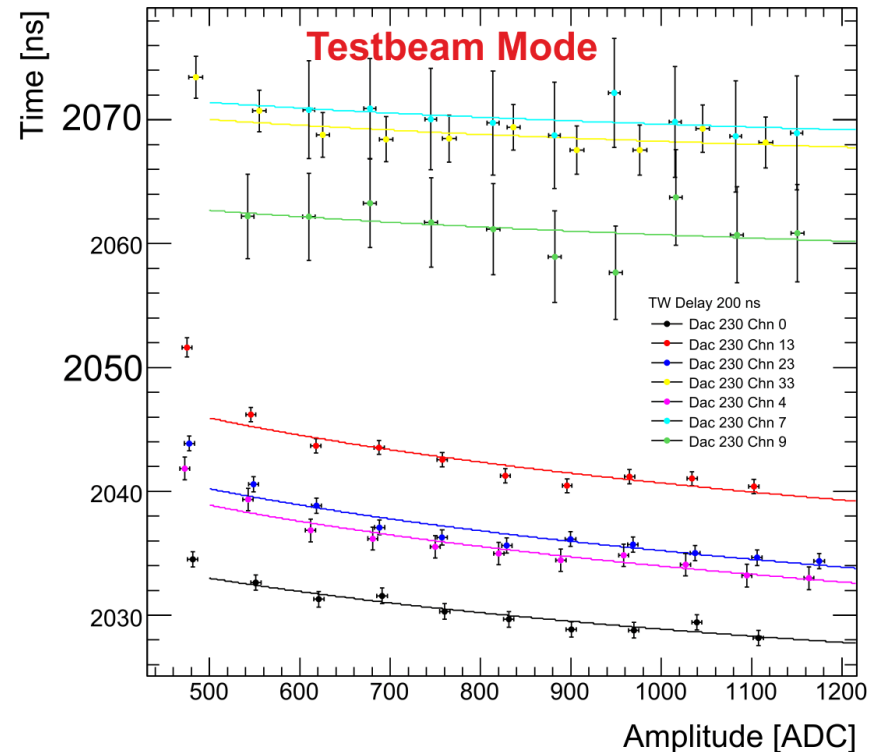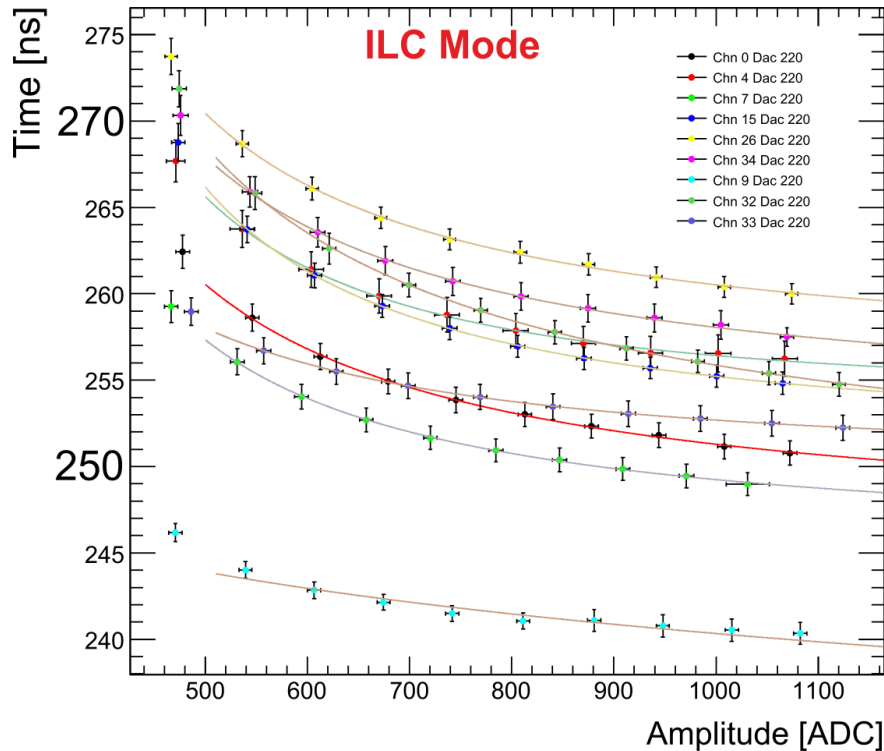
> Amplitude-dependent time-shifts and channel-to-channel differences.

> Difficult to parameterize because of different behaviours. Channel-wise TDC calibration necessary as for ADC (MIP calibration)?
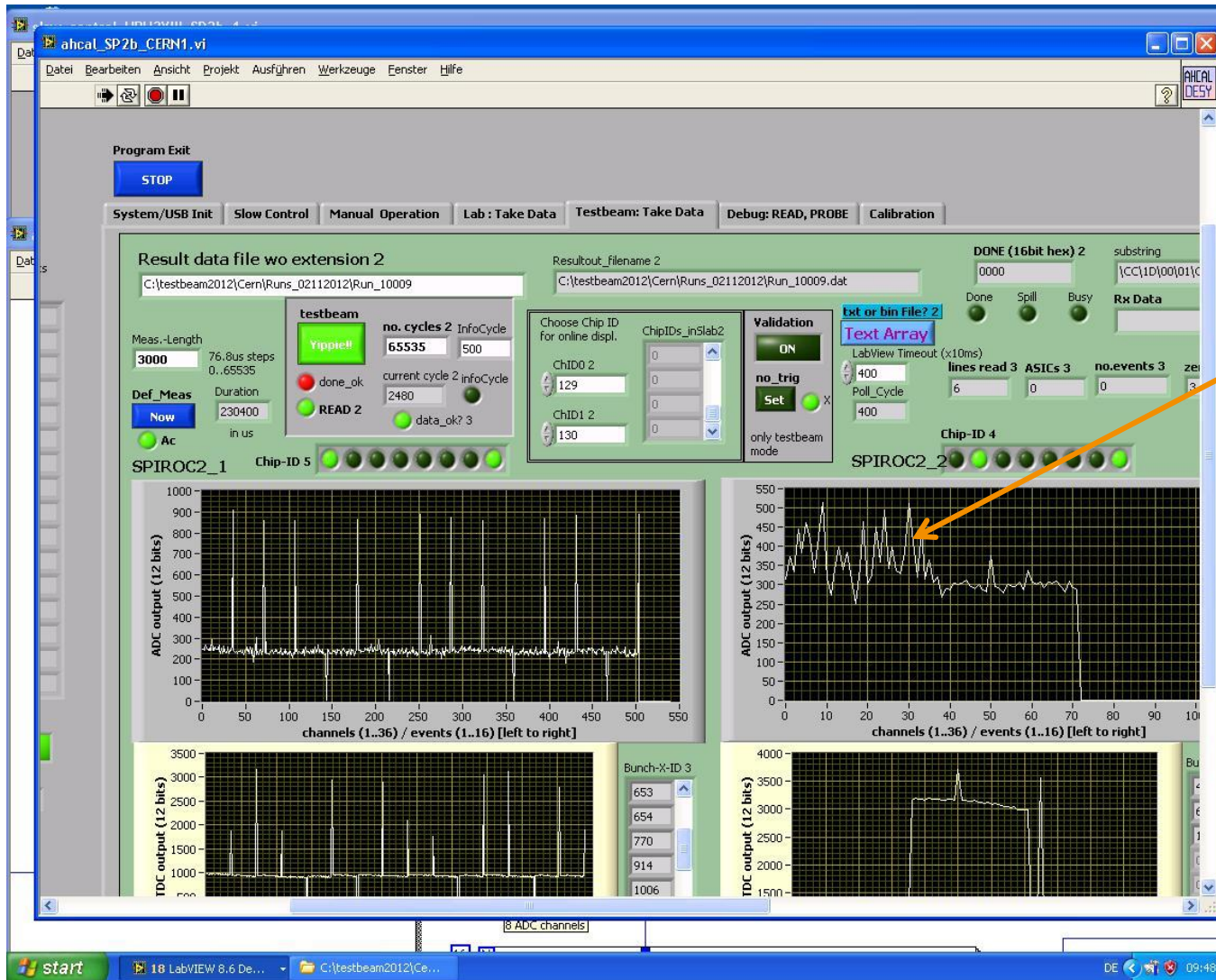
> TDC result depends on memory cell

> The SPIROC2b internal TDC ramps have different amplitudes and for a specific event it cannot be identified with which ramp the TDC result has been achieved (known problems).
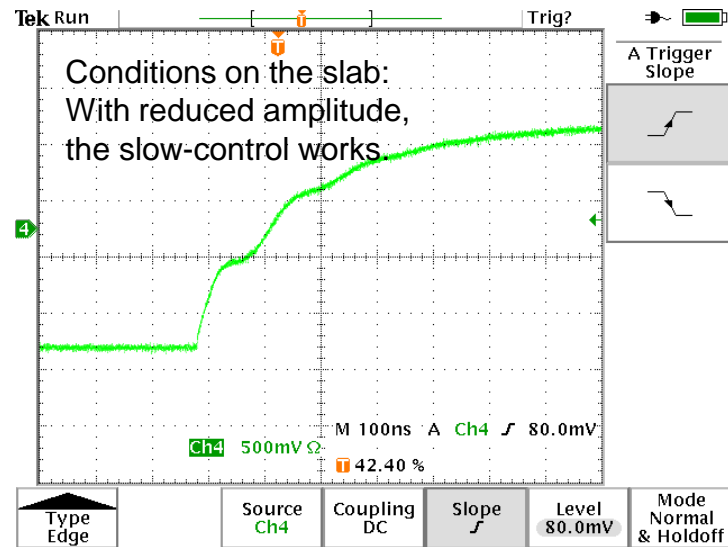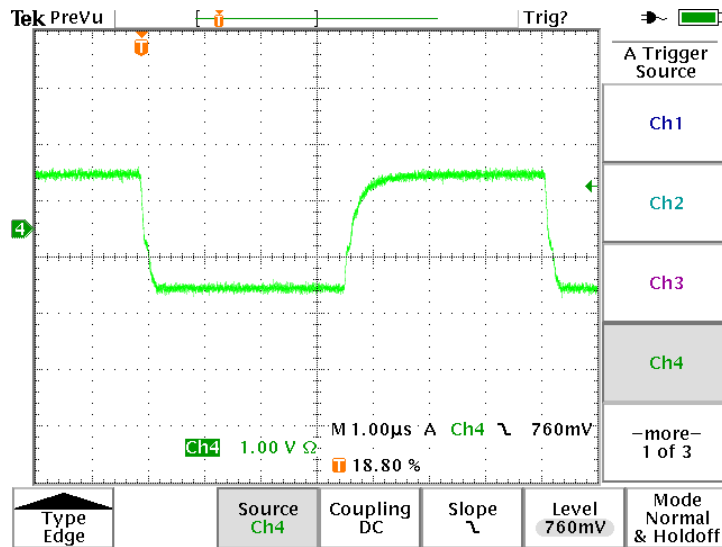
Start-Run Problem

CERN testbeam

High noise on pedestal for first 1-2 readout cycles

Slow-Control Problem

> For longer AHCAL slabs, the slow-control programming is instable. Reason: Slow-control clock, special pulse-shape needed (series R, termination R, block-C)

> Although the slow-clock looks fine, the configuration does not work.

> Analysis ongoing, I2C in SPIROC3.