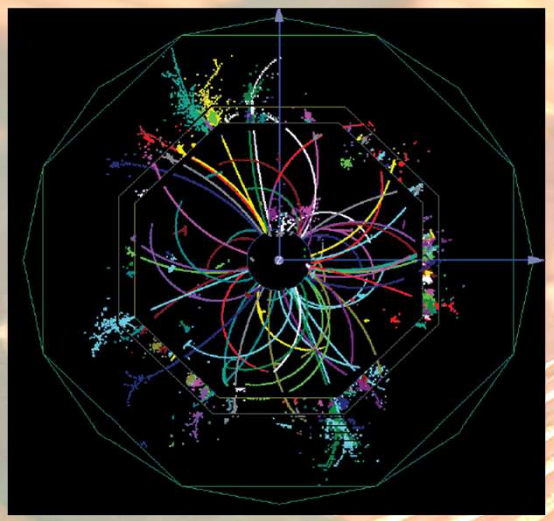
Plans for SKIROC and SPIROC



Mardi 9 décembre 2013

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Organization for Micro-Electronics desiGn and Applications

Our plans for the ROCs chips

Engineering run in *AMS 0.35 µm SiGe* expected before the end of 2014

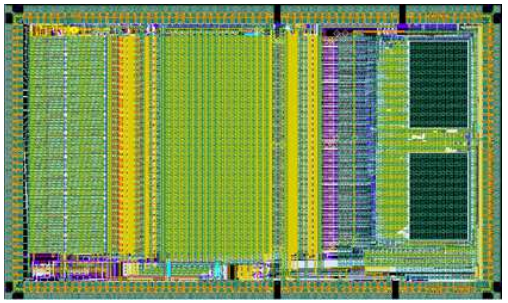
- Several chips will be produced. We will take the opportunity to submit a new version of **SKIROC 2b** and **SPIROC 2d**

These chips will be an intermediate step before switching to 3rd generation chips

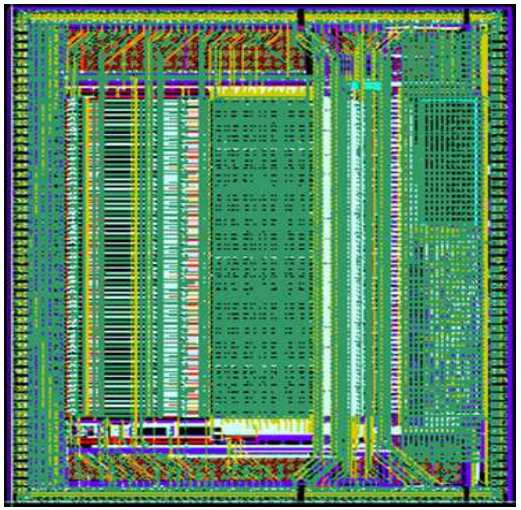
3rd generation ROC chips:

- The **64 (HR and SK) or 36 (SP) channels** will be **independent for zero supress**, meaning that only the hit channels will be memorized in the SCA
- **I2C link** for the slow control parameters
- ….

HARDROC 3 was submitted in Feb 2013 (funded by Aida). (see Nathalie's talk). **Feedback tests** are necessary before submitting any other third generation chip.



SPIROC 2
Analog HCAL
(SiPM)
36 ch. 32mm²



SKIROC 2
E CAL
(SIW)
64 ch. 70mm²

On road to SPIROC 2d and SKIROC 2c

SKIROC2 and **SPIROC2** are very similar chips except for the very front-end stages.The SCA and the digital part are the same…

Many laboratory measurements and testbeam have been done on SKIROC 2 and SPIROC 2.

The feedback of the different users (HBU, EBU, and FEV) is crucial for us.

Towards the next SPIROC

Topics to keep in mind …

- Pedestal shift @ huge signals, pedestal different for internal/external trigger.
- Memory cell dependent amplitude decay. Solved by compensation caps.
- Slow-Control configuration is problematic for long slabs.
- Feedback of channel-wise trigger thresholds on the global threshold.
- Random zero events and zero-results for the first trigger.
- Poor uniformity of the input DACs.
- Holdscan is different for HG/LG.
- Trigger threshold width increases with threshold height.
- Amplitude-to-threshold relation depends on preamp. setting and pulse shape.
- TDC: Amplitude dependent time-shifts and channel-to-channel spread.
- TDC: Result depends on which ramp is used and the memory cell.
- TDC: big chip-to-chip spread of ramp slopes.

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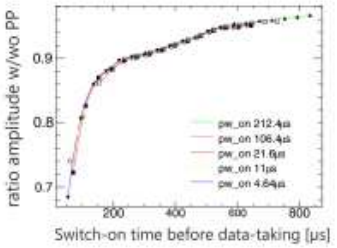
Power and Power Pulsing (PP)

- Aim: Switch on as short as possible before data taking starts (initial idea: 20µs).
- Results with charge injection show a decreased amplitude response with PP.
- Single-Pixel Spectra measurements show a reduced amplitude with PP.
- Aimed power dissipation of 20µW per channel not reached yet.



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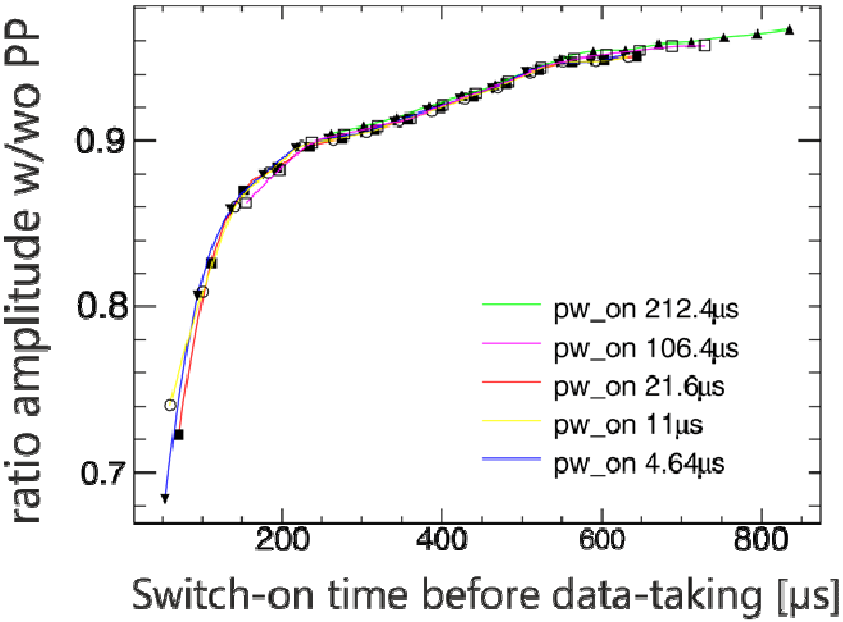
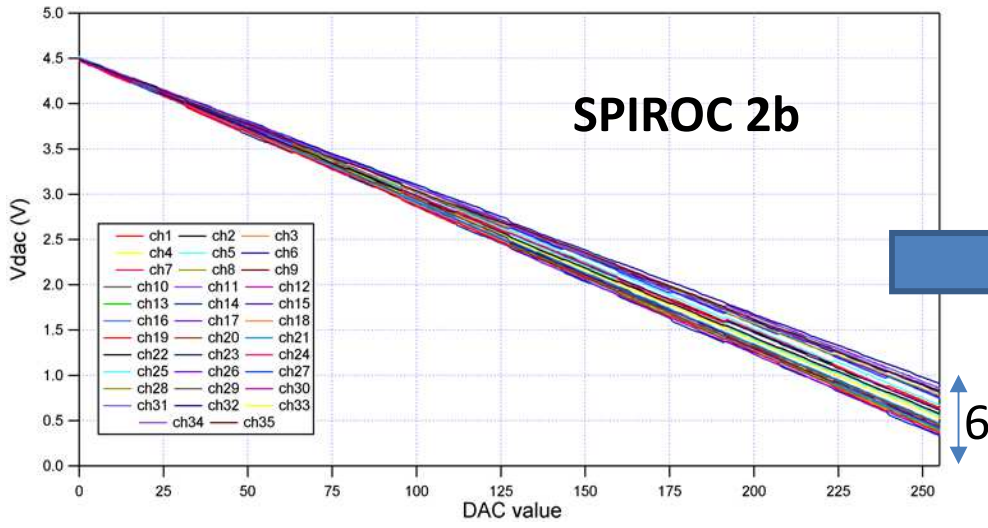
SPIROC 2d and SKIROC 2b improvements

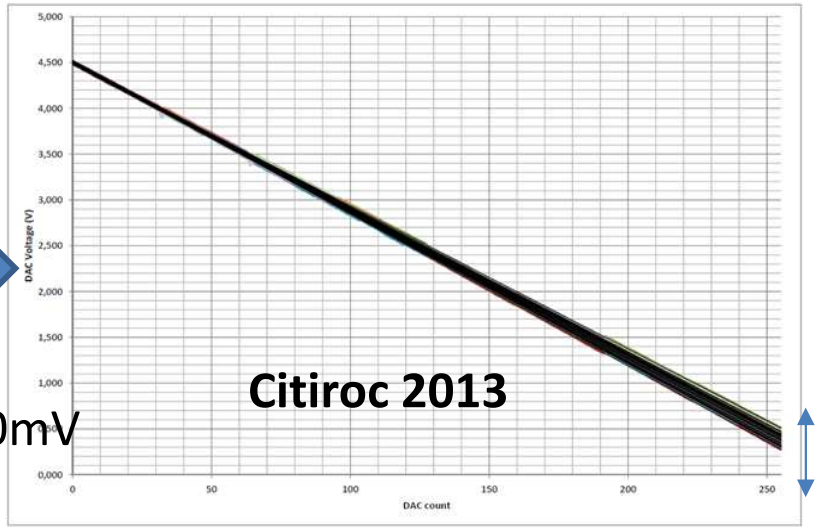
- Many issues already understood and solved in SPIROC 2c will be in SPIROC 2d/SKIROC 2b
  - Pedestal shift @ huge signals, pedestal different for internal/external trigger.
    - Due to long distance cross-talk
  - Memory cell dependent amplitude decay (“rate effect”).
    - Due to switches on compensation capacitances
  - Influence of channel-wise trigger thresholds on the global threshold.
    - Due to internal parasitic resistances
  - Random zero events and zero-results for the first trigger.
    - Due to ADC management signals sequence
  - Holdscan is different for HG and LG
    - Due to cross-talk between HG and LG

SPIROC 2d and SKIROC 2b improvements

- Power pulsing issue: far from the expected 20us
  - A system must be implemented to help the preamp to recover in less than 20us the ability to take data
- Input DACs uniformity:
  - performance noticeably improved but not yef satisfying (difficult due to the small power budget)

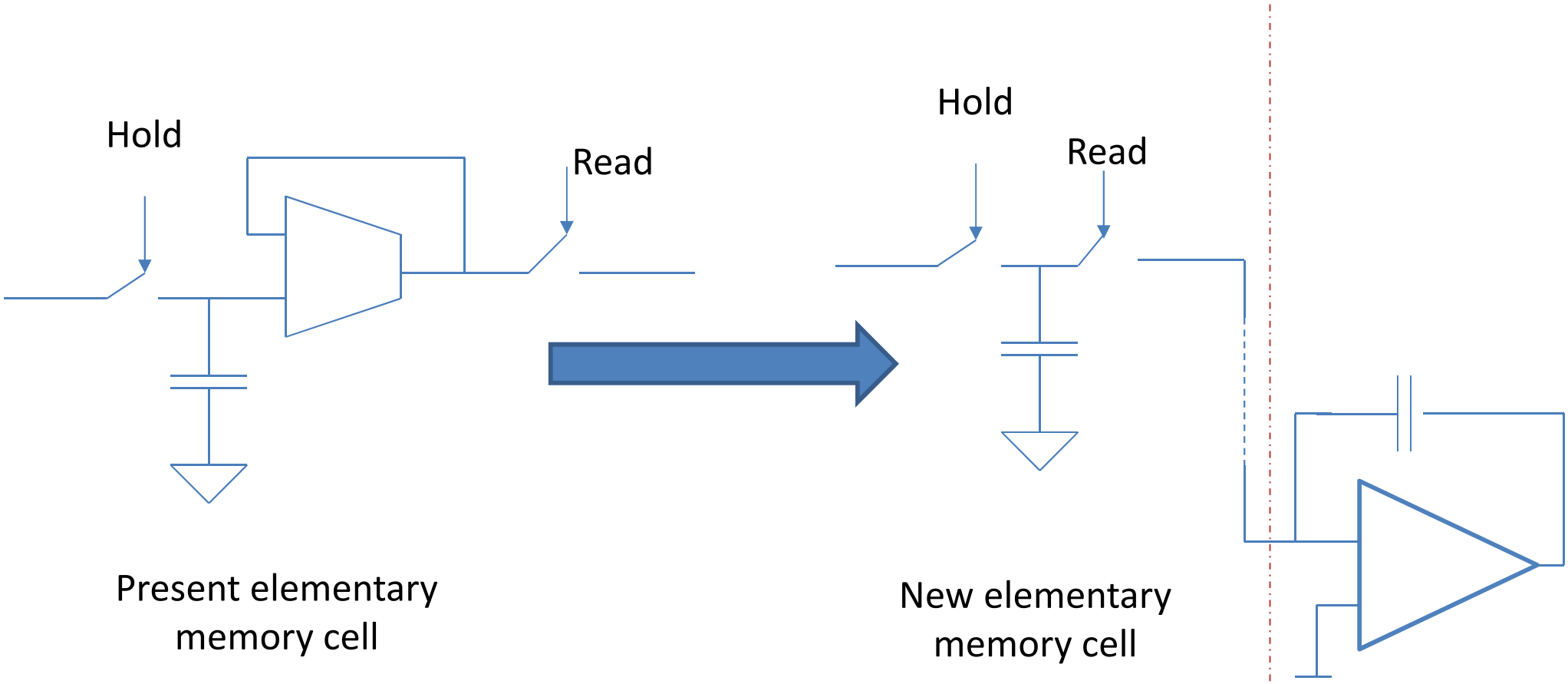






SPIROC 2d and SKIROC 2b improvements

- The present analog memory system introduces an offset on each elementary cell : could be improved but droop to be checked

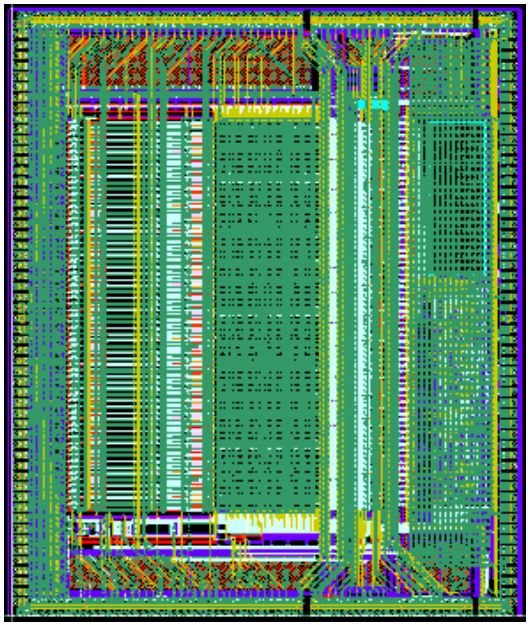


SPIROC 2d and SKIROC 2b improvements

- Preamp choice : need to decrease sensitivity to vdda
  - At system level, on HBU, EBU and FEV
  - Preamp input stage
  - On chip power filtering
- Substrate coupling issue
- Power sequencing issue (« power up problem »)
- Reliability improvement (in particular the input DAC)
- TDC to be redone (as in petiroc)

Development with XFAB 180nm

- **Exploration of a new technology for future**
- **Advantages of the XFAB 0.18 µm SOI HV technology :**
  - SOI -> less coupling via substrate
  - Sustainable because used by the car industry
  - Masks cost lower thanks to multi-mask process
  - Dimensions theorically reduced by a factor of 4 compared 0.35 µm. In practice : factor 2-3 expected)
- **Drawbacks: we've never used this technology**
  - Building blocks are necessary to be submitted before to check the technology. A PhD. student of LLR has started to work on it with our group.



SKIROC2 : 70 mm²
=> 70 k€ AMS 0.35µm SiGe MPW run (proto)

Summary

- Many laboratory measurements and testbeam have been done on SKIROC 2 and SPIROC 2. These mesurements allow to understand all the chip features.
- The feedback from the different users (HBU, EBU, and FEV) is crucial for us.
- Submission of a SKIROC 2b and a SPIROC 2d during our engineering run (expected before the end of 2014) => intermediate step before switching to 3rd generation chip.
- In parallel, plans to submit building blocks in XFAB 0.18 µm SOI HV technology for second source.
- HARDROC 3 test feedback necessary before submitting SPIROC 3/SKIROC 3