HR3: First measurements

OMEGA, 22/11/2013

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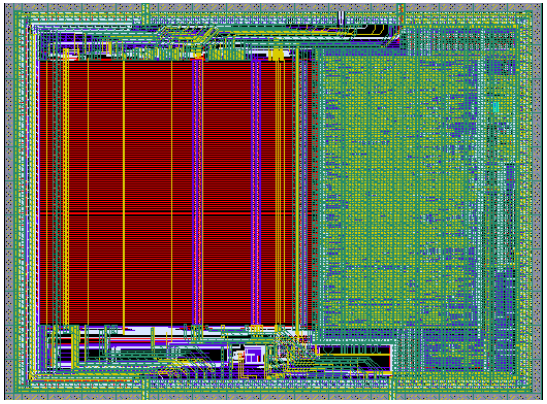
Organization for Micro-Electronics desiGn and Applications

HARDROC3

Omega

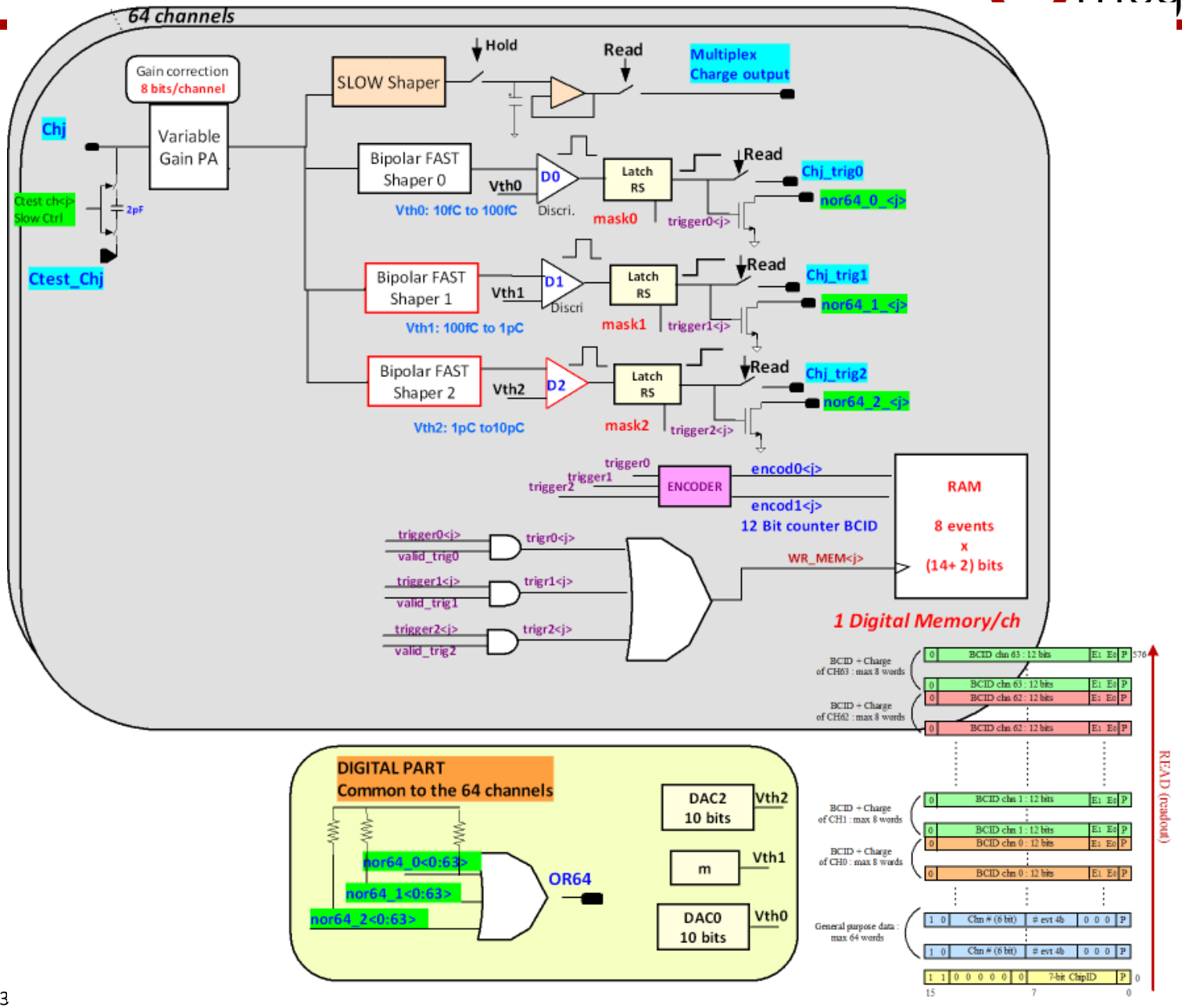
- **3rd generation chip for ILD**
  - **Independent channels (zero suppress)**
  - **I2C link (@IPNL)** for Slow Control parameters and **triple voting**



- HARDROC3: 1st of the 3rd generation chip to be submitted
  - analog part: extension of the dynamic
  - PLL: integrated to generate clocks internally
  - Submitted in Feb 2013 (SiGe 0.35µm), funded by AIDA, received end of June 2013
  - Die size ~30 mm^2 (6.3 x 4.7 mm^2)
  - Packaged in a QFP208,
  - HR3 will equip 2-3m RPC chambers

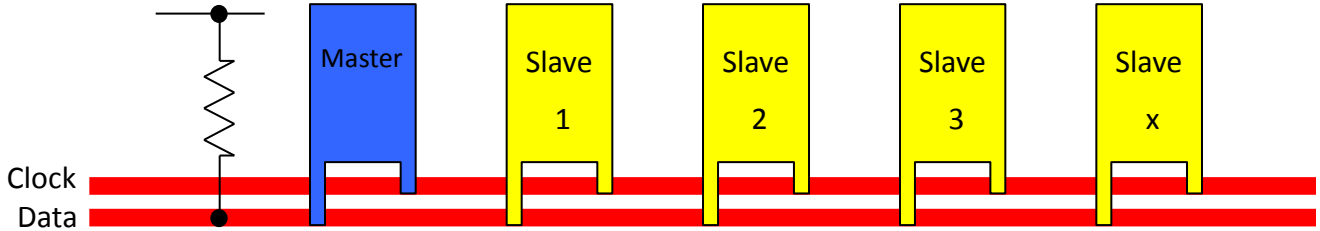
AIDA

SIMPLIFIED SCHEMATICS



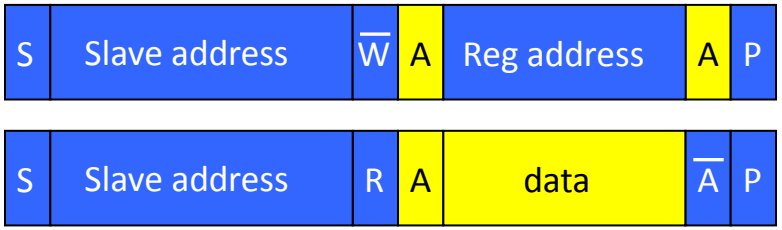
3rd generation: Slow Control parameters

- Slow control parameters:
  - Backward compatibility with 2Gen ROC chips slow control
    - Use of classical shift register slow control
  - Embedded I2C
    - 7-bit address + 1 general call address (127 chips can be addressed)
    - Access port doubled
    - Bidirectional data line with open collector (Driver will be the same as Dout)
  - Read back capability of SC bits (non destructive)



Write frame:

Read frame:



Pb: data stuck to 0 inside the chip
(buffer added by OMEGA to output the data)
⇒ Not possible to test the I2C link
⇒ Use of the old SC system

3rd generation SC

- Extra pin needed for I2C / SC:
- Possibility to choose between old SC registers/ New I2C link (Select_I2C_SRb) available on one pin)

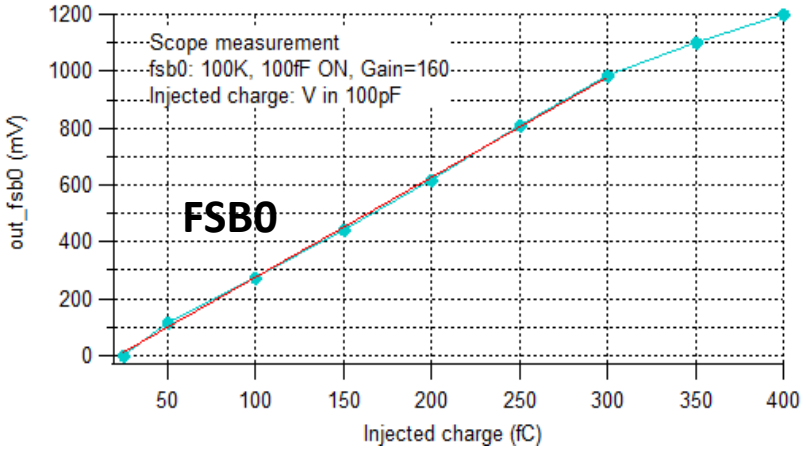
HR 2		HARDROC 3		
sr_in	1	sr_in	1	
sr_out	1	sr_out	1	
sr_clk	1	*sr_clk*	*1*	*Also for I2C*
sr_rstb	1	*sr_rstb*	*1*	*Also for I2C*
		Loadb_sc	1	
		SC_WR_RDb	1	Read back SC
		Error_SCb	1	Triple V. error
		Select_I2C_SRb	1	Selec old/new SC
		Select_I2C_Port	1	2 I2C ports
		2 x (I2C_clk / I2C_data)	4	2 I2C ports
		7-bit I2C: ChipID<0:6>	*7*	*I2C address* *Hardwired on PCB*

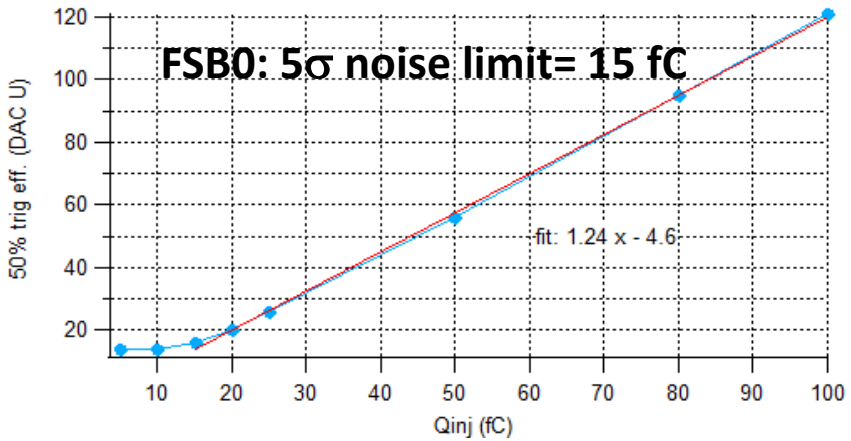
Standard SC

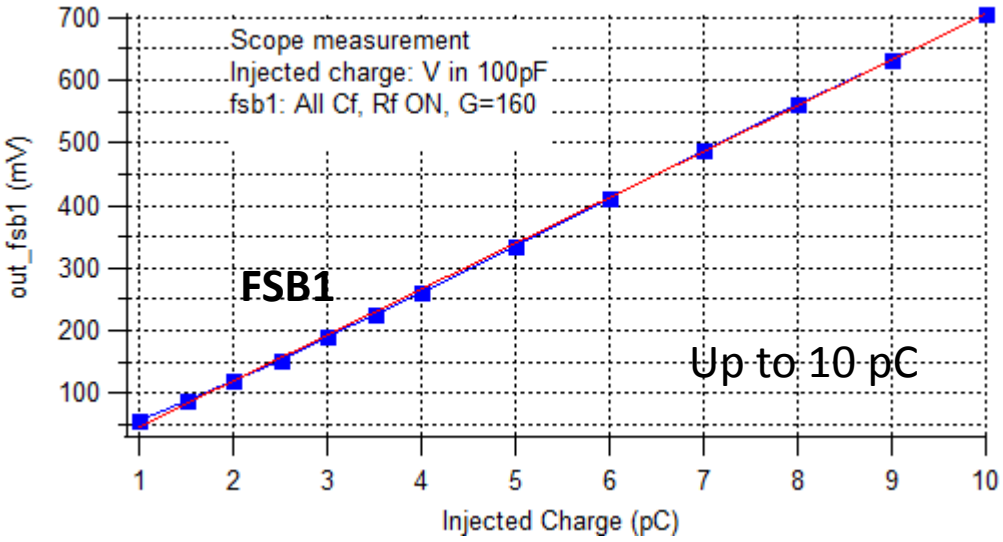
SC with triple voting

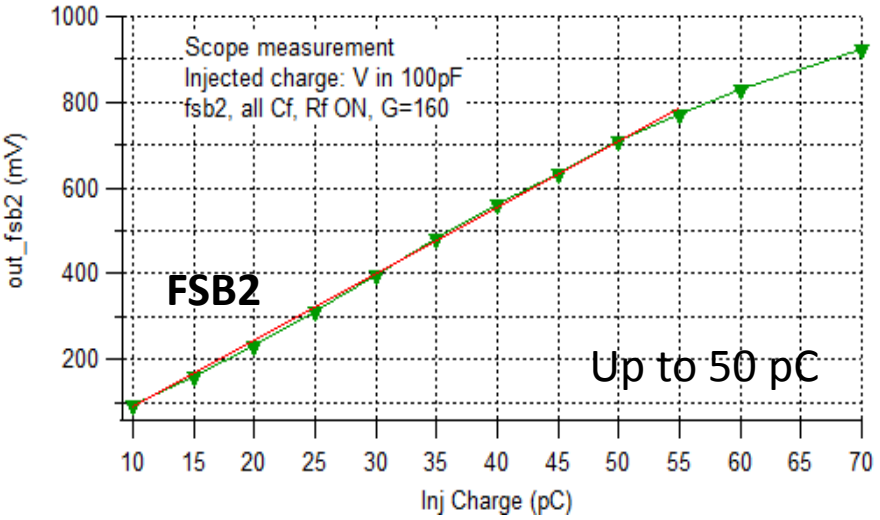
I2C

ANALOG PART: FSB LINEARITY



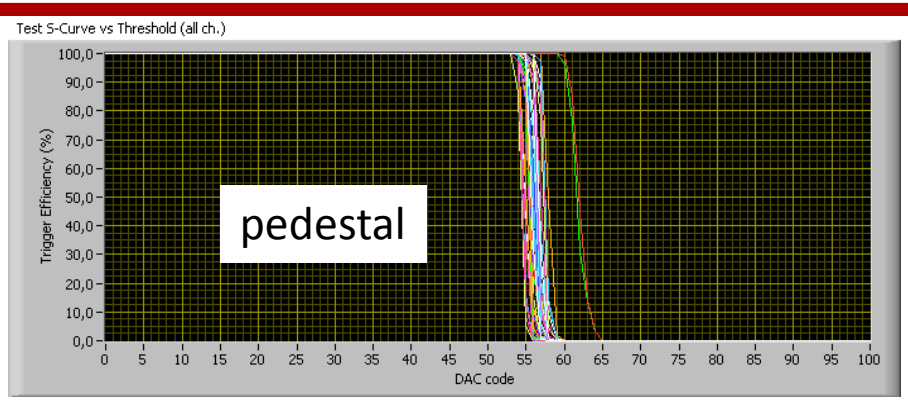


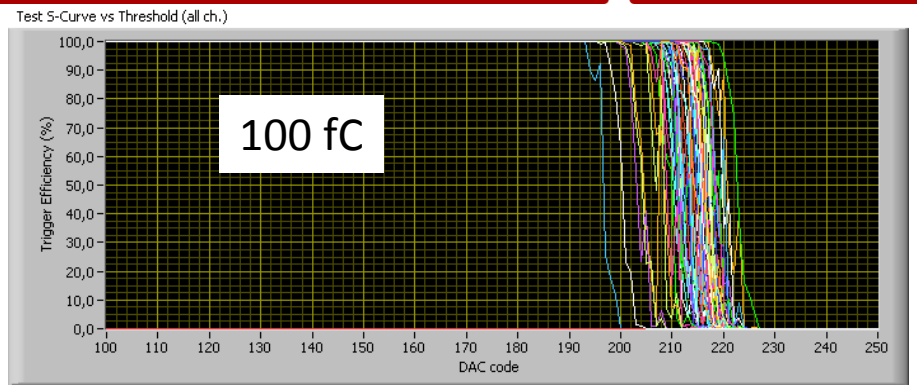


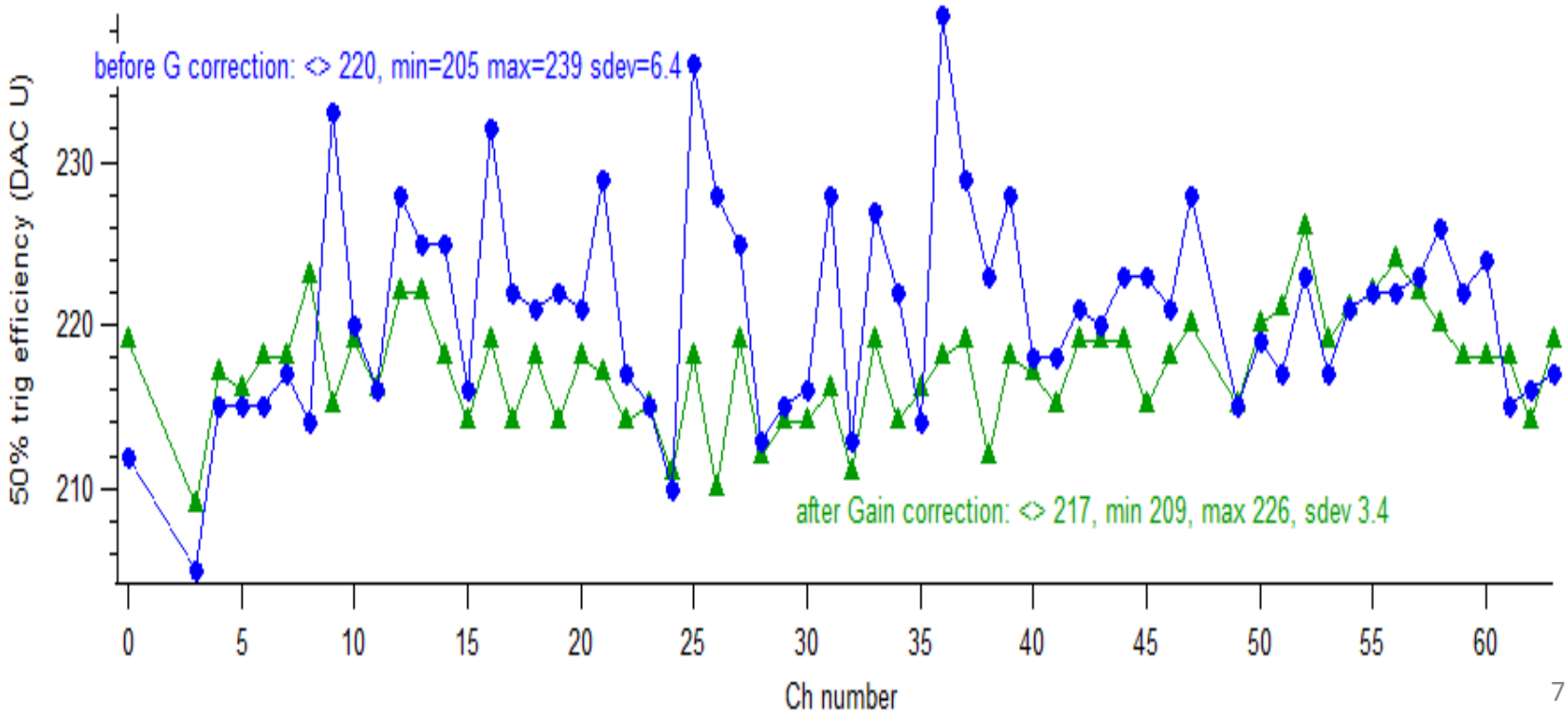


SCURVE MEASUREMENTS

Omega







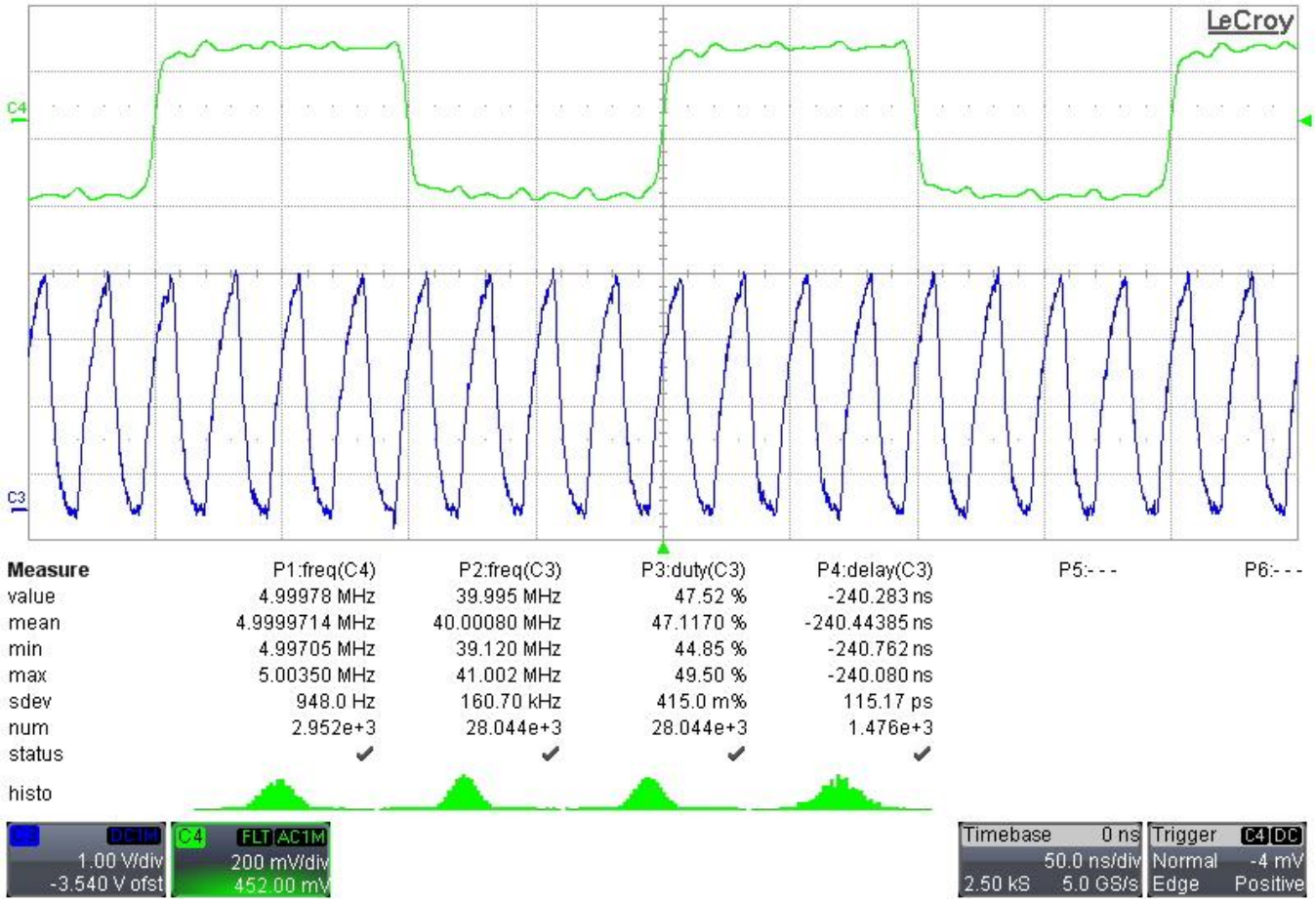
HR3: PLL tests

Input LVDS clock @ 5 MHz:

⇒ Mult factor = N+1 = 8

⇒ Output freq of PLL = 40 MHz

⇒ Full chain tested with charge injected on chn 31 and readout on serial link



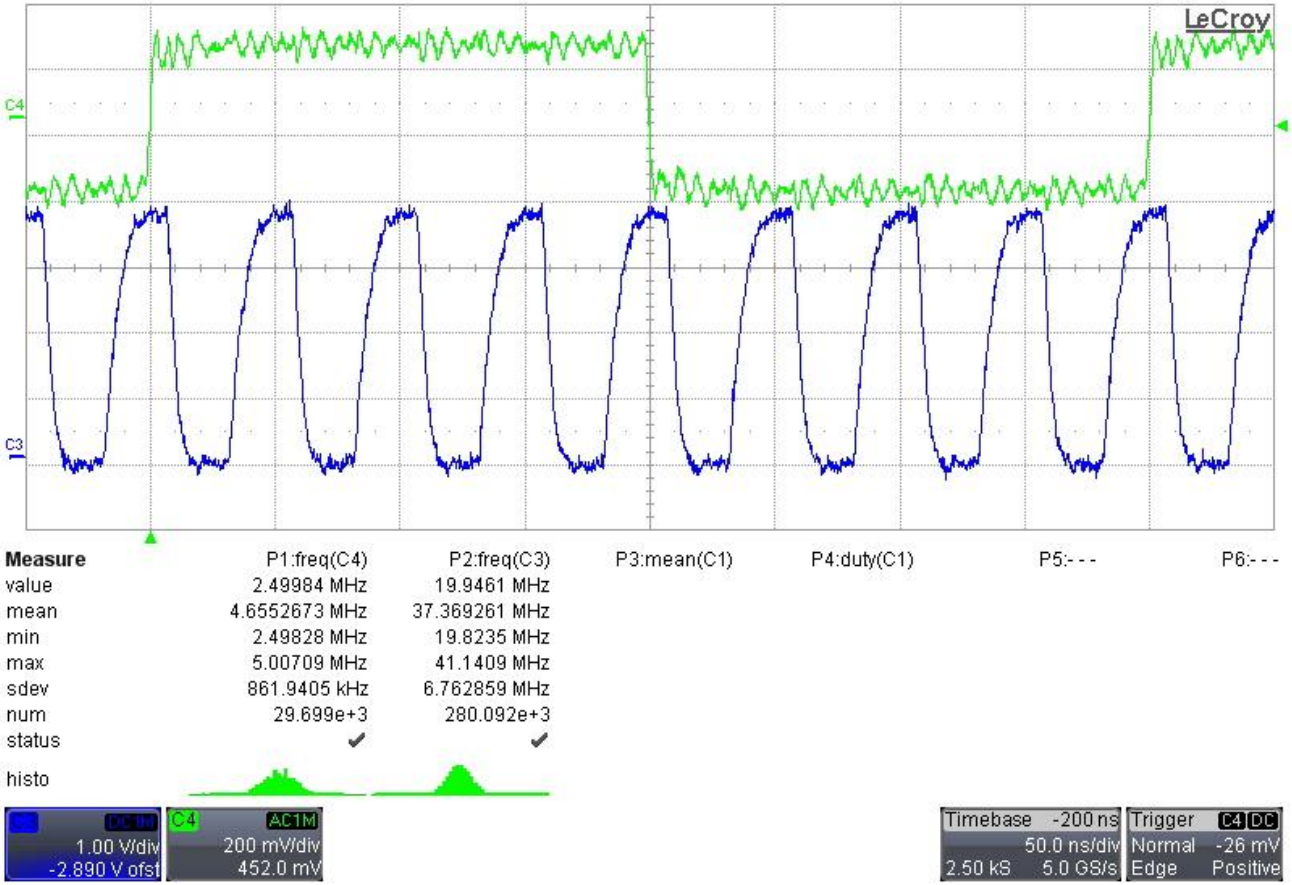
HR3: PLL tests

Input LVDS clock @ 2,5 MHz:

⇒ Mult factor = N+1 = 8

⇒ Output freq of PLL = 20 MHz

⇒ Full chain tested with charge injected on chn 31 and readout on serial link

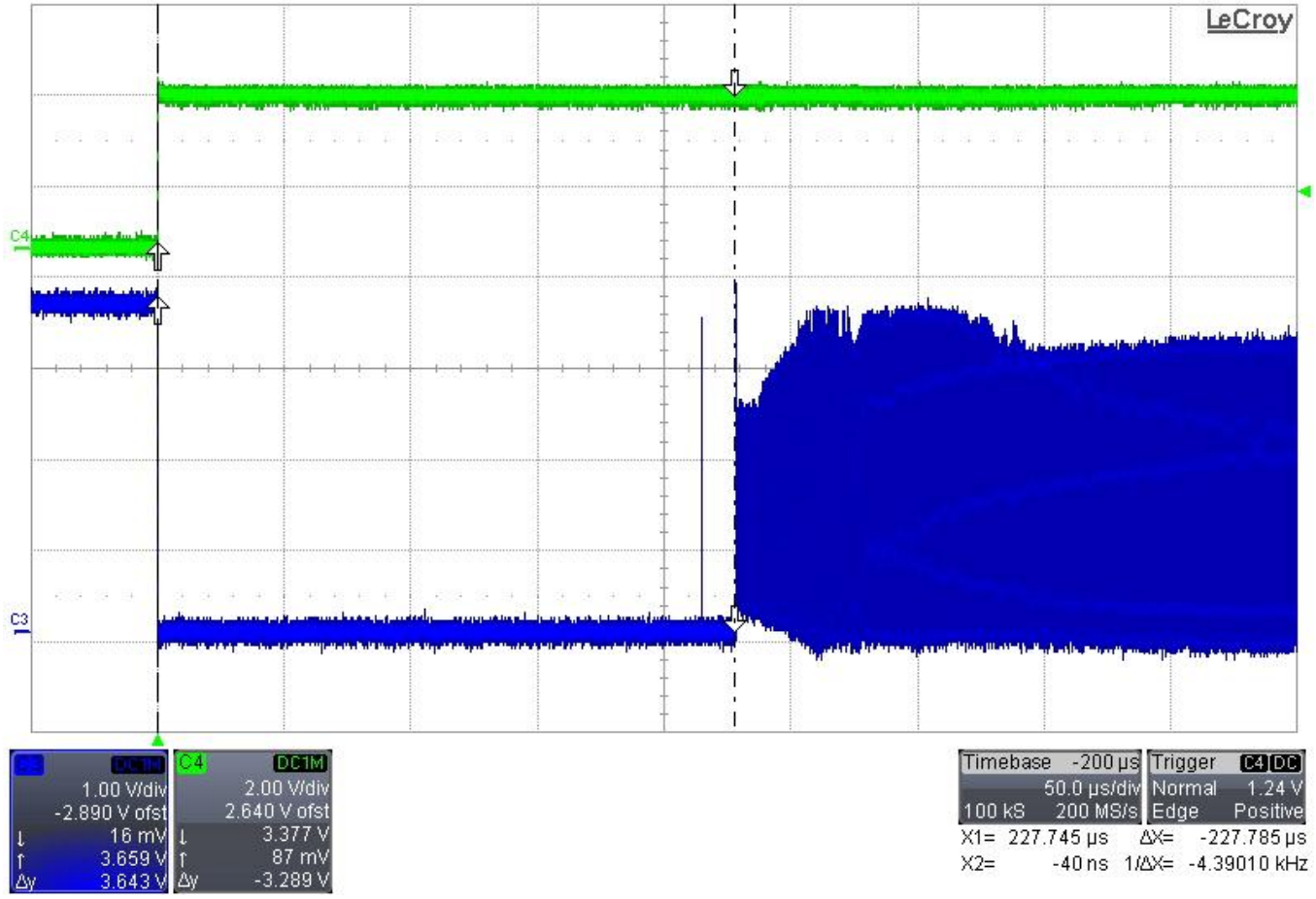


HR3: PLL lock time

Lock time (start time):

⇒ Green = PowerOnD / Blue = Out_PLL

⇒ Time needed to have a stable clock = 230 + 30 = 260 µs



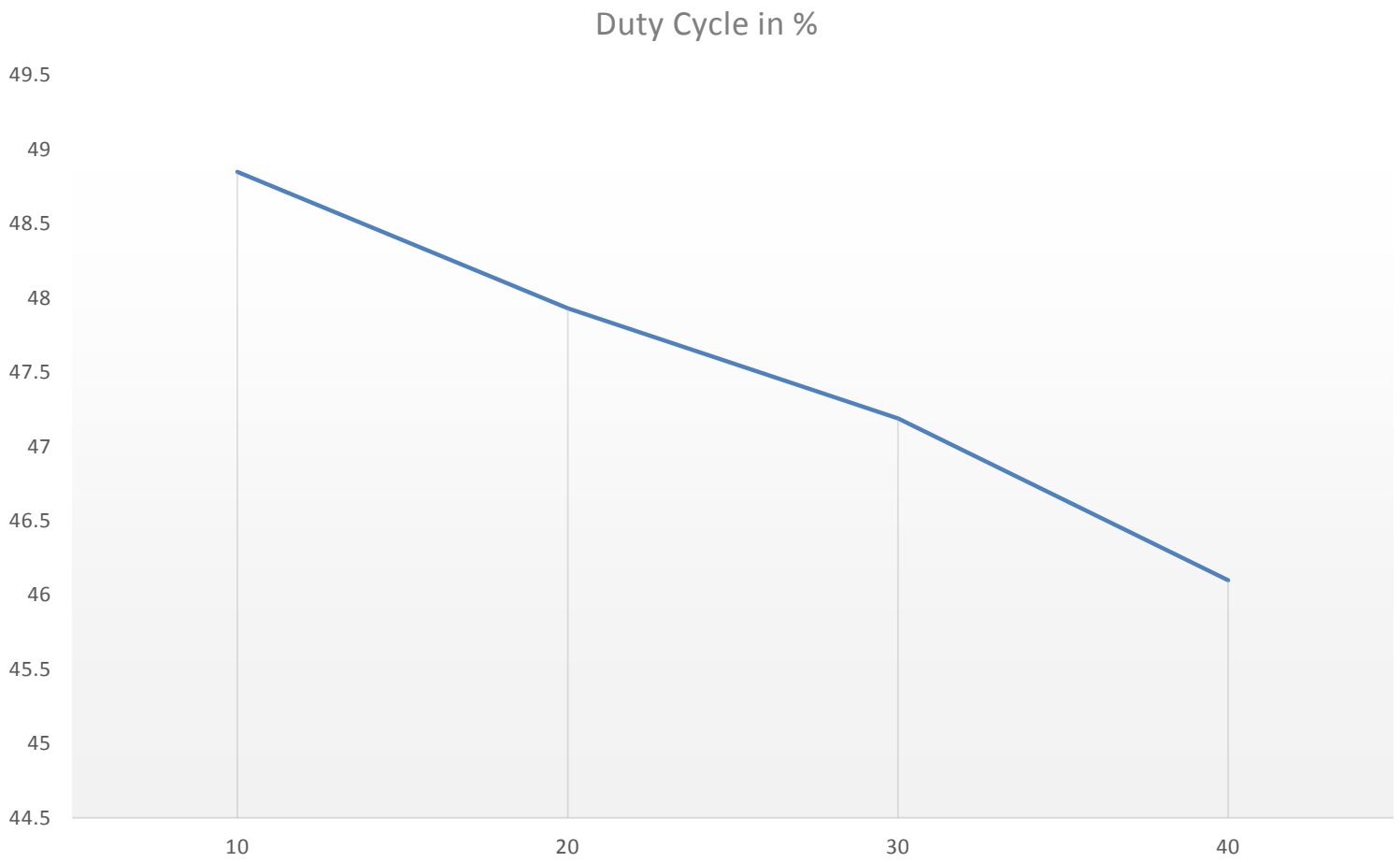
HR3: PLL Duty cycle

Input LVDS clock @ 5 MHz:

⇒ Mult factor = 2 / 4 / 8 / 16

⇒ X = freq of Out_PLL

⇒ Y = duty cycle in %



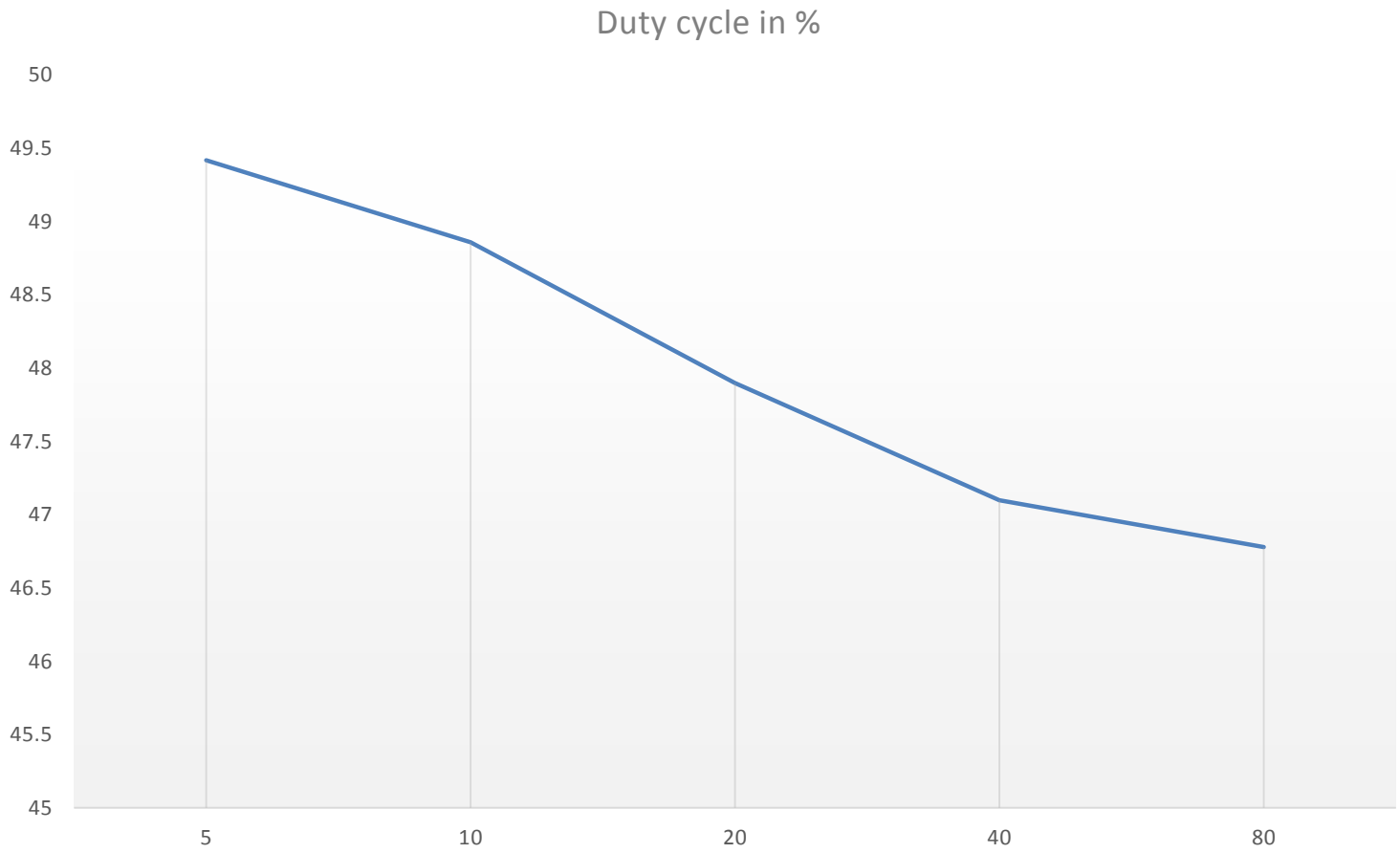
HR3: PLL duty cycle

Input LVDS clock @ 2,5 MHz:

⇒ Mult factor = 2 / 4 / 8 / 16 / 32

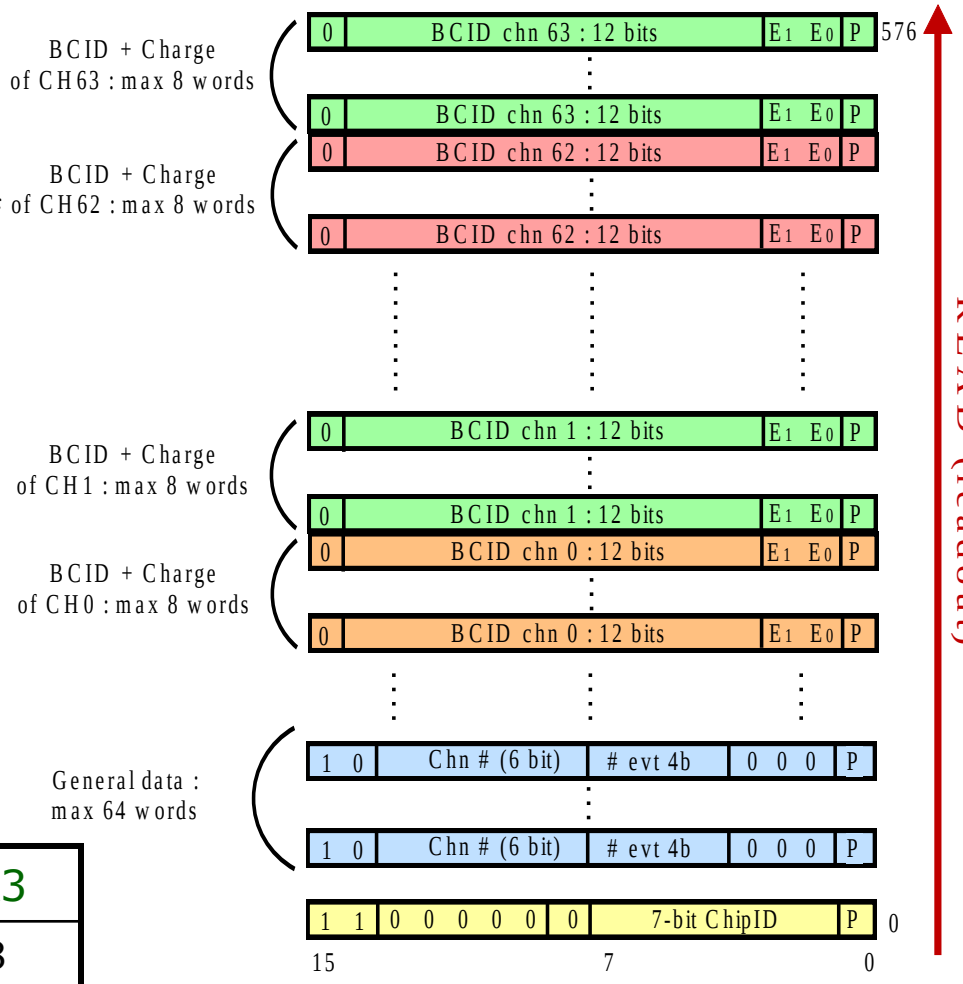
⇒ X = freq of Out_PLL

⇒ Y = duty cycle in %



HARDROC 3 : Memory mapping

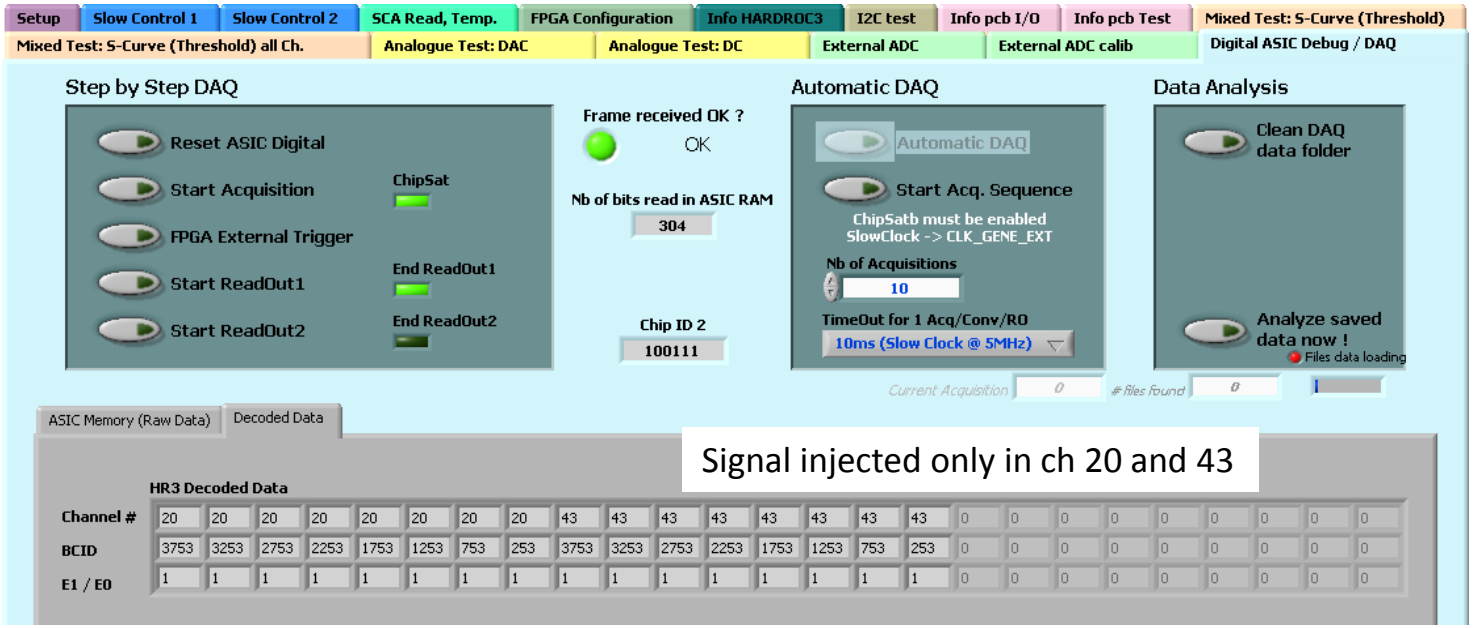
- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - "1": general data (Hit ch number and number of events)
  - "0": BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:



	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336

HARDROC 3 : digital part

- Zero suppress (only hit channels are readout): test OK



- Roll mode SC : test OK
  - If RollMode = "0" ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = "1" ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored
- "Noisy Evt" SC: 64 triggers => Noisy event => no data stored : test OK
- "ARCID" SC (Always Read Chip ID): test OK
  - If ARCID = 0 ➔ Backward compatibility: No event ➔ No readout
  - If ARCID= 1 ➔ New behavior: No event ➔ Read CHIP ID

Summary and next steps

- Good analog performance:
  - dynamic range extended up to 50 pC
  - PLL => clocks generated internally
- Preliminary good digital performance
  - Zero suppress, roll mode, ARCID mode, Noisy evt mode tested successfully on testboard
  - External trigger available to be able to check the status of each channel
- I2C link
  - FIB on 2 chips to test the link
- 2-3m long RPC chambers to be built and equipped with HR3 in 2014