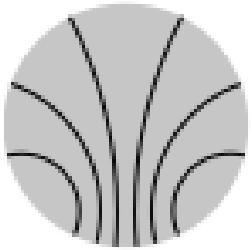
Peak Sensing ADC for SiPM readout

Wei Shen



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Outline

- ✓ *Motivation & Requirements of the ADC*
- ✓ Analog to *Digital Converter structure*
  - *Peak holder*
  - *SAR capacitor array*
  - *Switches*
  - *Comparator*
  - *Residue amplification*
  - *Power estimation*
- ✓ *Status & Time Plan*

Motivation and Requirements

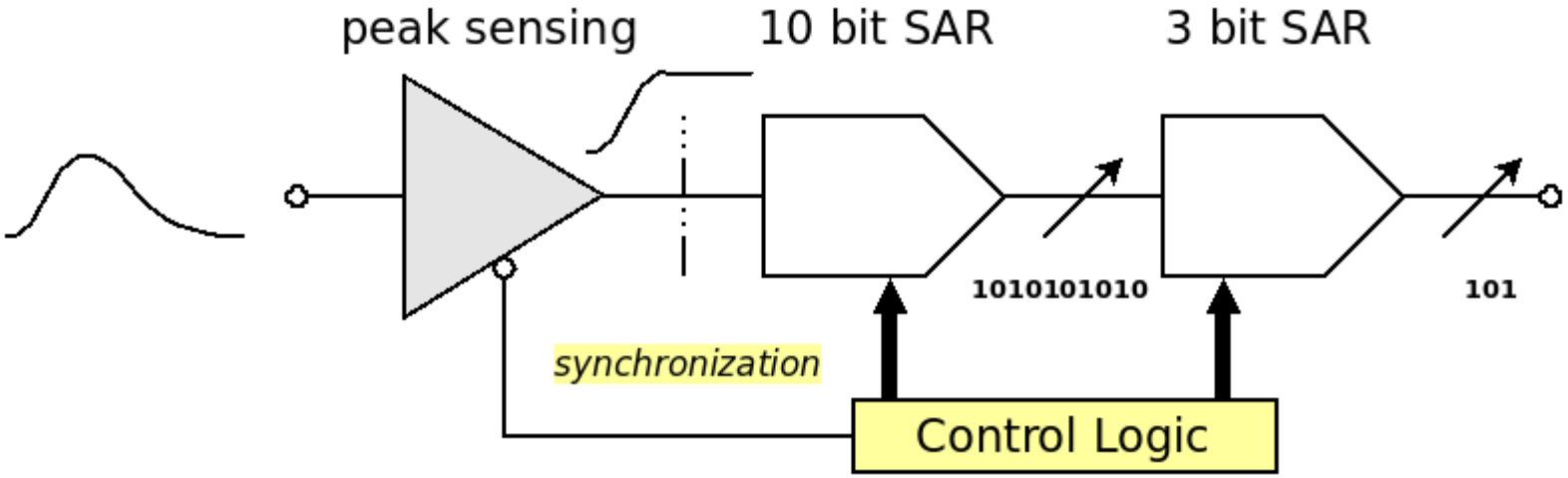
- ✓ *Quatization (one ADC per channel):*
  - *charge integration for SiPM output*
  - *low power < 1mW*
- ✓ *Charge collection is a time dependent process*
  - *peaking time is rather sensitive to the signal shape*
- ✓ *Resolution - 12 bits is needed in a small range*
  - *3 different types of signal to quantize:*
  - ☆ SiPM calibration signal

    12 bits, $\sigma = 260\mu V < \sigma_e$
  - ☆ physical MIP-like signal

    ramp voltage

    10 bits, $\sigma = 1.04mV \sim \sigma_e << S_{pixel}$

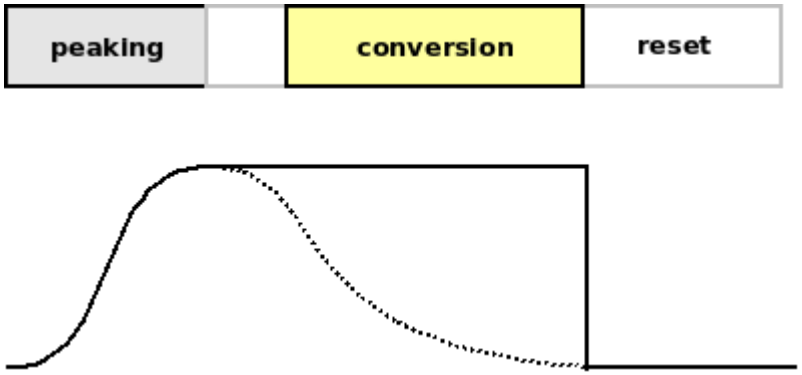
ADC structure



- *Random signal peak tracking >1.2V*
  peaking time > 50ns
- *Peak identification is provided for synchronization*
- *SAR sampling rate 5MS/s , but not limited*
  max 50MS/s

ADC structure

- The total processing time consists of
  - peaking time : $t_{peaking}$
  - synchronization time : t_{syn}
  - conversion time : t_{conv}
  - reset time : : t_{reset}



shaping time $\tau = 50ns$, samping rate $= 5Ms/s$

$t_{peaking} = 100ns$, $t_{conv} = 200ns$

$t_{syn} = 20ns$, $t_{reset} = 150ns$ (5%)

$t_{total} = 470ns$, $< 10\ \tau$

direct signal processing + conversion

The data taken is only dependent on the FIFO size

✓ $\tau = 25ns$, $10Ms/s$, $t_{total} < 350ns$

Circuit units - umc 0.18µ

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Peak holder

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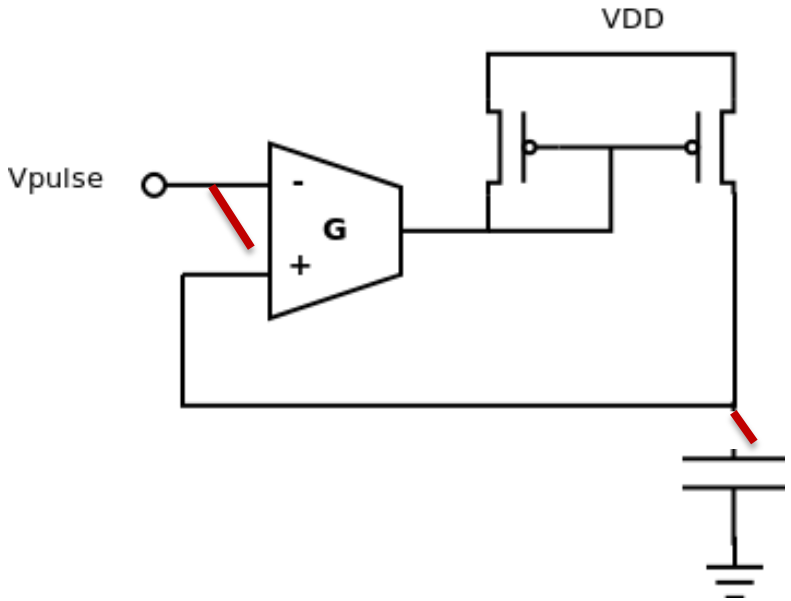
3 functional phases

tracking (sampling switch)
peaking
reset (fast recovery needed)



capacitor is shared by the SAR array

bootstrape switch is needed
non-linearity should not be affected by signal amplitude.
Only a constant part

Peak holder - simulation

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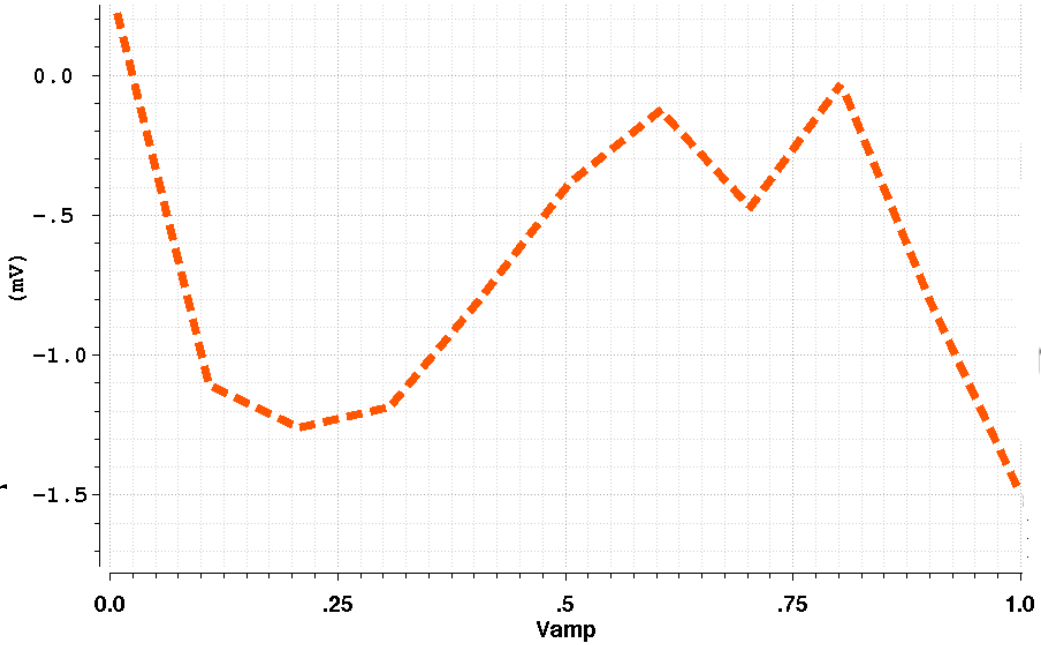
Offset is expected, but differential operation might rescue Pedestal tracking beforehand

Residue smaller than +/- 1mv in all signal range

nevertheless, only the small signal part needs 12 bit resolution



SAR capa array

- Largest Error comes from switch of the MSB

  DNL = $(2^k - 1)dC/C$ LSBs

  k=10 , DNL < 1 LSB, dC/C must be better than 0.1%

  According to the UMC datasheet, for Cpoly W=L > 7um, 10um will be taken

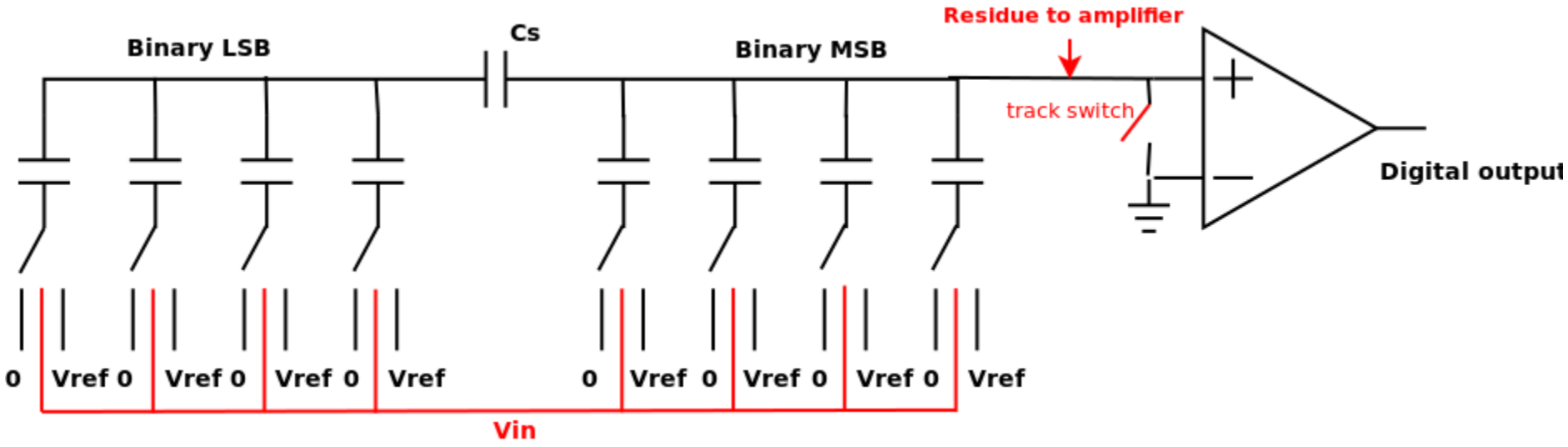
- The total size of the C-array

  32um * 100um, differential 64um *100um

  KT/C noise, (thermal noise comes from the switch channel resistance) will be around 0.2 mV

Setting time < 10ns

SAR capa array



SAR capa simulation

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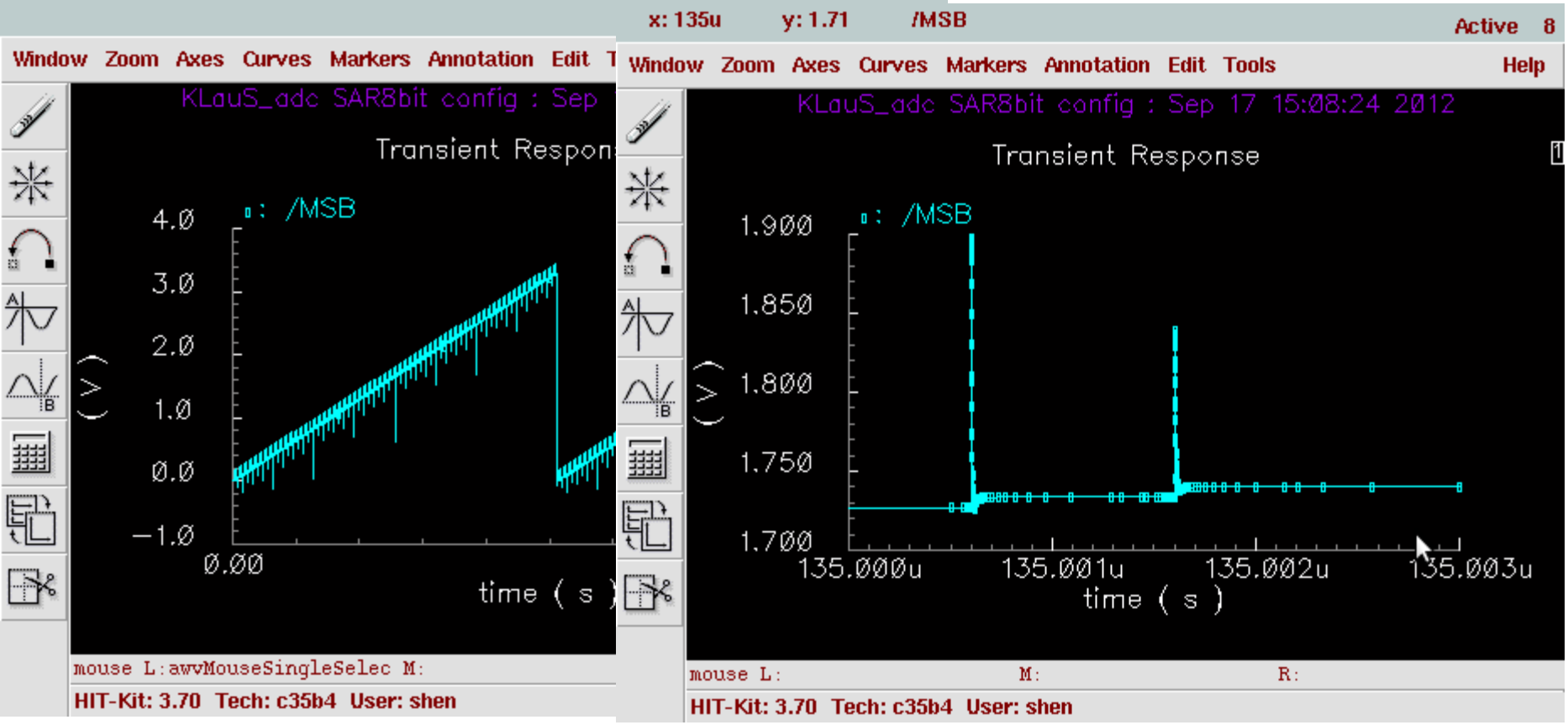
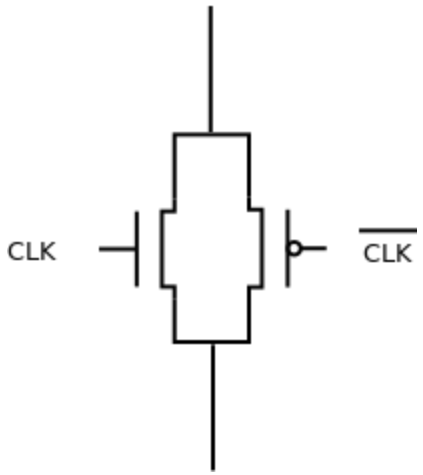


DNL/INL < 0.5 LSB

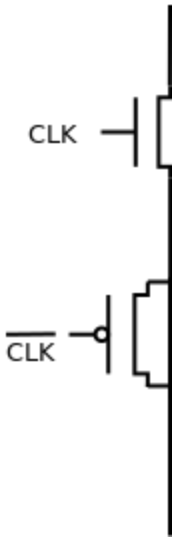
response fast enough

switch design

- There are 3 types of signal to switch
- vcc, gnd, signal, 3 different switches need



gnd
switch



No complete cancellation

At all corners, error about 1-2mV in MC connected to Cmin,

Max error +/-125uV at comparator

switch design

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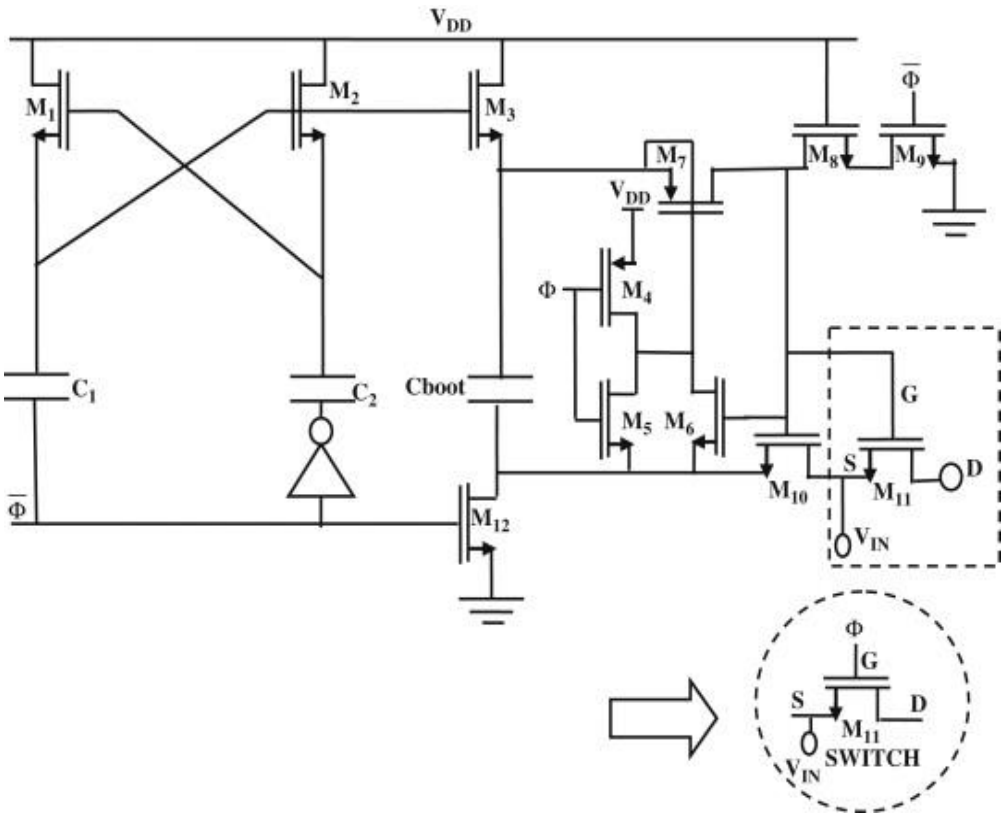
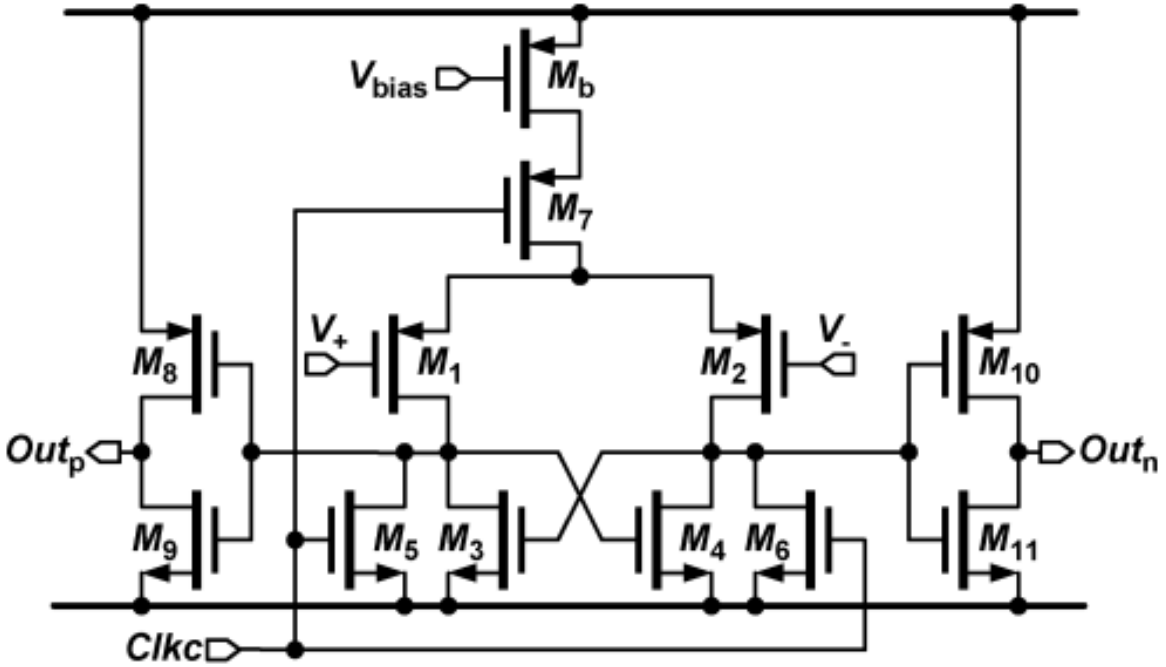
- For signal, range range from 0 to 1.8V, switch with P/N mos is necessary, but the channel charge / clock feedthrough is dependent on input signal:

  Bootstrap Switch



compatator design



dynamic comparator

fast response time
simple latch structure

no DC power

Mb is used to reduce mismatch error

- Current source Mb sinks 20uA
  no DC power
  AC power < 5uW response speed <1.5ns

Residue Amplification

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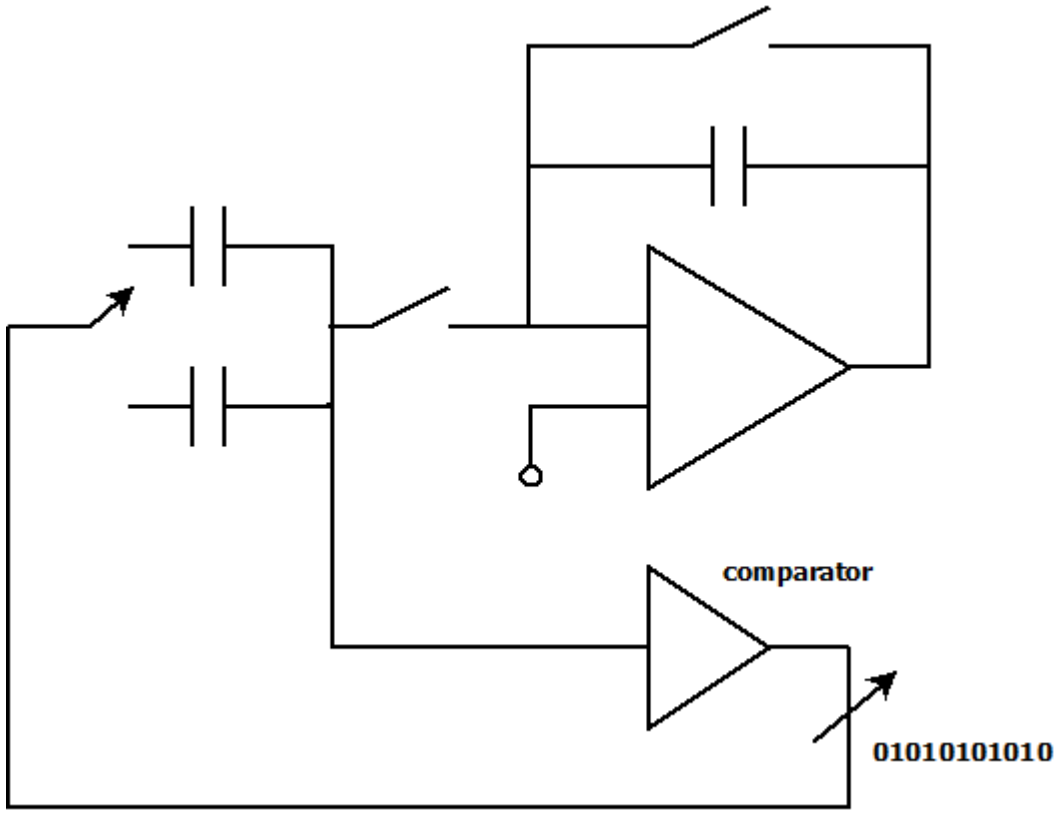
- Only functional in the calibration mode 12 bits
- Residue is amplified by

$C_{array}/C_{feedback}$

Detailed

switch control

Is necessary



Power estimation

- The power consists of **5** components
  - peak sensing (amp, additional comparator)
    - amp = 350μW , additional comparator = 50μW
  - capacitor track power
    - 1μW (1% occupancy)
  - SAR switching power
    - 80μW (max)
  - dynamic comparator
    - 5μW
  - control logic 100μW

In total < 600μW (aggressively, 400μW)

Status & summary

- SAR ADC structure chosen
- 12 bits = 10 + 3 with 1 bit redundancy
- SAR part

  peak sensing , switches, comparators finished

  control logic and fine tuning

  residue part not finished yet

Tape out , spring 2014, UMC 0.18μ CMOS