Status of DAQ System for Scintillator Calorimeters.

- Design concept
- DAQ Software
- Clock and Control Card (CCC)
- Link and Data Aggregator (LDA)
- Future plans

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Calorimeter for ILC

HELMHOLTZ ASSOCIATION

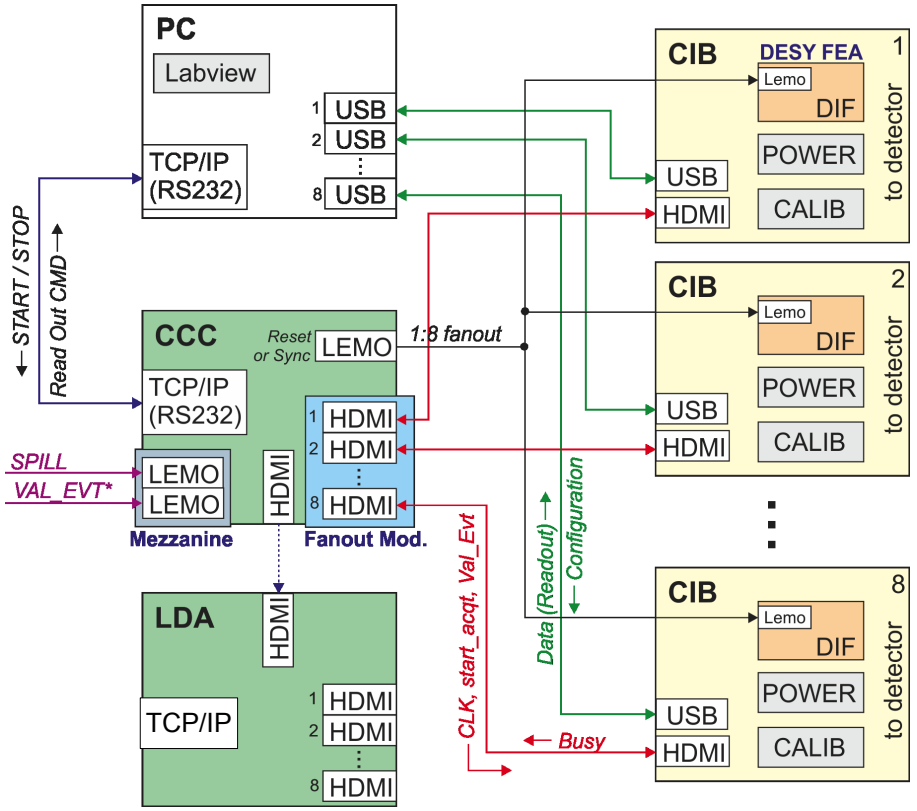
THE PICOSEC MC-NET PROJECT

Universität Hamburg

DESY

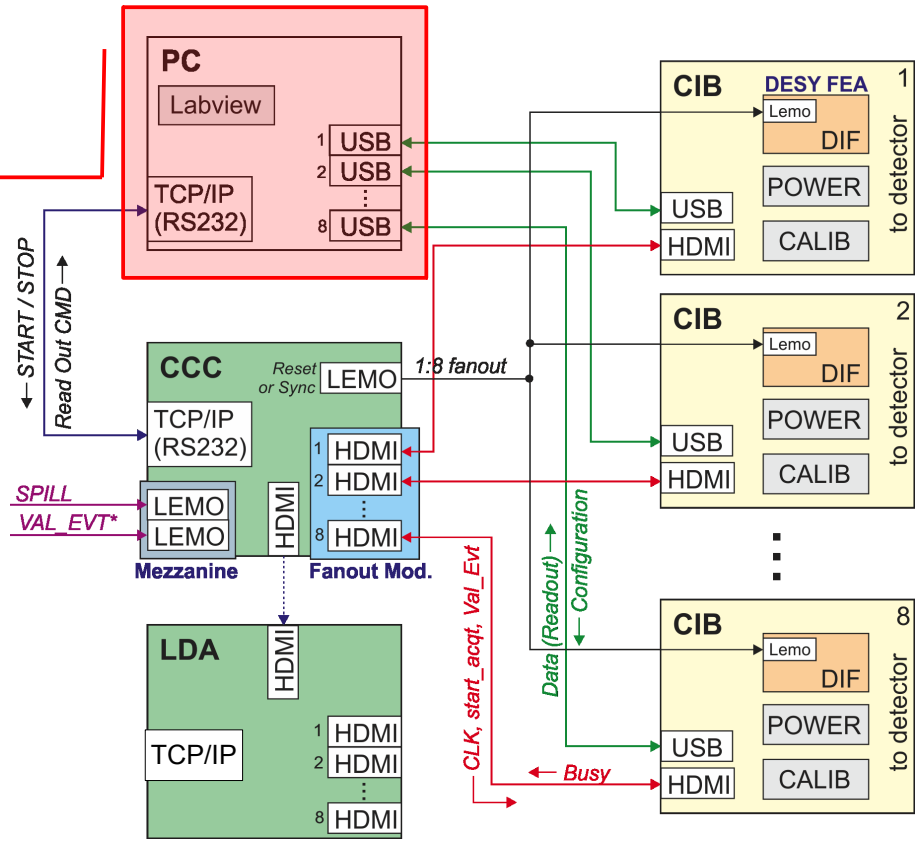
DAQ Design Concept

- The original DAQ could operate only one layer
- New multilayer DAQ based on the original CALICE DAQ concept
- Built on the single layer DAQ
  - Software improvement
  - Multiple-DIF configuration
  - Global clock and control
  - Data aggregator
  - Parallel readout
  - Scalable
- Currently there are 2 connections to DAQ interfaces (DIF):
  - HDMI for fast signals
  - USB for slow signals and data

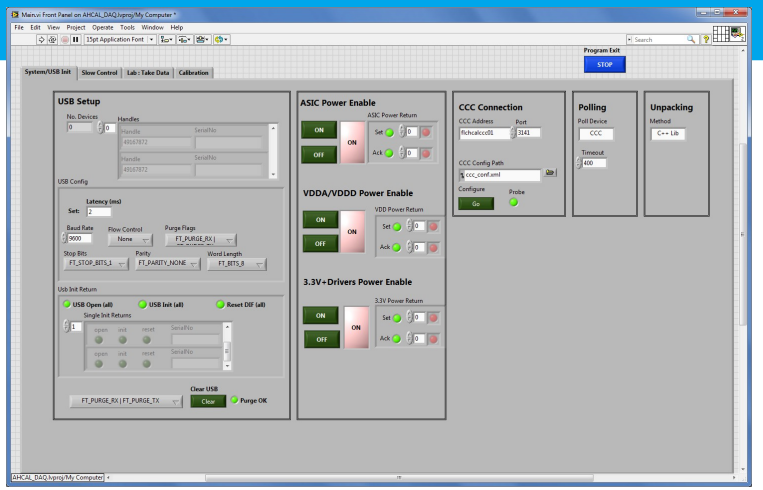


Main DAQ components

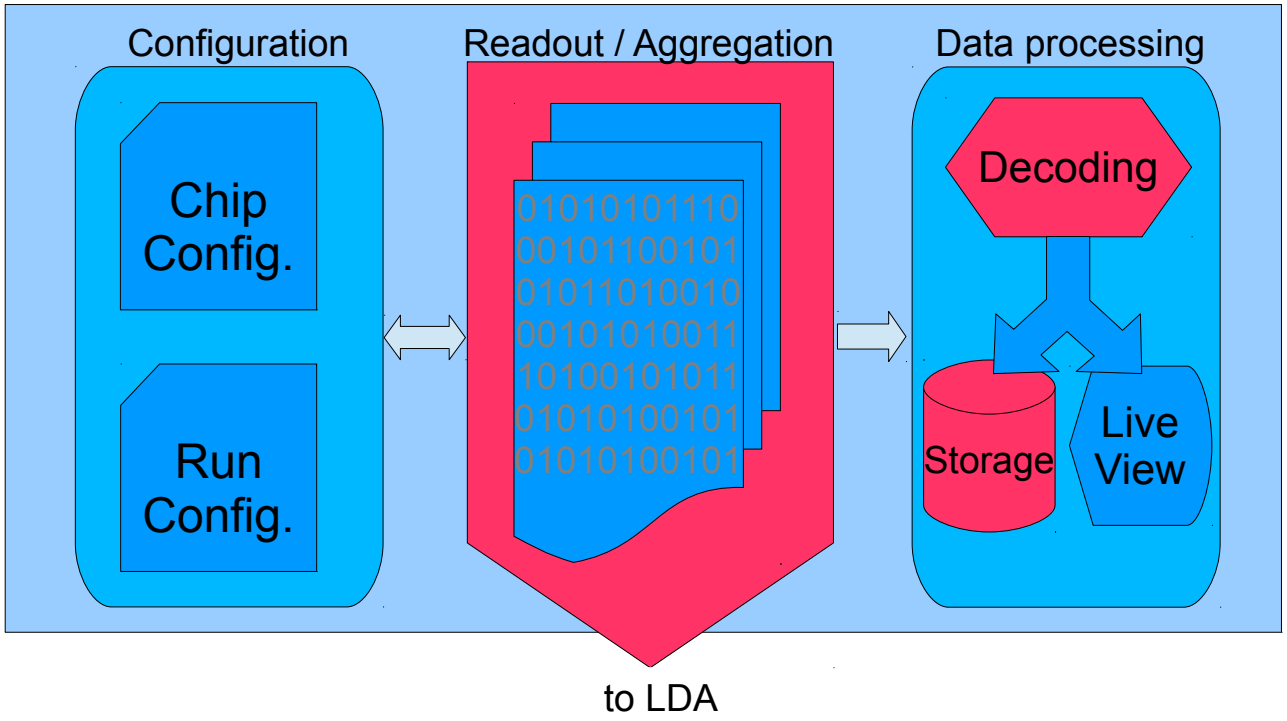
- DAQ Software
- Clock and Control Card (CCC)
- Link and Data Aggregator (LDA)



AHCAL DAQ Software

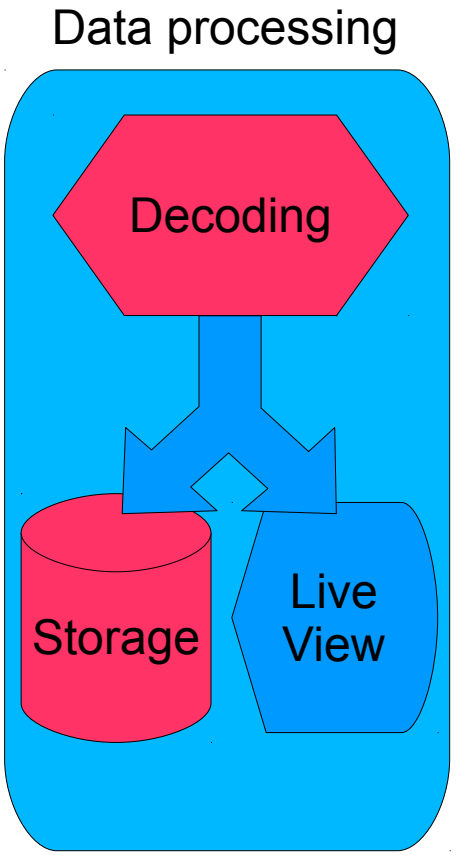


- Based on LabView
  - Live monitoring, easy modifications
- Some tasks done using C++ libraries
- Multithreaded
- Modular



C++ Libraries for Decoding and Storage

- A C++ windows library (DLL) is developed to replace native LabVIEW decoding
  - Faster by a factor of 5
  - Calling the C++ DLL from LabVIEW is ~20% faster
  - Decoding algorithm will be optimized to make it even faster
- ASCII file output for storage
  - In current version LabVIEW handles the storage
- A LCIO converter function is developed and is tested in Linux environment
  - Not implemented in DAQ software as of yet
  - To be added to the LDA master software



Main DAQ Components

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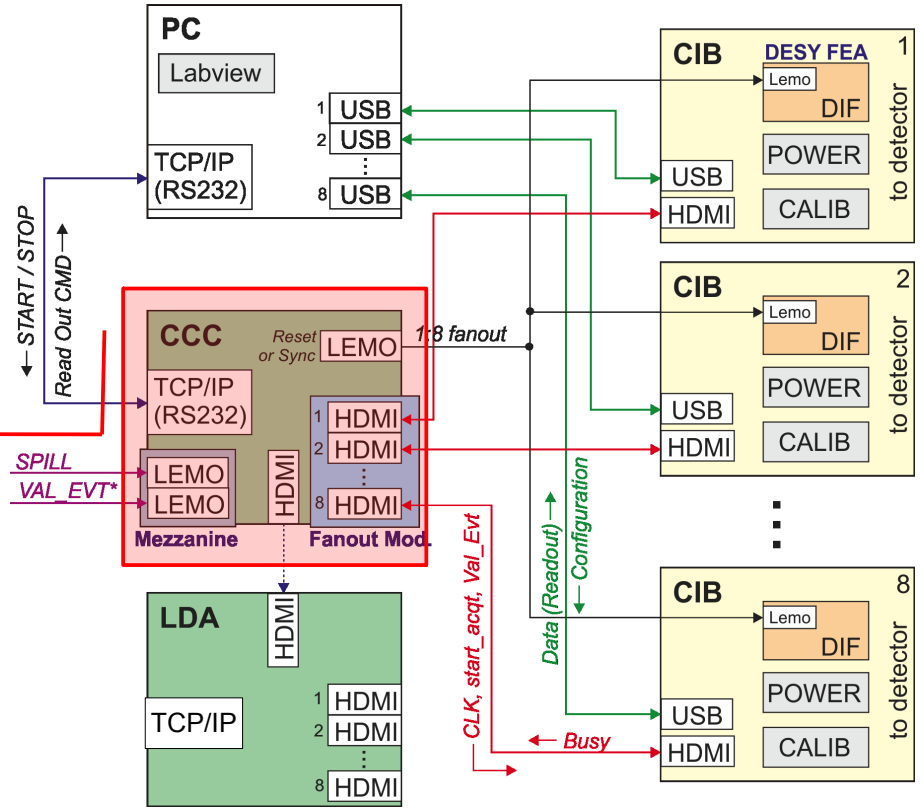
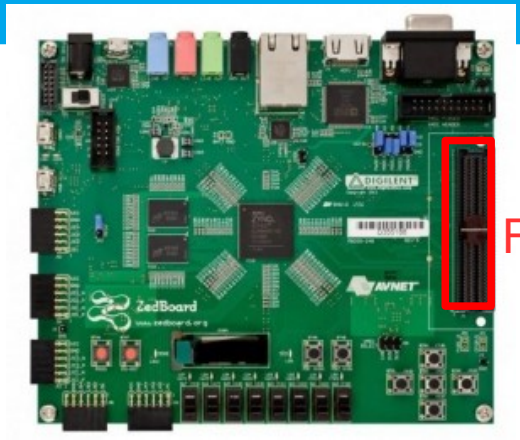
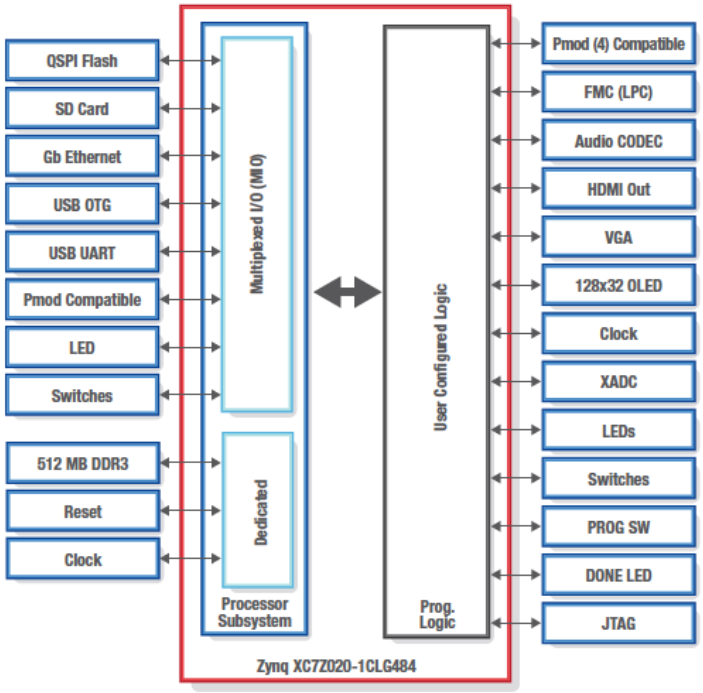
- Link and Data Aggregator (LDA)



ZedBoard

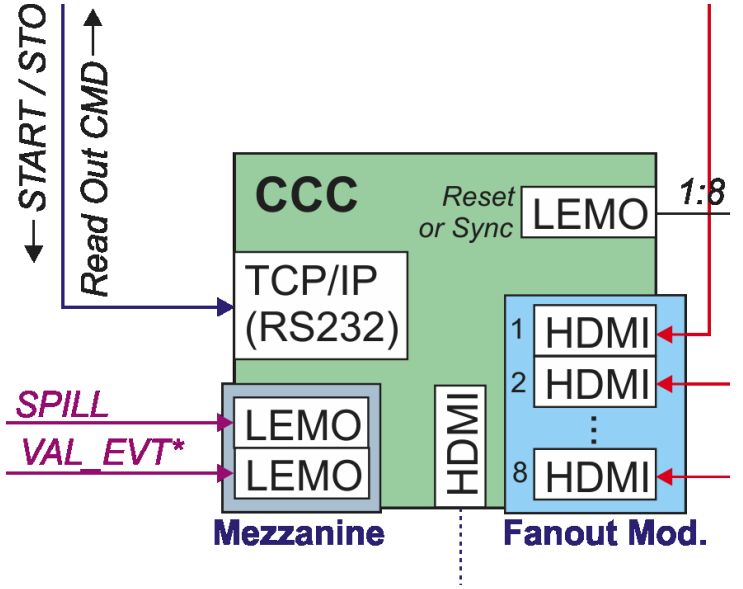
- Zynq Evaluation & Development Board
- Xilinx Zynq-7000 SoC
  - Processor Subsyst. (PS): Dual ARM Cortex-A9
  - Programmable Logic (PL): Xilinx 7 series FPGA
  - 100Gbps interconnect bandwidth
  - ARM programmability+FPGA flexibility
- On board memory
  - 512 MB DDR3 + 256 MB QUAD-SPI
- PS is able to run Linux
- FPG Mezzanine Connector (FMC)
  - Allows adding custom boards

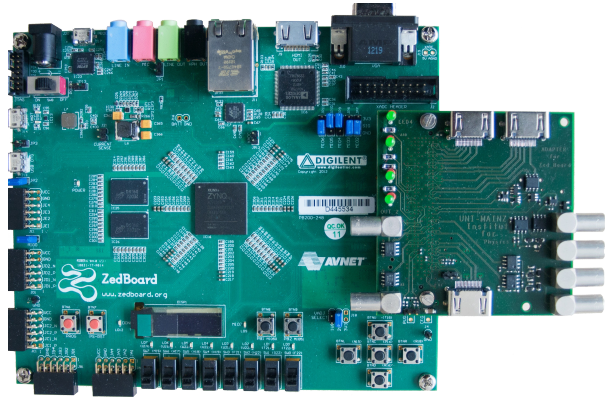




Clock and Control Card (CCC)

- New CCC design by university of Mainz
  - Compatible with CALICE DAQ
- Based on the ZedBoard
- Mezzanine board designed at Mainz uni.
- Ethernet connection to DAQ PC
  - Start / Stop / Readout
- In temp. setup while LDA is being developed
  - 8 layers are served using an 1:8 HDMI fanout
- LEMO connections for
  - Validation signal
  - Spill signal
  - Reset / Sync signal
- Tested successfully and is in operation

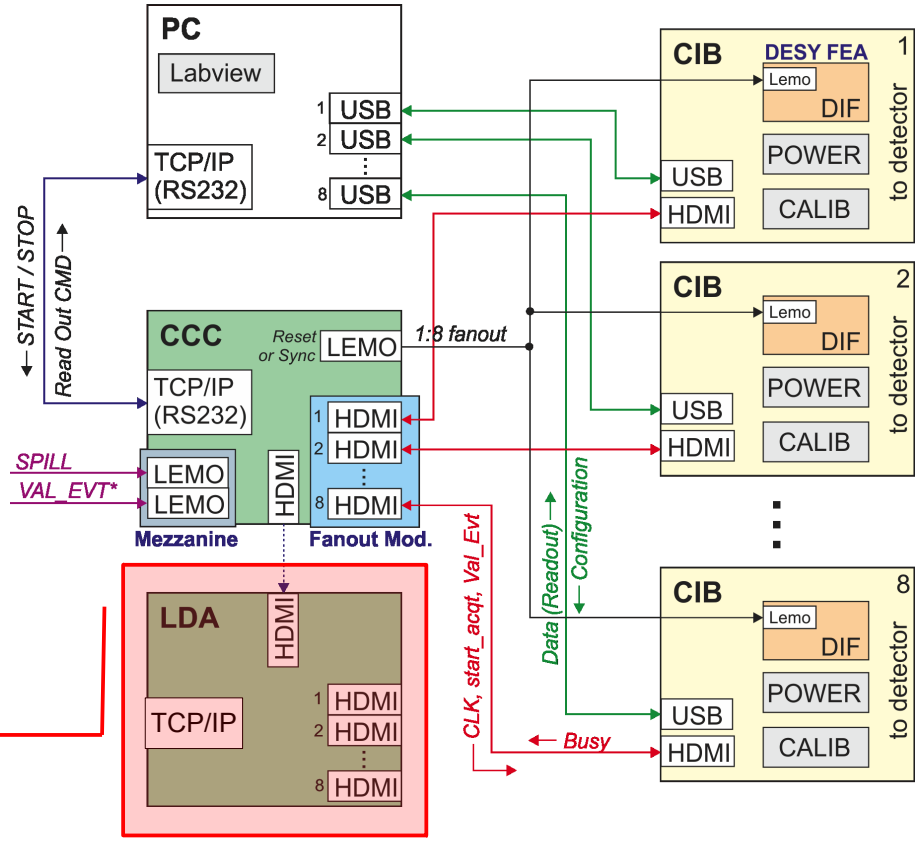




ZedBoard and Mezzanine

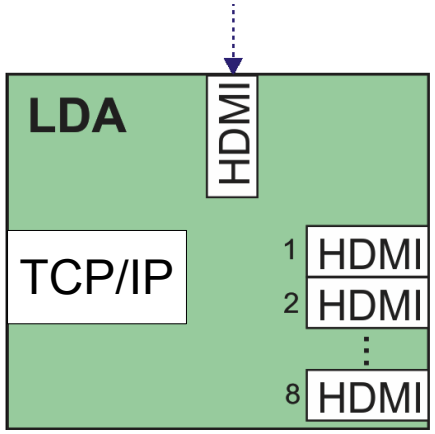
Main DAQ Components

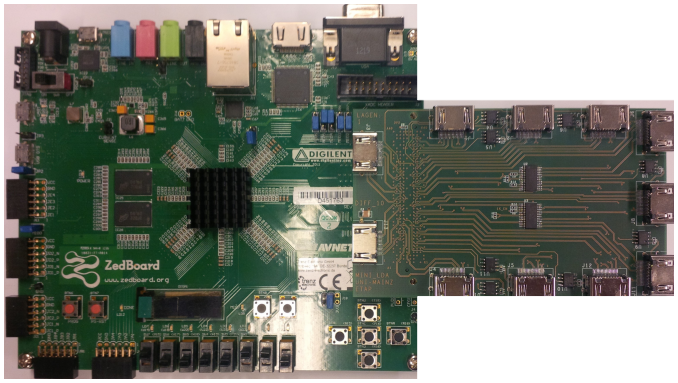
- DAQ Software
- Clock and Control Card (CCC)
- Link and Data Aggregator (LDA)



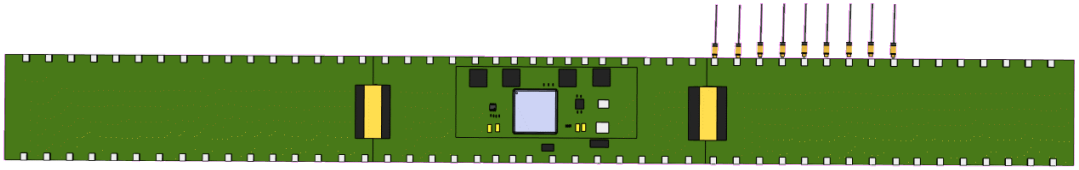
Link and Data Aggregator (LDA)

- New LDA design by university of Mainz
  - Compatible with CALICE DAQ
- Based on the ZedBoard
- Mezzanine board designed at Mainz uni.
- There are two options
  - Mini-LDA: ZedBoard + Mezzanine → Generic
  - Wing LDA → AHCAL geometry specific
- Mini-LDA hardware is ready
  - 1 HDMI connection to the CCC
  - 10 HDMI connections to the the DIFs





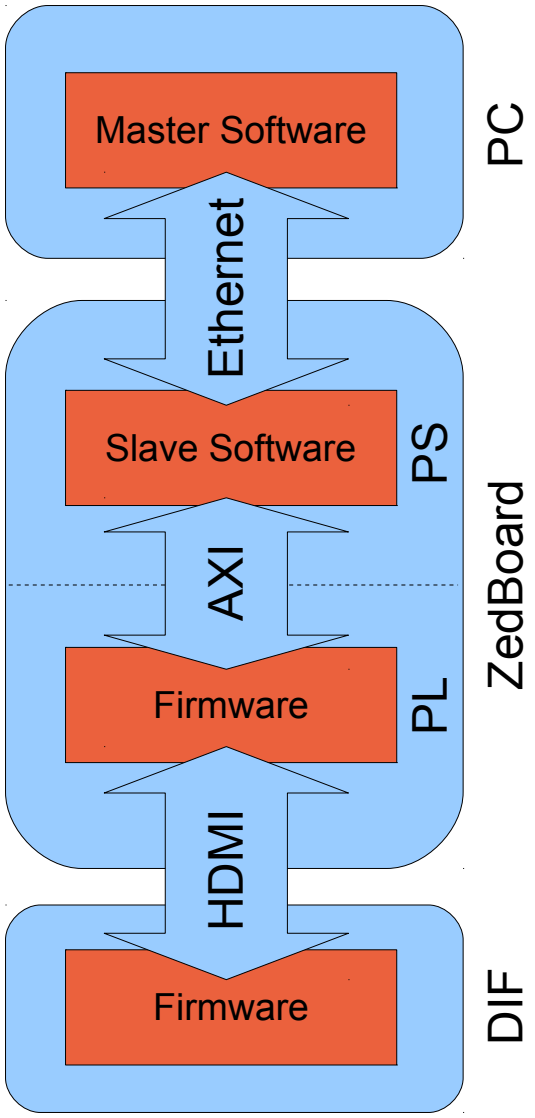
Mini-LDA and Mezzanine



Wing LDA

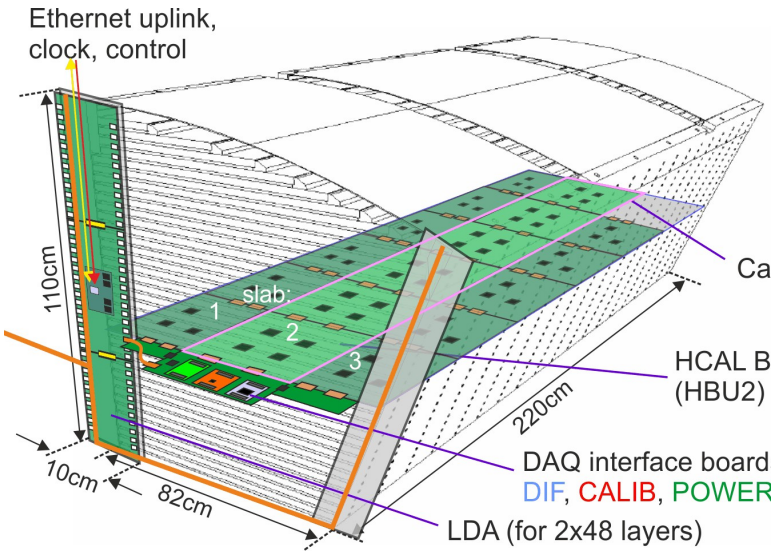
LDA Development Roadmap

- A fully functional LDA requires
  - Programming the PL (Firmware)
  - Programming the PS (Slave Software)
  - Change in DAQ software (Master Software)
- 1st step: Mini-LDA as fanout
  - Only firmware development is needed
  - To be tested during December testbeam
- 2nd step: HDMI and USB connection
  - HDMI for fast signals and reading data
  - Firmware and master/slave software development
  - Firmware is being developed at DESY, software at the university of Mainz
  - To be tested during January testbeam



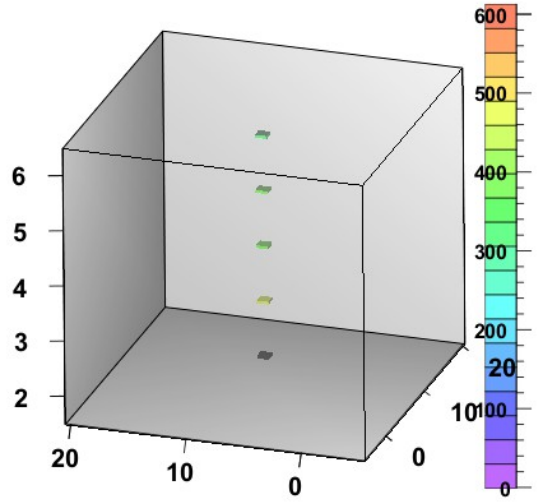
LDA Development Roadmap

- By the end of the first two steps
  - Control signals and data are transferred via HDMI
  - Level/Edge sensitive single signals
  - All twisted pairs of HDMI cable are already used
  - Slow signals are still transferred via USB
  - Therefore implementation of protocol for block-transfer and command packets is required
- 3rd step: Only HDMI connection
  - LDA Firmware
  - LDA master/slave software
  - DIF firmware modification
- Parallel development of the wing-LDA
  - To allow for more than 10 layers
  - Mini_LDA firmware and software could be adopted with minimum effort

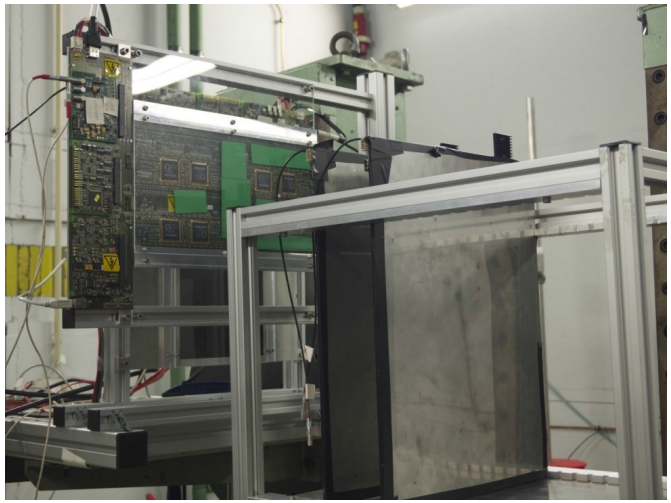


Performance of the DAQ system

- Current version of the DAQ tested in different setups
  - Lab Setup, Cosmic Muon run, Test beams
- Fully synchronous operation of 5 layers
- Very stable operation
  - 72+ hours cosmic Muon run
- Faster than ever
  - ~9Hz readout frequency
  - ~150Hz sustained trigger rate
- Successfully tested in a two detector setup
  - 2xHBU + 2xEBU
- It could be used for the other calorimeters

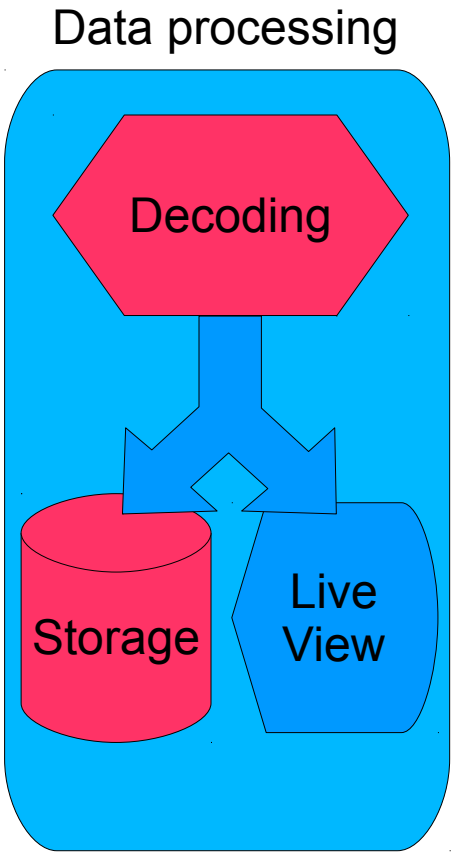


A track in 5 layers at test beam


HCAL+ECAL

Scalability Considerations

- Readout rate of ~9Hz (all memories full)
- Seems not to scale with number of layers up to now
- Different components need to be tested in larger setups with more layers/HBUs
- Decoding is the bottle-neck
  - Depends on the computing power of the PC
  - In previous tests each layer used one core
- Having more layers/HBUs will slow down the system
  - Unless computing power is increased
- Decoding on one of the FPGAs could be a better solution
  - DIF FPGA or LDA FPGA?



Next Steps and Summary

Next steps

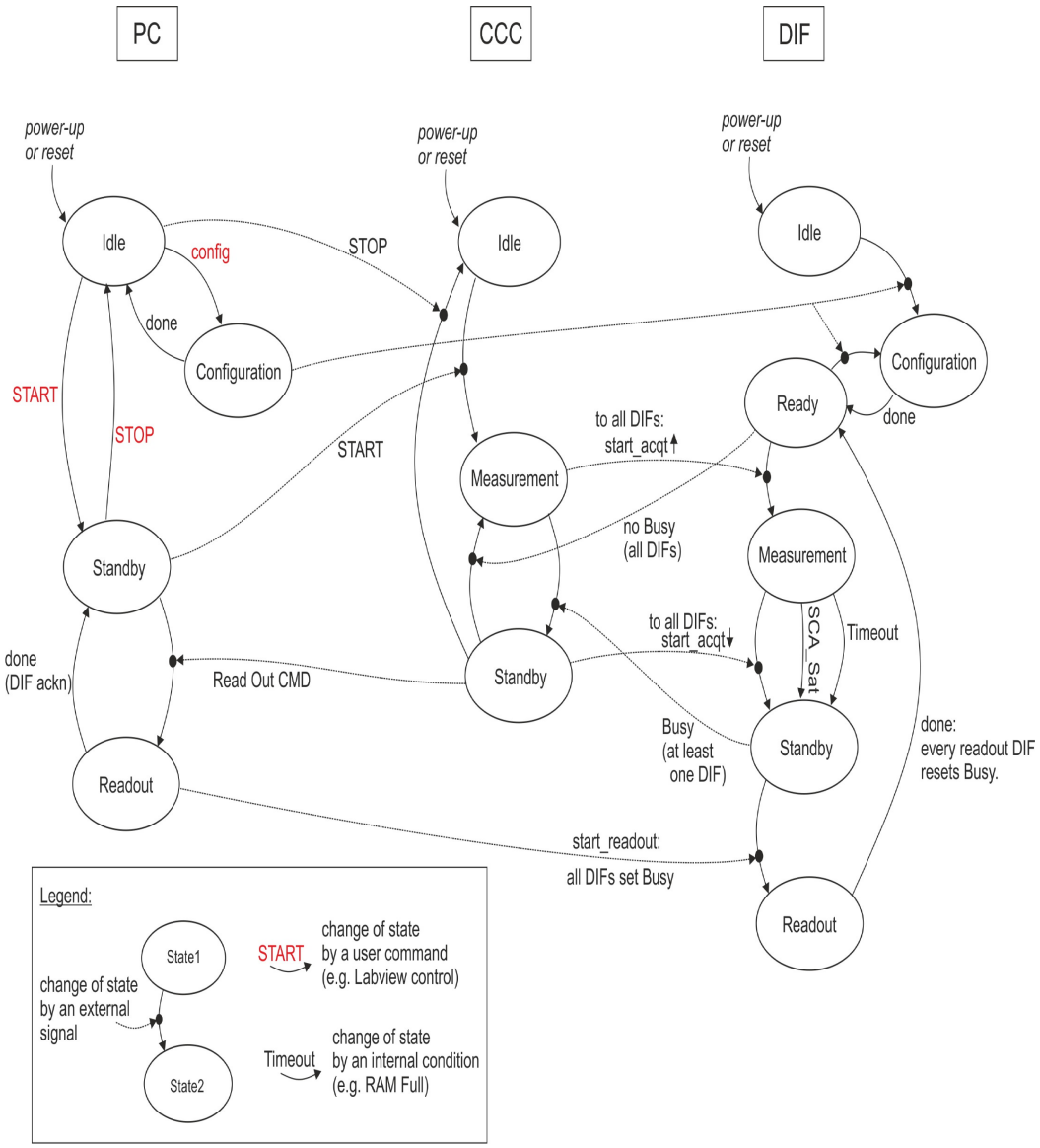
- Full implementation of the Mini-LDA
- Finalizing the Wing-LDA
- Testing an optimization of the full DAQ in different setups
- Scalability considerations

Summary

- DAQ system for scintillator calorimeters is under development
- Main DAQ software is improved and tested
- CCC is tested and in operation
- LDA is under development
- Current version of the DAQ was tested successfully in a multi calorimeter setup

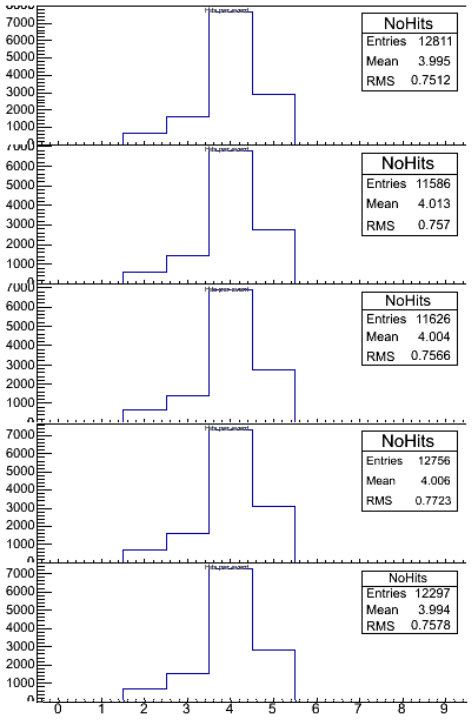
Backup

State Diagram

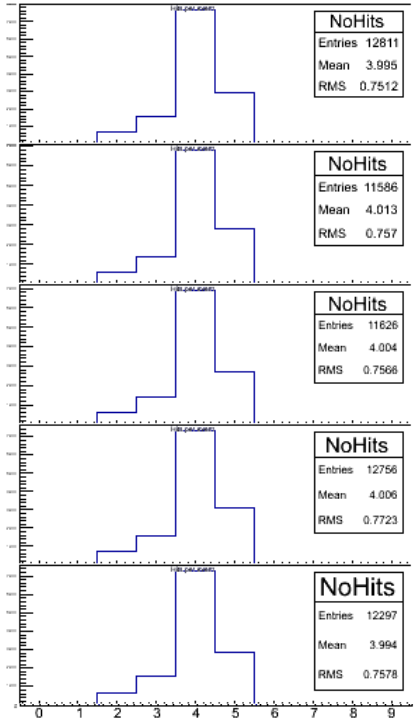


Multilayer Synchronicity

- During July test beam synchronicity was tested
- For the same run, number of hits was checked in two different event builders
  - Accepting only the same bunch crossing IDs
  - Accepting bunch crossing IDs +/- 1
- Absolutely no difference is observed



Same BunchX ID



BunchX ID +/- 1

- We have a true synchronous detector