A Consideration of Combined DAQ for hybrid ECAL

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CALICE DAQ

According to

https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ

The CALICE DAQ is supposed to be generic and quite independent of the underlying detector technology.

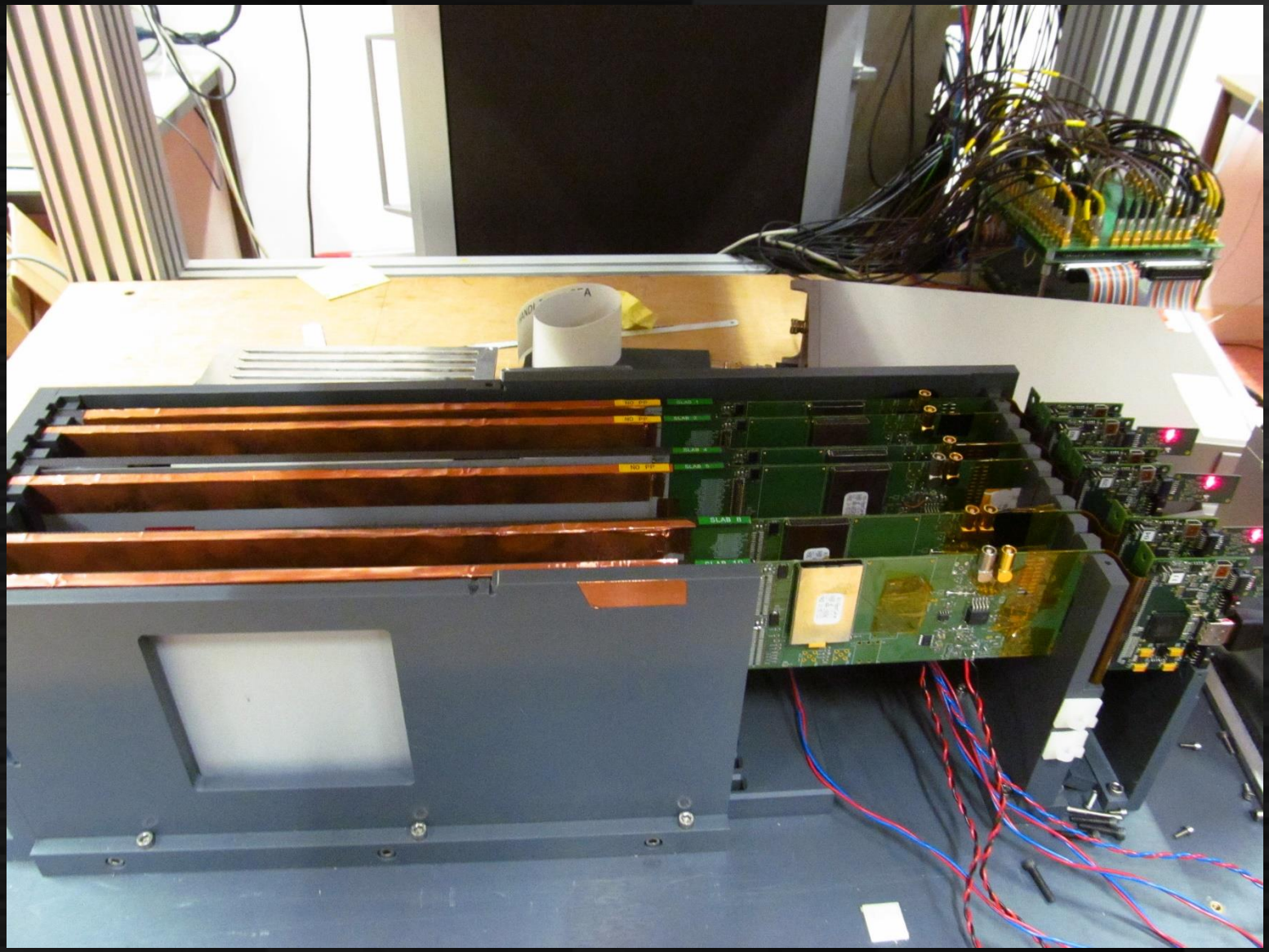
But currently we use independent DAQ systems in

- Si ECAL
- Sc ECAL / AHCAL
- SDHCAL
- DHCAL
- Others?

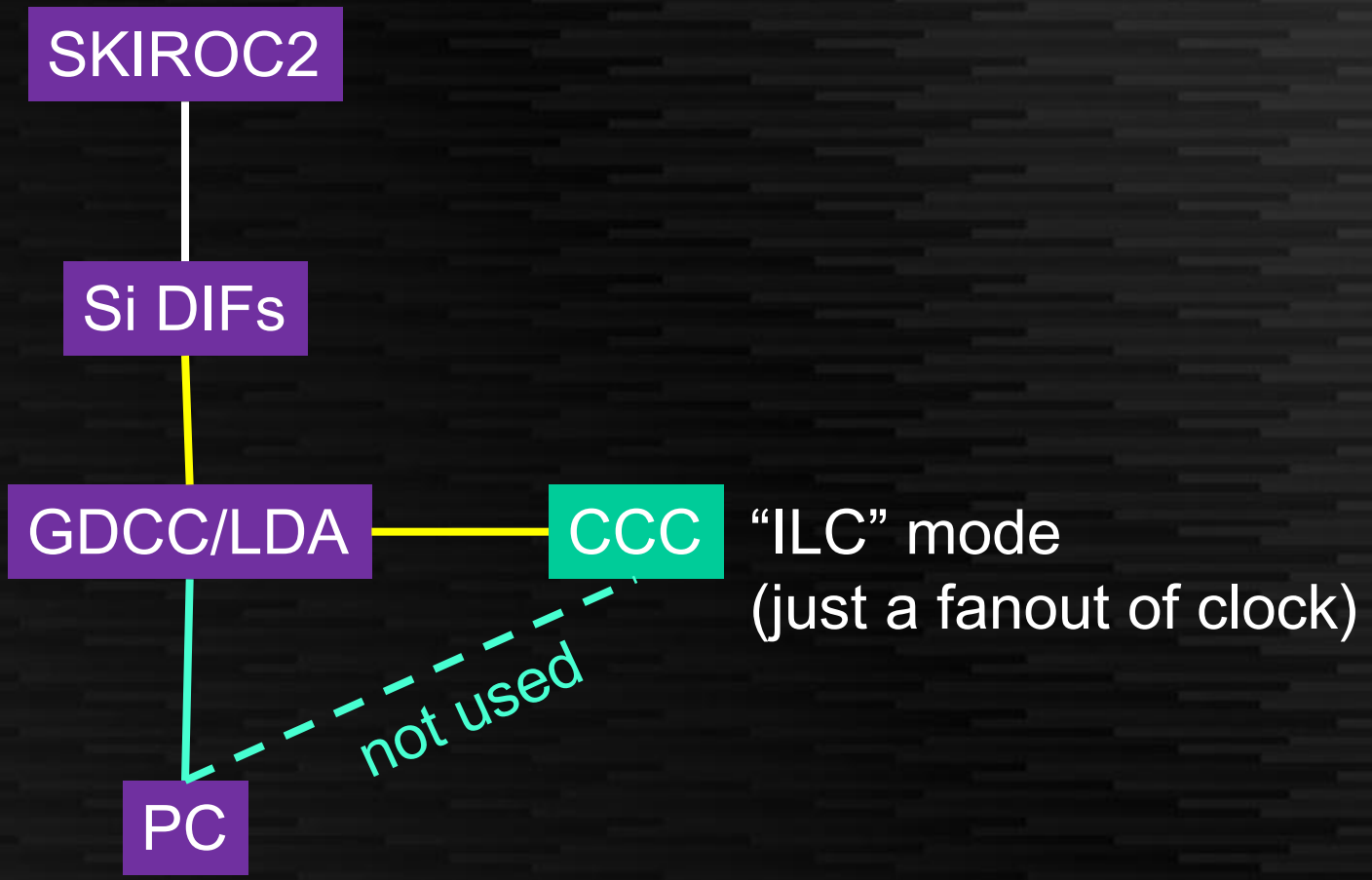
Our motivation

- Hybrid ECAL
  - We are considering hybrid (Si+Sc) ECAL as an option of good balance for cost and robustness
  - We are considering to perform a combined beam test for some time in this or next year
  - We'd like to combine DAQ of SiECAL and ScECAL to run synchronously and to get an easy-to-combine output
- In addition, I think ILD should gain from combined DAQ to reduce overall efforts
  since ROC chips are very similar for all systems.

SiECAL slabs (FEV8) in LLR

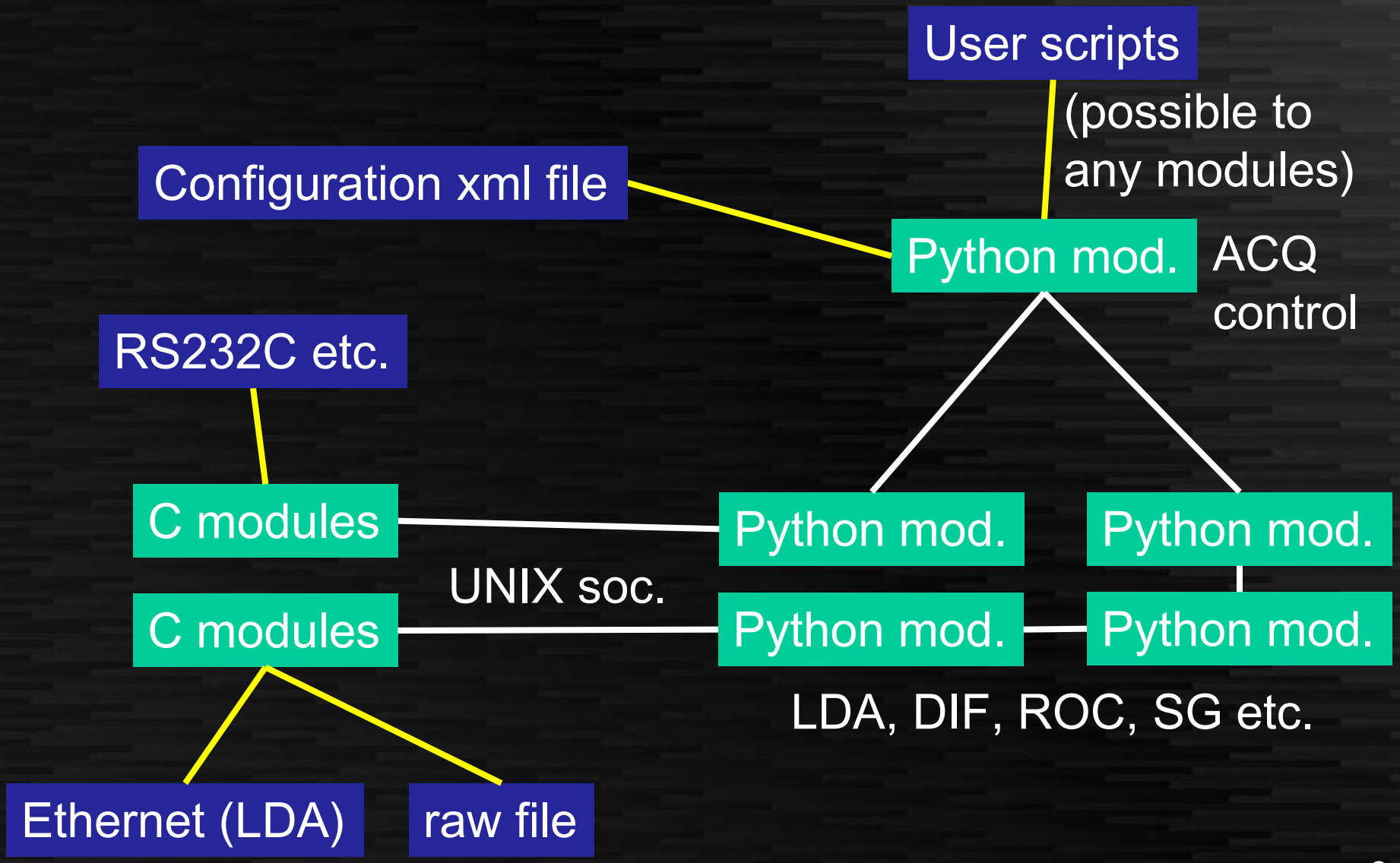


Si-ECAL DAQ

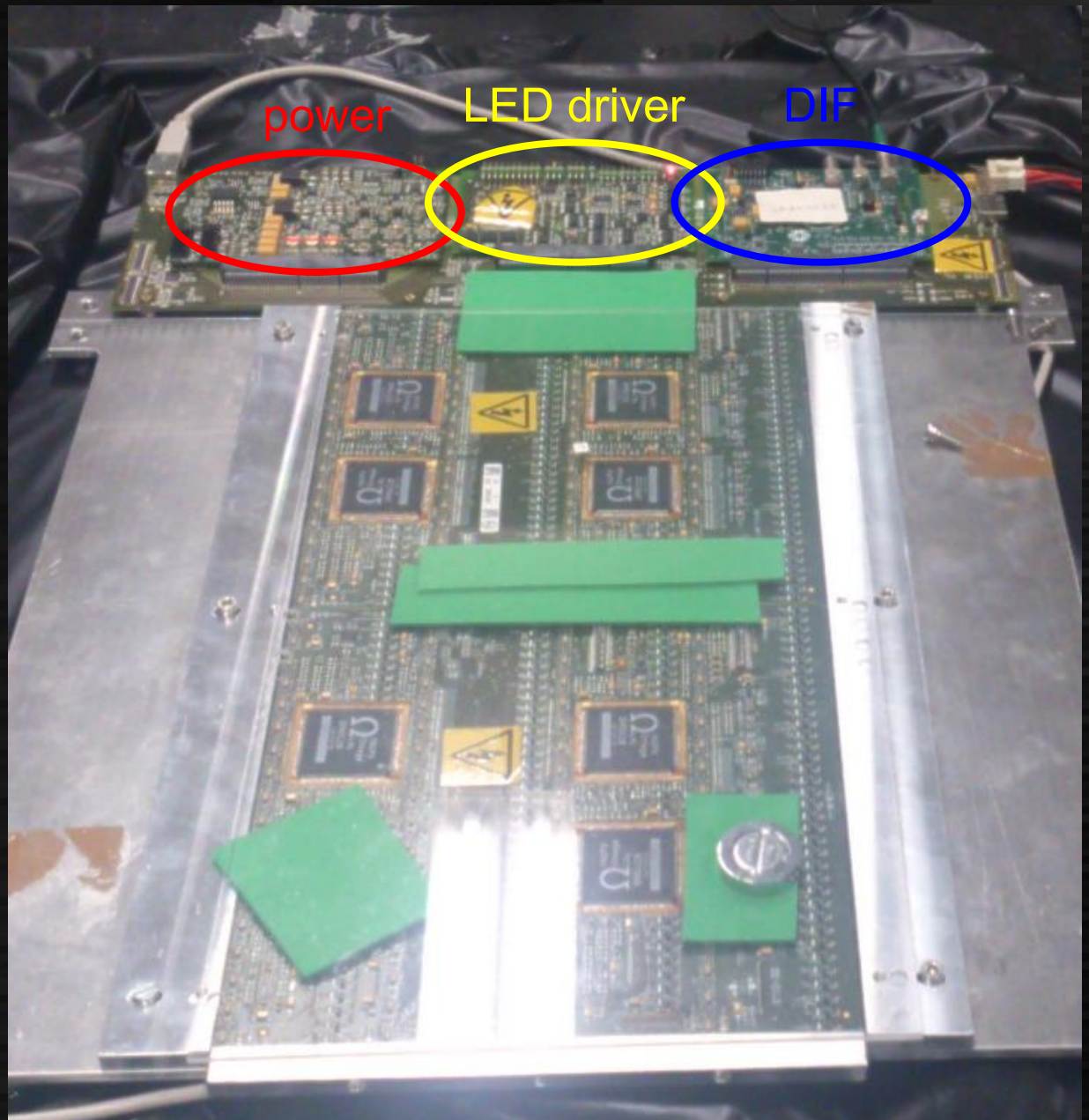


HDMI connetion
Ethernet connection

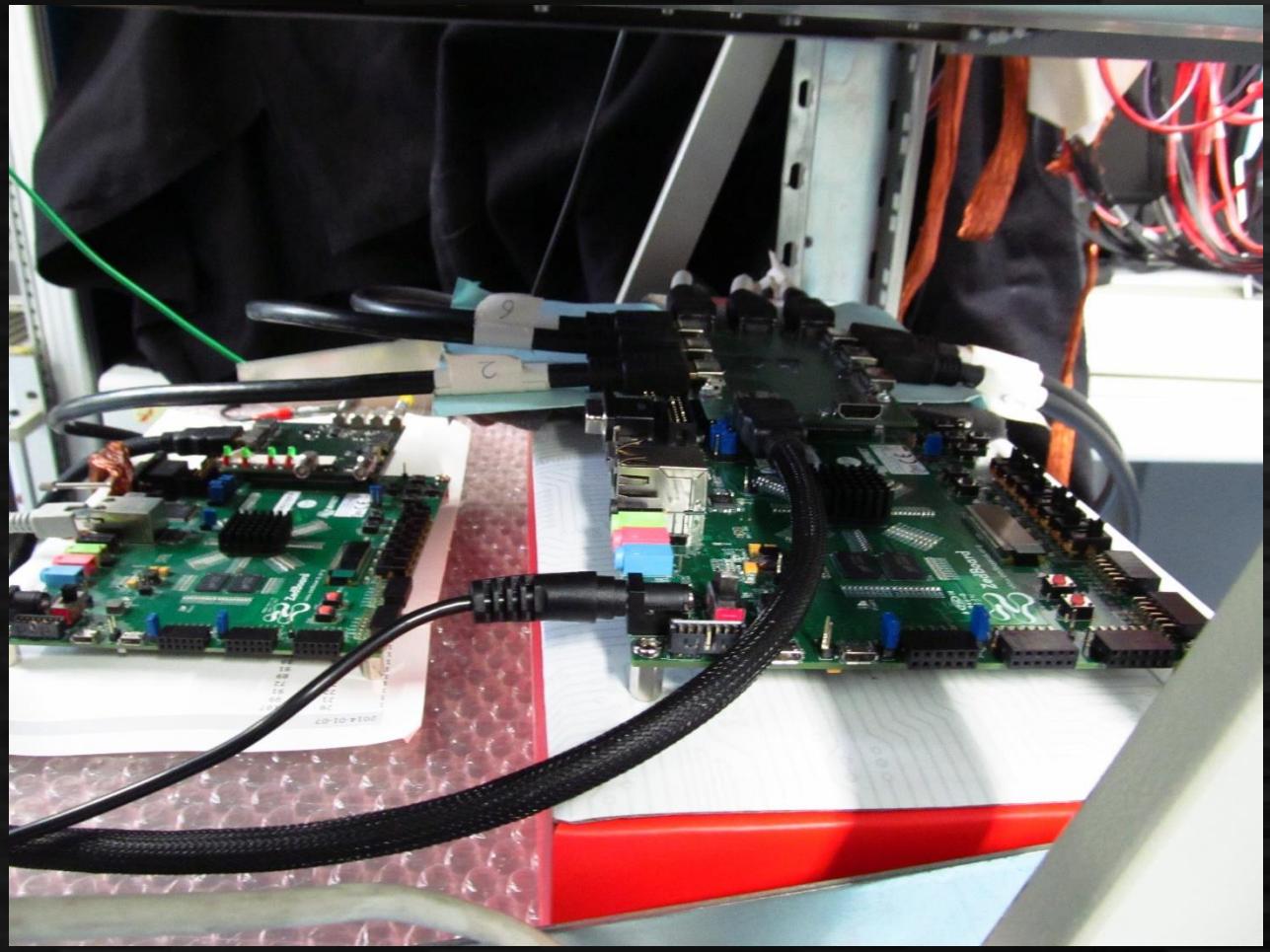
calicoes


User scripts
(possible to any modules)
Configuration xml file
Python mod.
ACQ control
RS232C etc.
C modules
Python mod.
Python mod.
UNIX soc.
C modules
Python mod.
Python mod.
LDA, DIF, ROC, SG etc.
Ethernet (LDA)
raw file

Sc-ECAL slab (EBU) in Shinshu

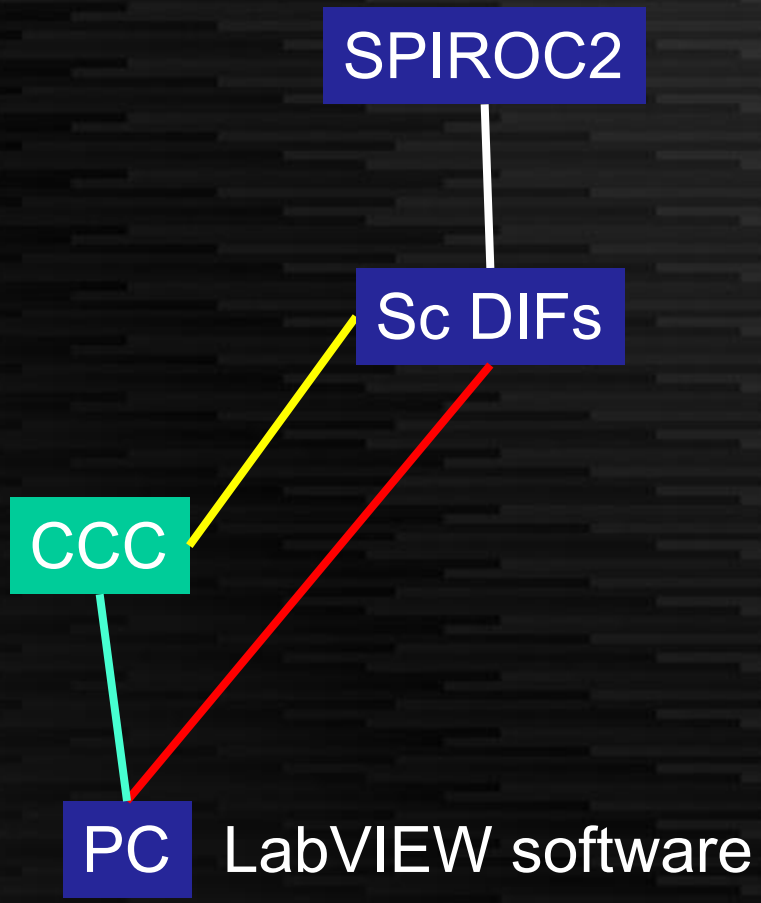


New CCC/xLDA in DESY



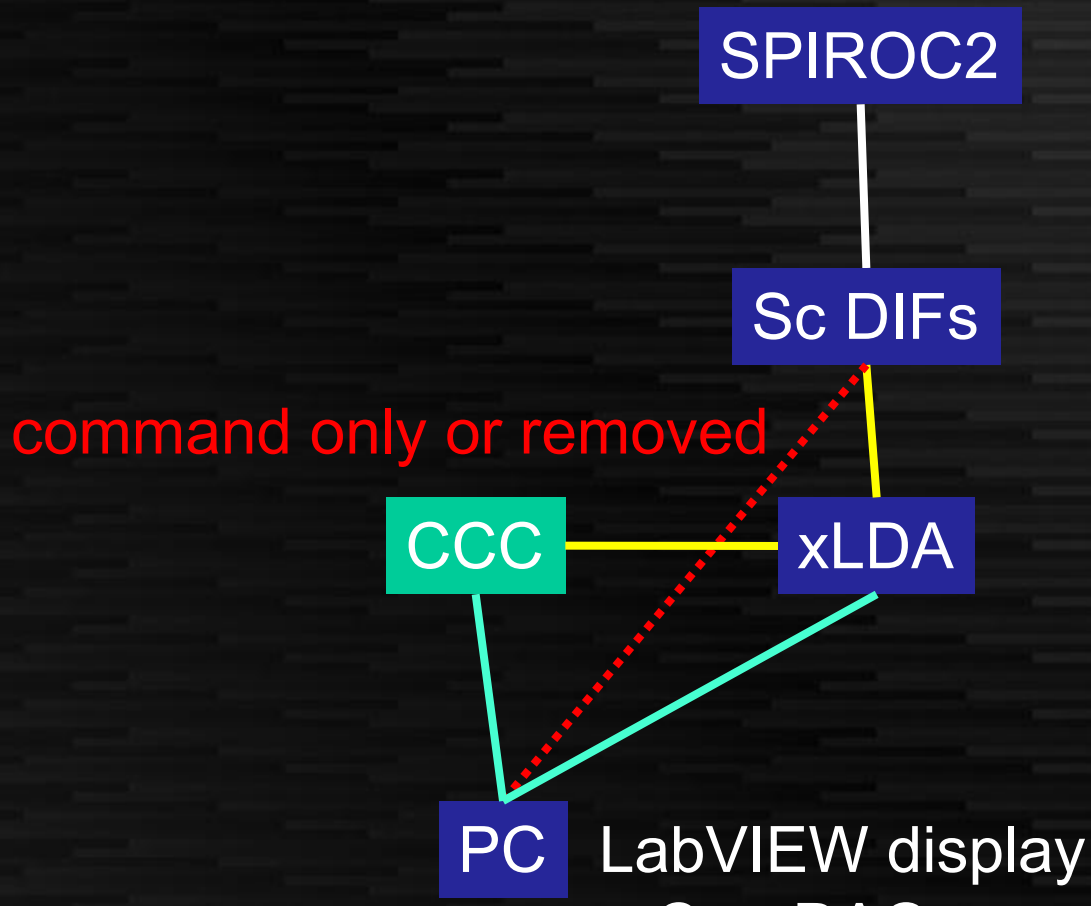
still under development

Sc-ECAL/AHCAL DAQ



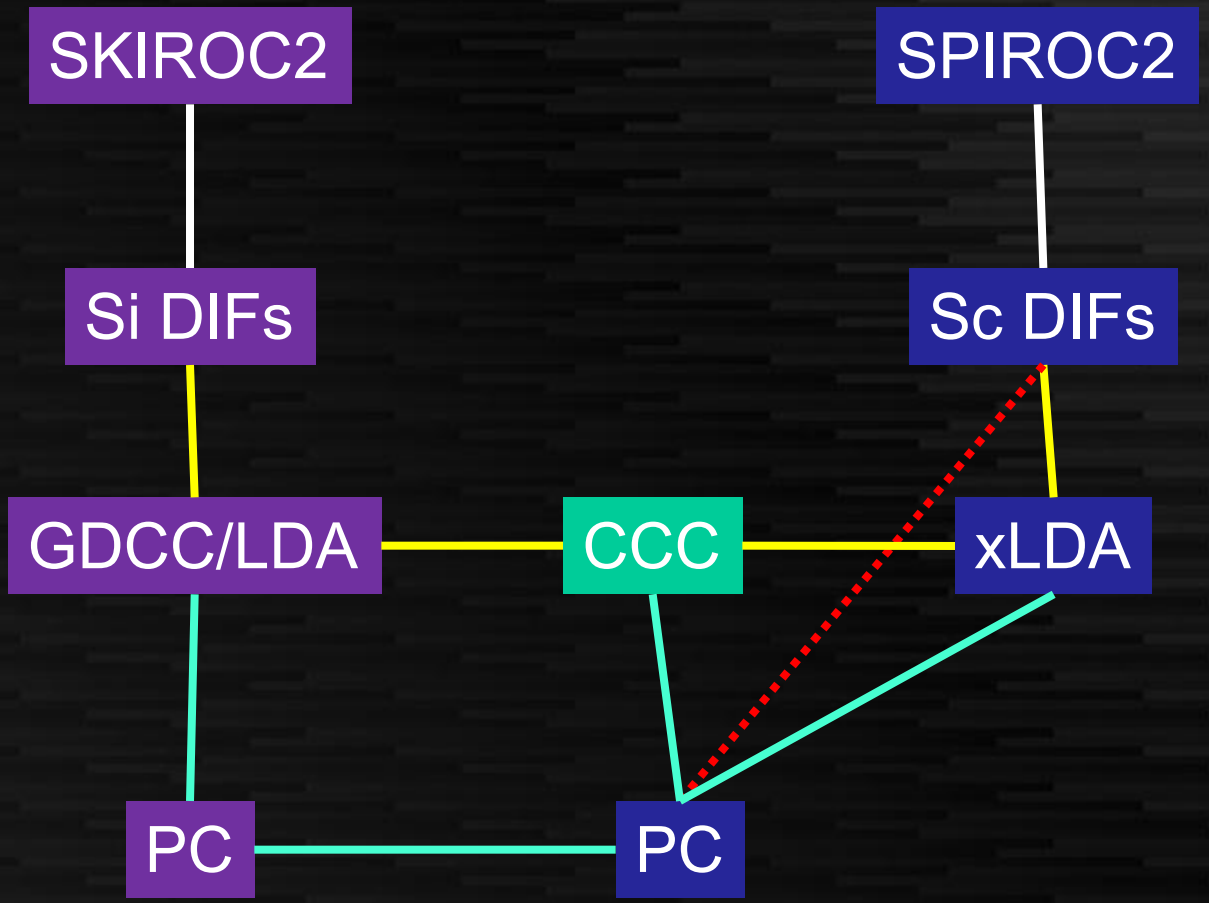
HDMI connetion
Ethernet connection
USB connection

Sc-ECAL/AHCAL DAQ (planned)



HDMI connetion
Ethernet connection
USB connection

Combined DAQ?



HDMI connetion
Ethernet connection
USB connection

CCC is at least common!

Some issues on CCC

- BUSY treatment
  - BUSY = clock (or oscillating) in Si-ECAL
  - BUSY = just a level in Sc
  - Possible to treat by “two-mode” CCC
- Ramp-up time (in power-pulsing)
  - May be different in Si and Sc
  - “Pre-spill” preferred – or fixed wait?
- BX tagging
  - Common problem – reliability of timing of FAST command

CCC: three modes

1. “test beam” mode
   - start_acq → wait busy → stop_acq → wait busy cleared → start_acq
2. “ILC” mode
   - start_acq → wait fixed time → stop_acq → wait fixed time → start_acq
   - Start/stop of run is still controlled by CCC
3. “just a fanout” operation
   - Same cycle as 2
   - No run control: just passing through spills

CCC I/O of HDMI

- Digital lines (3+2 pairs in HDMI)
  - Clock, ExTrig, commands CCC→LDA
  - Busy, (commands) LDA→CCC
- Commands
  - Start_acq (SPILL)
  - Stop_acq

- New CCC from DESY/Mainz for all?

LDA/GDCC/xLDA

- Claimed that “function is the same”
- Possibly exchangeable, maybe not
  - Maybe not needed
  - Easier if exchangeable
- Output connection to PC not compatible
  - TCP/UDP/raw ethernet
  - format of data

Software: options

1. Independent software
   - The way which I do not want to go
     - just keep at a backup option
   - At least run info should be communicated
2. Unified software
   - Calicoes/LLR
   - LabVIEW/DESY
   - xDAQ (CMS/SDHCAL)
   - AIDA EUDAQ (just heard from Vincent today)
   - others/completely new

Comparison in my opinion

DAQ	Advantages	Disadvantages
Calicoes	SiECAL implemented Simple & easy	Lower maintenance level Not public GUI not implemented
LabVIEW	Sc implemented Easy to implement GUI	Slow Difficult to read/maintain codes
xDAQ	Maintained by CERN/CMS public framework Many features C++ based (for me: easiest)	A little complicated Have to learn the framework
AIDA EUDAQ	Simpler than xDAQ C++ based LCIO output?	No implementation for CALICE now?
new	Completely free	Maximum effort needed

Will consider xDAQ and AIDA

Support (I mean, just a code sharing) from SDHCAL possible for xDAQ?

Consideration on unified software

- Connectivity to calicoes
- Connectivity to LabVIEW configuration and data display for Sc system

- Maybe have own GUI
  - Focused on DAQ control and display, not for making detailed ASIC configuration files
    - each already has a script for the configuration

Summary

- With some consideration, hardware can be interoperated
- For software, I'll investigate xDAQ & AIDA

- Plan to be available later in this year
  - software will be public
- Any cooperation is highly welcome