DAQ system and LDA for the AHCal

Julien Caudron, Johannes-Gutenberg Universität Mainz
ETAP

JGU Mainz: Bruno Bauss, Volker Büscher, Phi Chau, Reinhold Degele, Karl Heinz Geib, Sascha Krause, Yong Liu, Lucia Masetti, Uli Schäfer, Rouven Spreckels, Stefan Tapprogge, Rainer Wanke

In collaboration with DESY (Aliakbar Ebrahimi, Oskar Hartbrich, Katja Krüger, Mathias Reinecke, Felix Sefkow)

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Overview

1) DAQ Design

2) PC software

3) Clock and Control Card

4) Link and Data Aggregation :

- Mini-LDA (10 layers solution)
- Wing-LDA (design integrated to the HCal)

5) Future plans

DAQ Design

DAQ in constant progression

1) PC Software

Based on LabView

Multi Layer support

USB for slow control and data

2) CCC

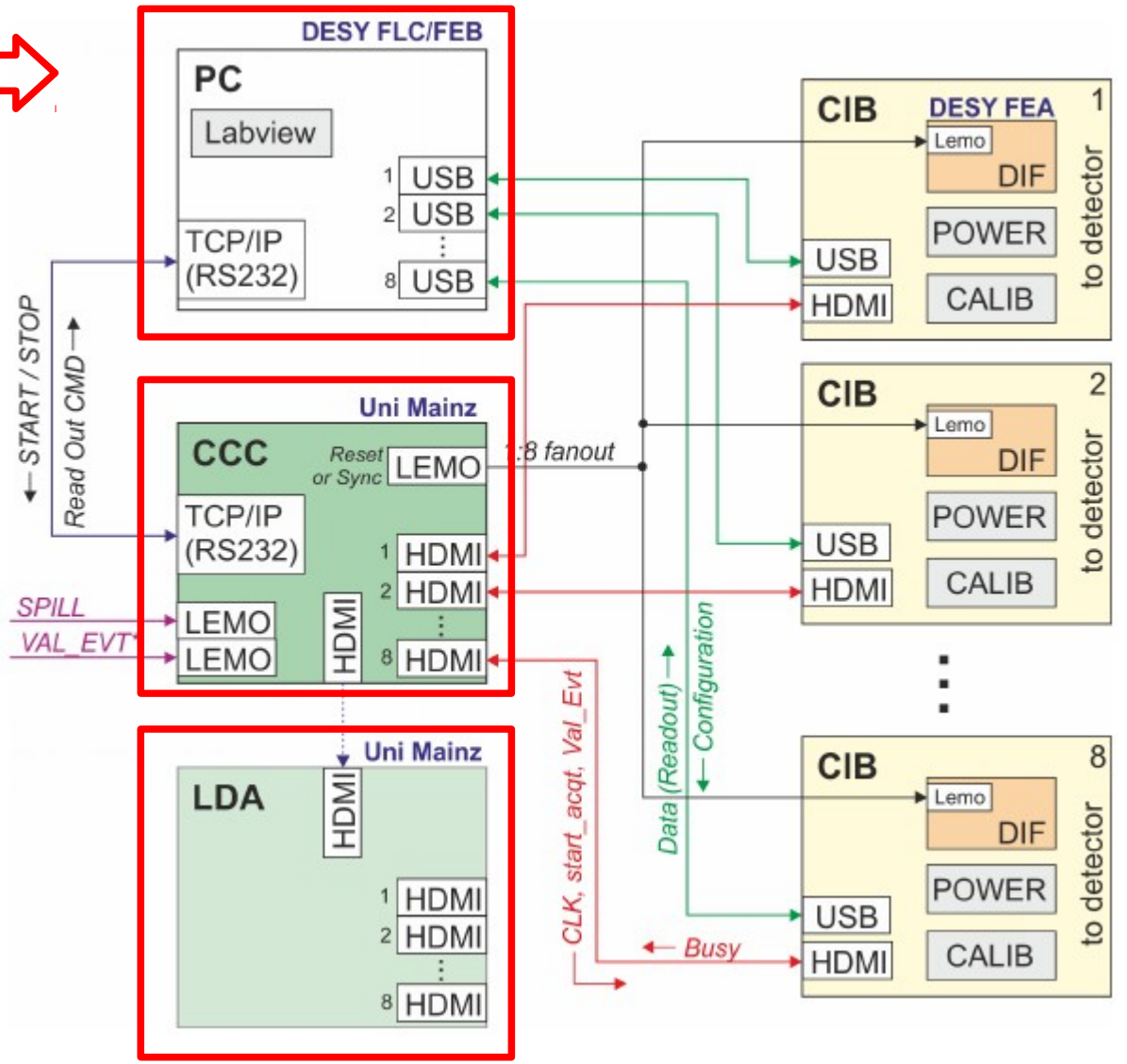
ZedBoard + Mezzanine

HDMI for fast signals

3) LDA

Integration in progress

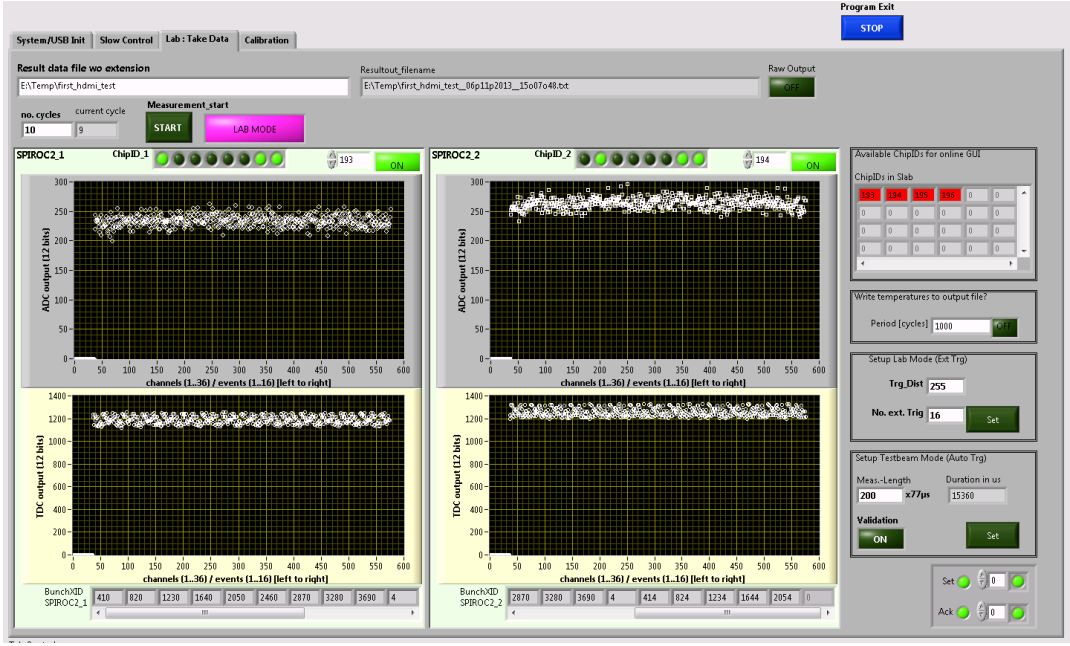
Mini-LDA as transition step

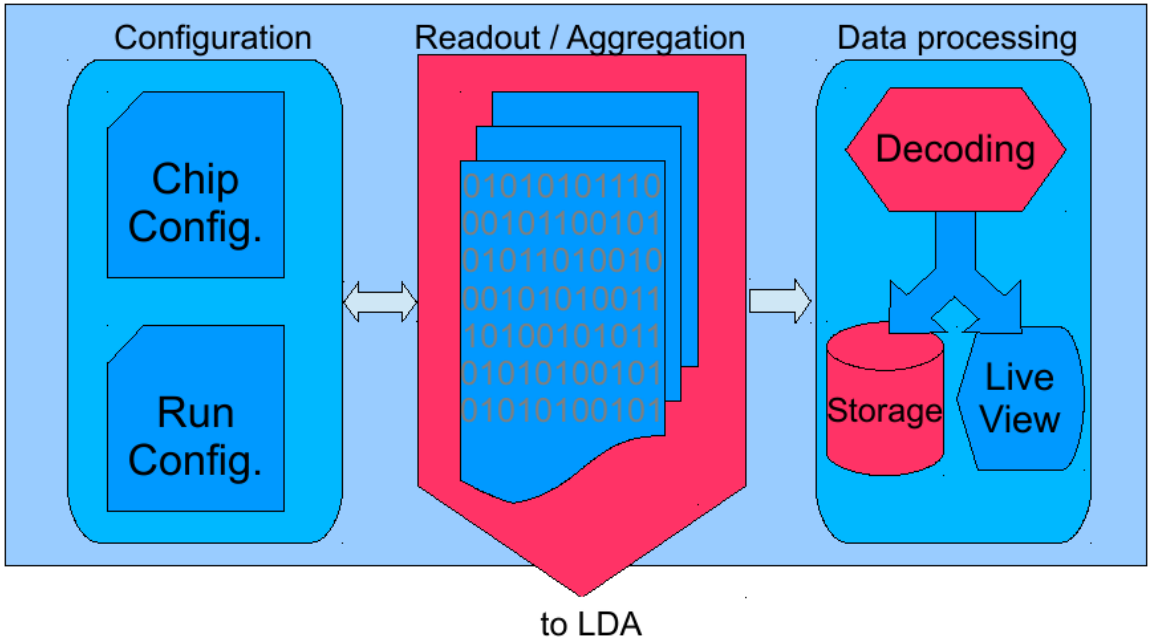


DAQ PC

- Currently using LabView:
  - adaptation of previous software
  - easy modifications
  - interface and live monitoring
  - already intensively tested
- Some tasks done in C++ lib
- Modular and Multithreaded
- Readout / data aggregation

  (Future: data aggregation done by LDA)
- Development of C++ lib to replace LabView decoding
  - Faster
  - LCIO output





DAQ PC

DAQ system with several layers has been tested

(without LDA: the CCC was using a fan-out)

Even if it is an intermediate design and that more development is needed for more layers / more HBUs:

- Readout rate of ~9 Hz (all memory full)
- It seems not to scale with the number of layers
- Bottleneck: decoding

  It depends of the computing power of the PC

  In previous tests, each layer used one core

A solution can be to do the decoding on one of the FPGA:

DIF FPGA or in LDA FPGA

investigation in progress

ZedBoard

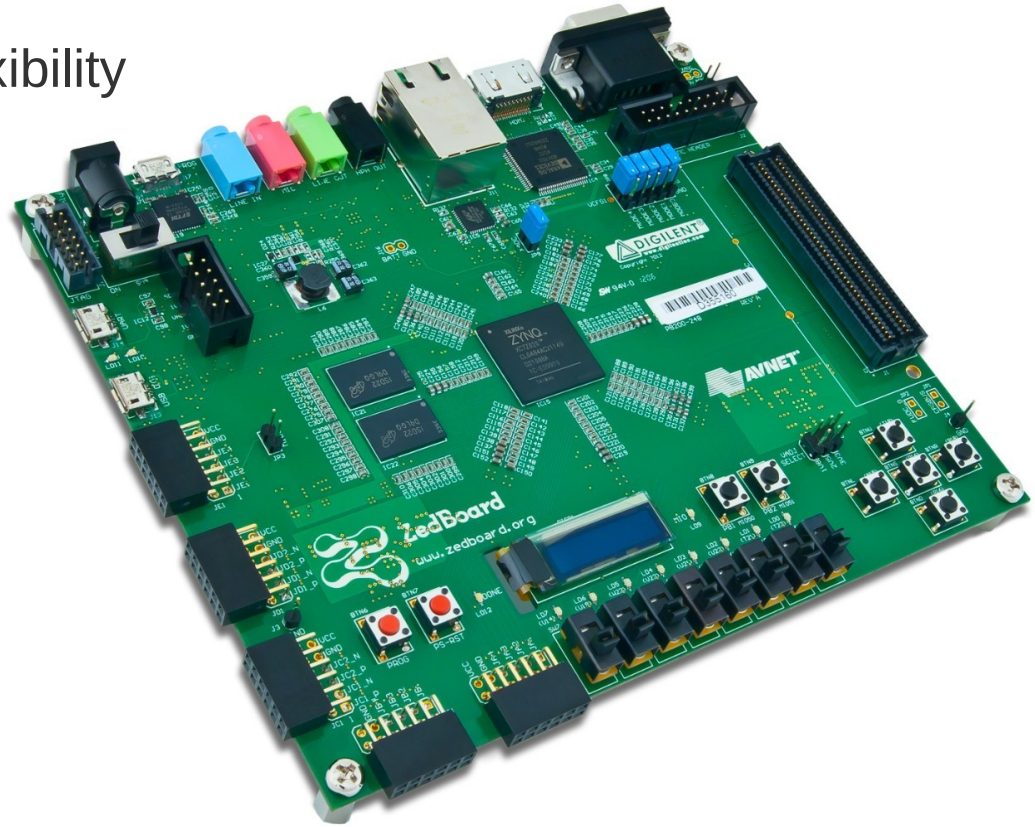
Zynq Evaluation & Development Board progression

used for CCC, Mini-LDA, Wing-LDA first tests

- Xilinx Zynq-7000 SoC
  - PS (processor subsystem): Dual ARM Cortex-A9
  - PL (programmable logic): Xilinx 7 series FPGA
  - 100 Gbps interconnect bandwidth
  - ARM programmability + FPGA flexibility
- On board memory:

  512 MB DDR3
  + 256 MB QUAD-SPI
- PS run on Linux
- FPGA Mezzanine Connector

  to adapt the ZedBoard to several usage

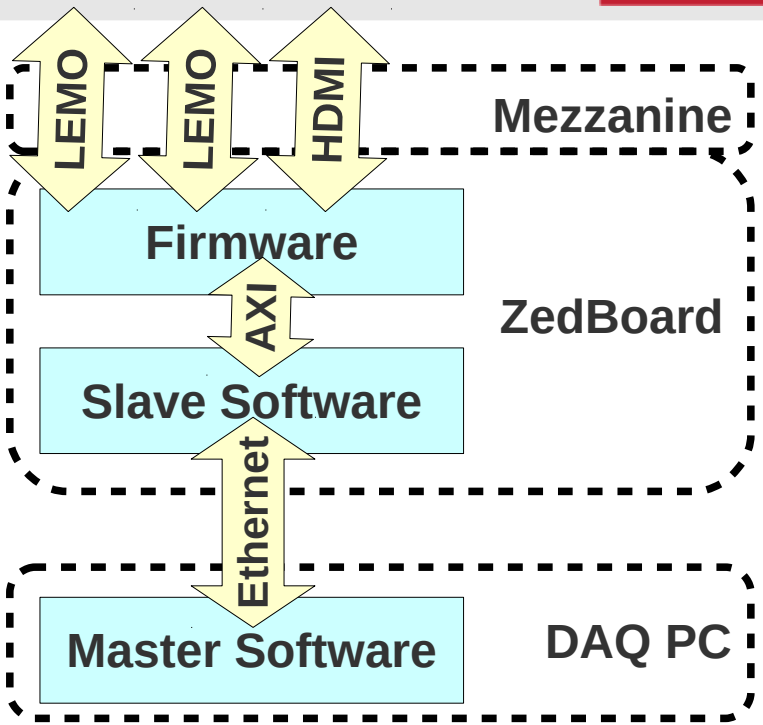


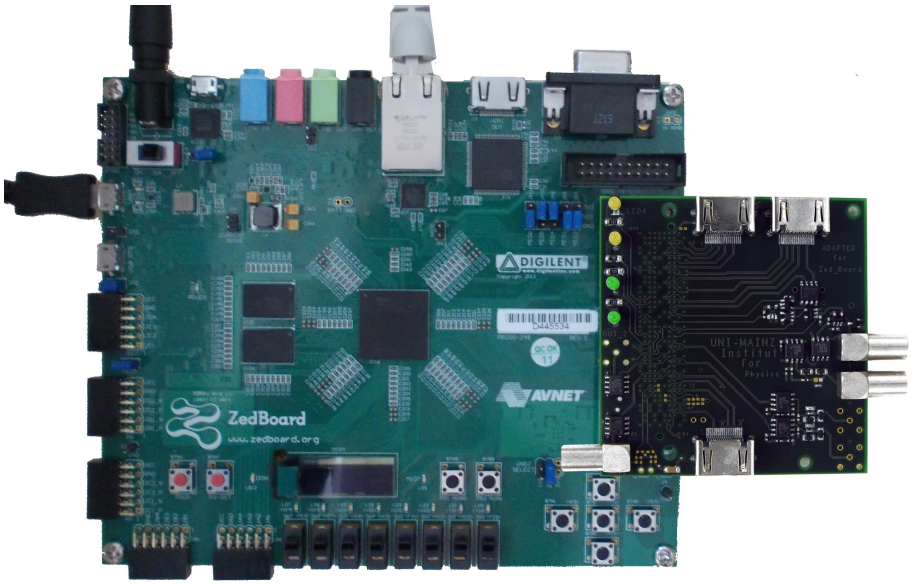
DAQ CCC

Based on ZedBoard + Mezzanine

1) Firmware on PL
2) Slave software running on PS
3) Master software running on DAQ PC

- Ethernet connection to DAQ PC
  - Start / Stop / Readout
- Several layer can be used
  - 8 layers can be used with 1:8 HDMI fan-out
- LEMO connections
  - Validation signal
  - Spill signal
  - Reset / Sync signal
- Has been used during several TestBeam
  - totally functional





LDA

Plan for the LDA:

- One layer DAQ without LDA

  done

- Multilayer DAQ without LDA

  done

- Multilayer DAQ with mini-LDA (transition solution, cf. next slide)

  first test with mini-LDA as fanout: done

  firmware / software in development ← We are here

- Multilayer DAQ with wing-LDA

  firmware / software adapted from mini-LDA

Development of the wing-LDA in parallel with mini-LDA:

Firmware / software easily adapted from one to the other

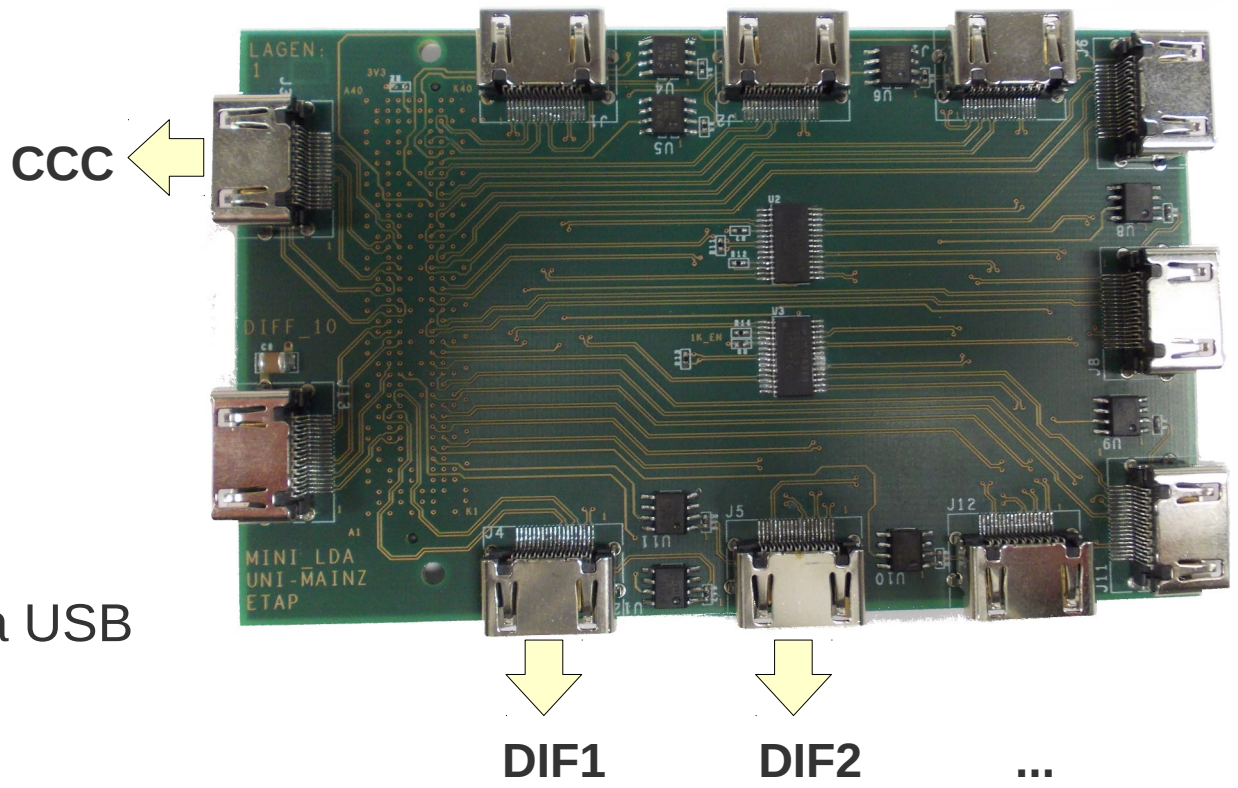
Mini LDA

Transition LDA:

1 ZedBoard + 1 mezzanine

with 1 HDMI to CCC
10 HDMI to DIF

Mini-LDA mezzanine:



As fan-out:

Tested in January

Only Firmware development
used to dispatch the fast signal
No data handling, slow-signals via USB

As LDA:

In development

Similar to CCC: Firmware (slow-controls + data handling)
+ Slave software (communication with the Master software on DAQ PC)

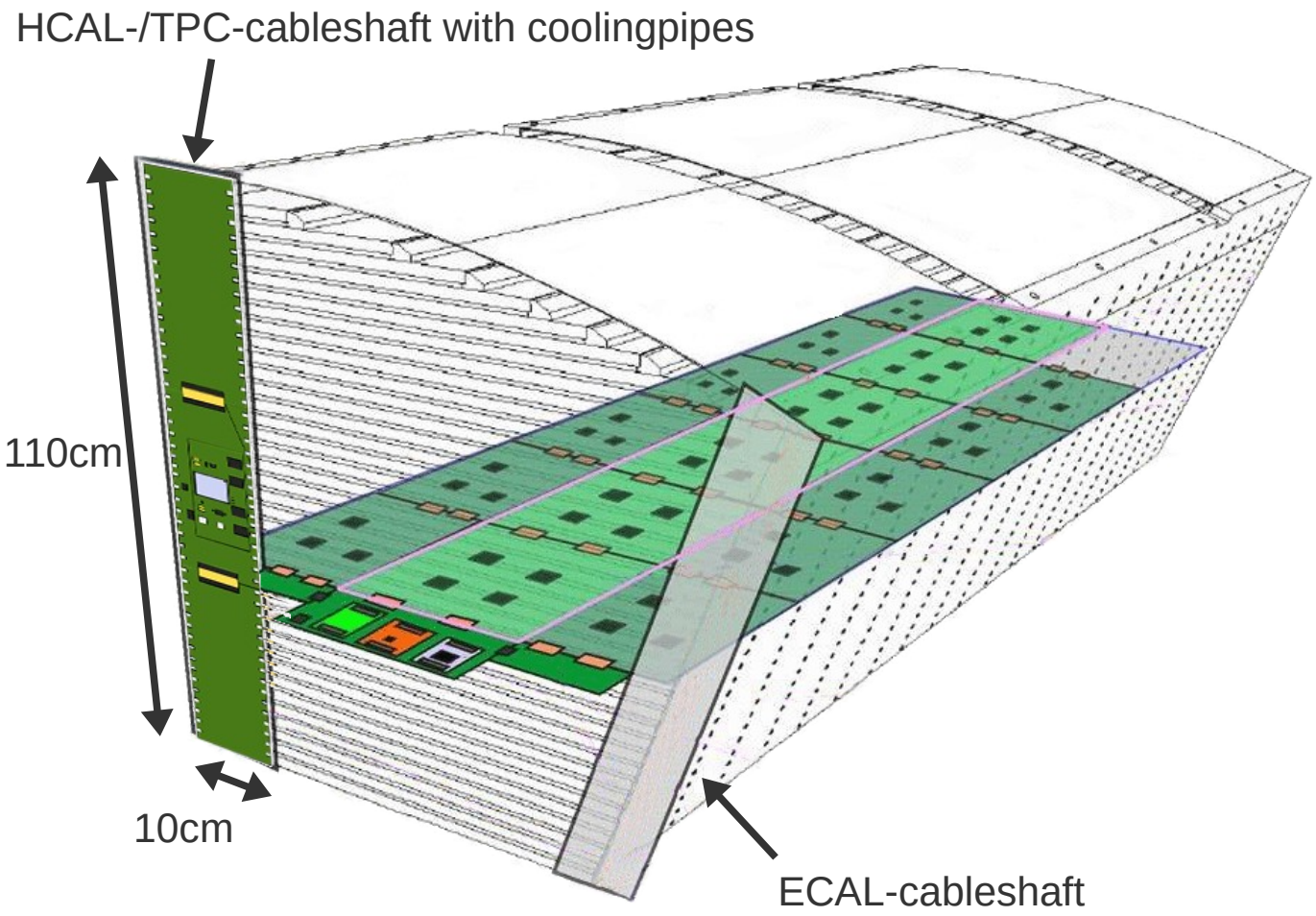
HDMI for fast-signals and data (and in a second step, slow-signals by HDMI also)

mini-LDA can also be used by ScECal

Wing LDA

Integration of the LDA in the HCAL:

in the 10x110cm cableshaft



Challenges:

- Outside the detector

  long PCB to avoid long cables

  timedelay between layers (up to 5ns) regulated with on-board electronic

- 48 layers

  smallest possible connectors

  → micro-HDMI

Wing LDA

Components:

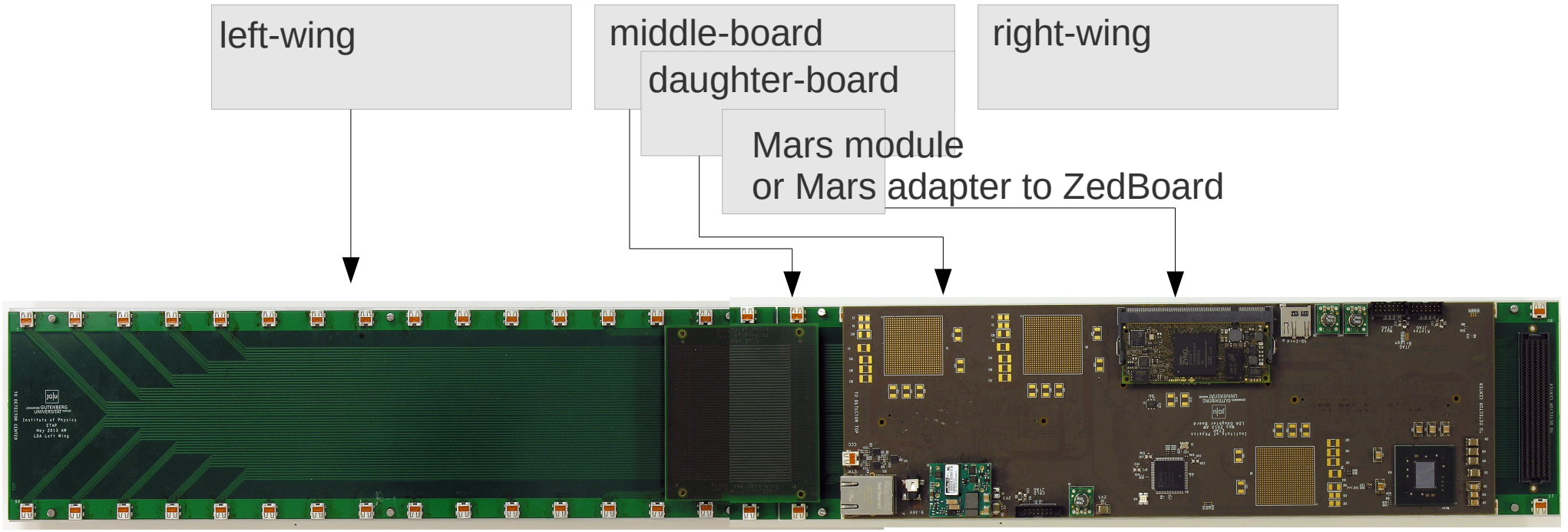
- 3 passive PCBs: left-wing, middle-board, right-wing

  total of 96 micro-HDMI connectors

  (linked by rigid-flex connections, not shown in the picture below)

- 1 daughter module: 4 Kintex FPGA +

  1 SoC: Mars module or adapter + ZedBoard



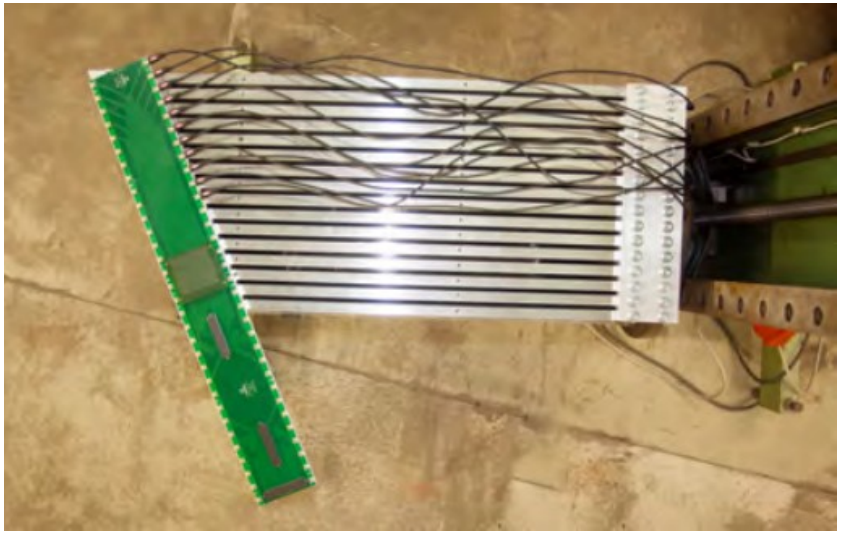
Wing LDA

Voltage and connectivity test:

Done at Desy in June 2013

Voltage problem found and corrected

Timedelay: on-board electronic not tested
measurements agree with simulations

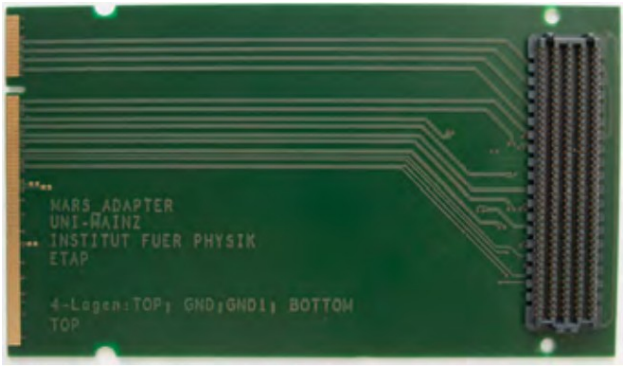


Currently:

- 1 Kintex FPGA soldered (24 DIFs)
- Difficulties with the Mars module prototype

  → adapter + ZedBoard
  (limited to 2 FPGA, i.e. 48 DIFs)
- Left-Wing can be used for tests with
  up to 24 layers

adapter:



Future Plan

- Firmware and software for LDA:

  controls signals handling

  data handling: to be finished in both the firmware and the software

- Move to full-HDMI connection:

  requires modifications on: DIF, LDA firmware, LDA software

- Scalability consideration:

  test components (DAQ PC software, ...) and explore solutions (decoding in FPGA)

- Global DAQ considerations:

  more robust system + run with SiECAL

  reflection on data transfer performance: AXI-GPIO vs. AXI-Stream

  working document in preparation

Conclusion

Current status:

- DIF on HBU: Heavily tested, functional
  Modification to move to full HDMI
- PC Software: Heavily tested and modular
  Tasks will be distributed between several PC
- CCC: Heavily tested, functional
  Fast command transfer and different run modes to be implemented
- LDA: First test of Mini-LDA as fan-out done successfully in January
  Data handling implementation in development
  Wing-LDA: needs minimum software/firmware adaptation from Mini-LDA

Next steps:

- Tests with different setup
- LDA development
- Global DAQ consideration