Building blocks 0.18 µm XFAB SOI

Calice Meeting - Argonne 2014

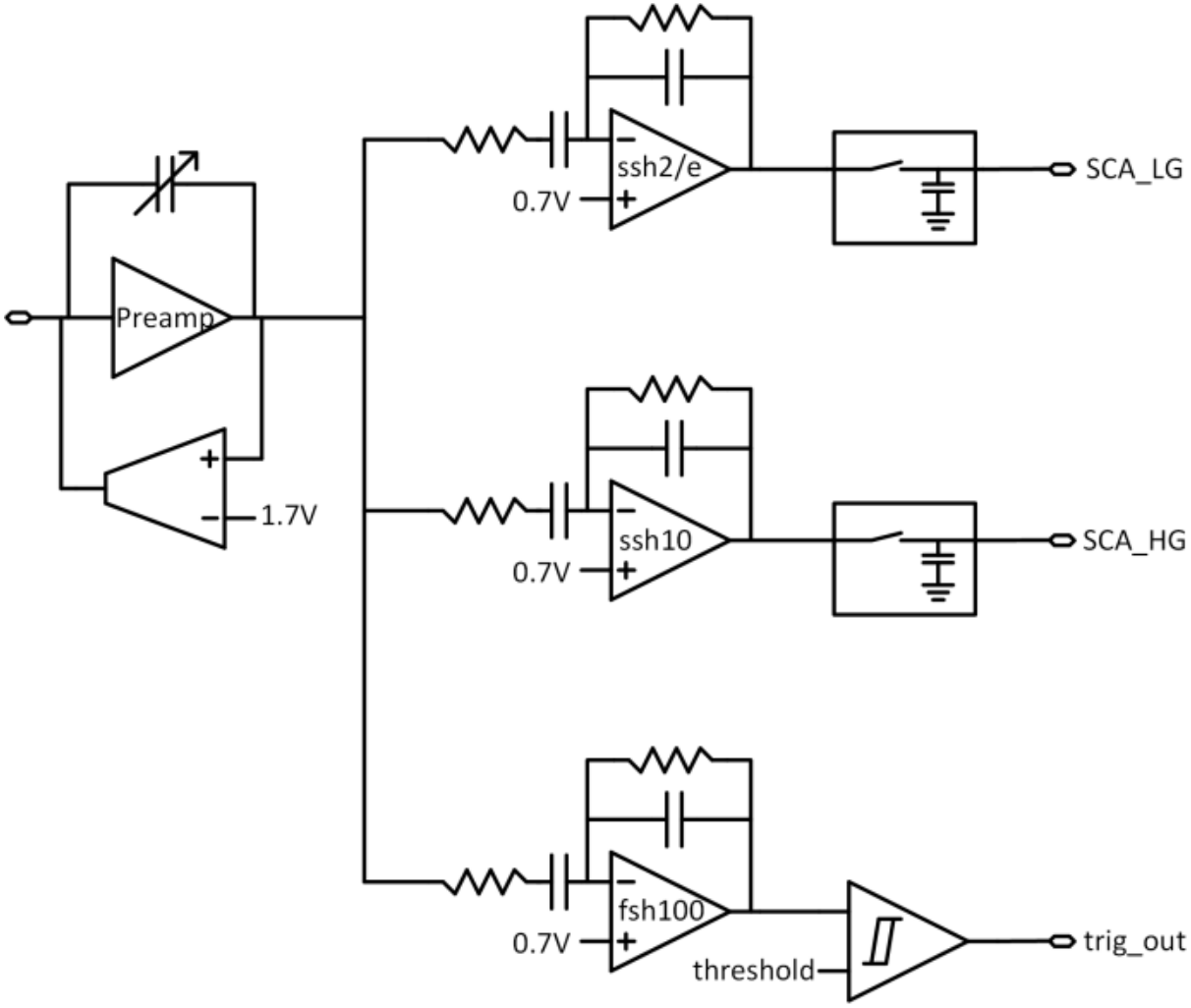
CALIIMAX-HEP

XFAB SOI 0.18 µm

- SOI Silicon On Insulator ;
- Recent technology (2011) ;
- Cheaper than the 0.35 µm AMS technology ;
- Better for digital electronics.

Disclaimer: The following is a study for building blocks in this technology, not a chip.

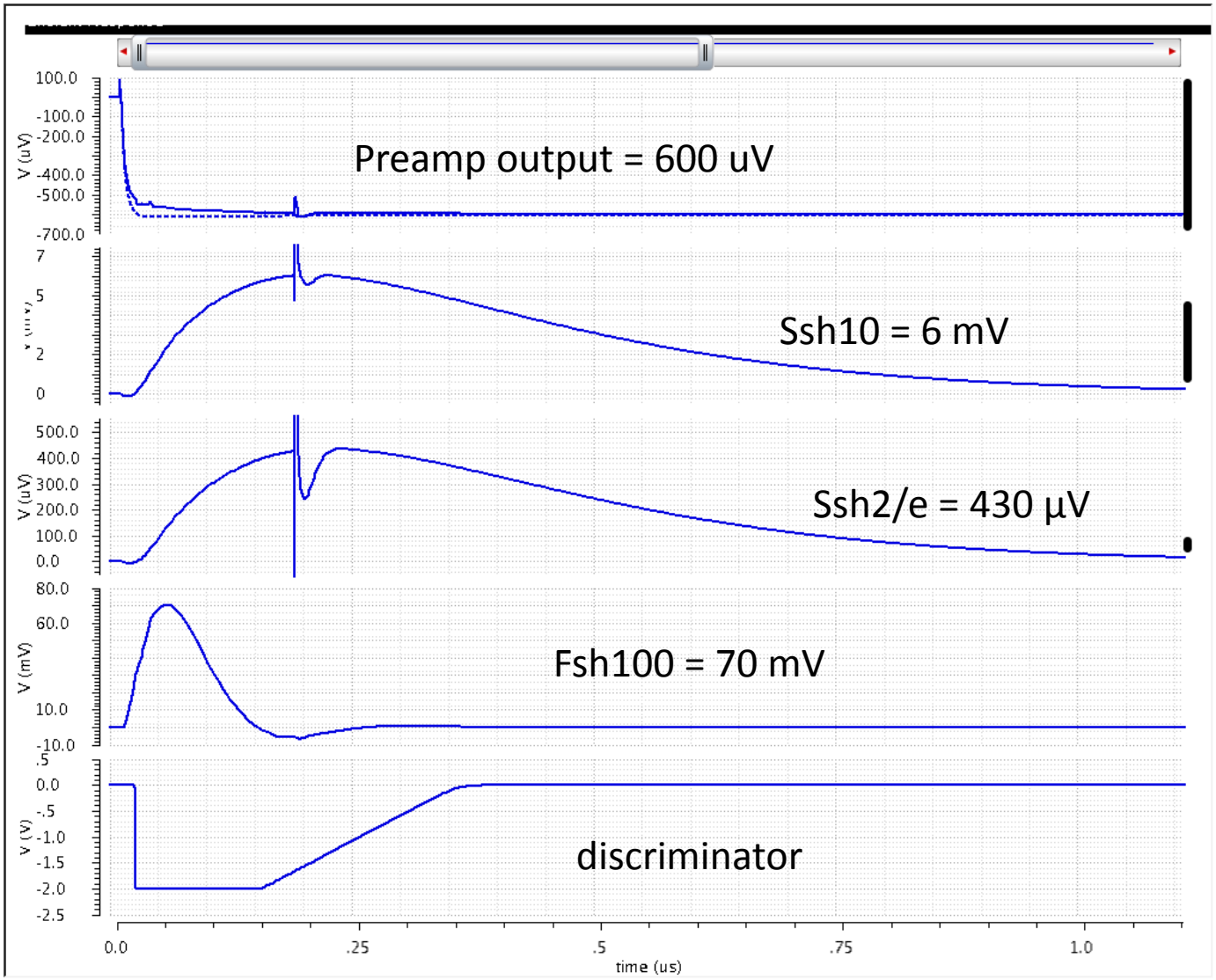
Simplified schematic



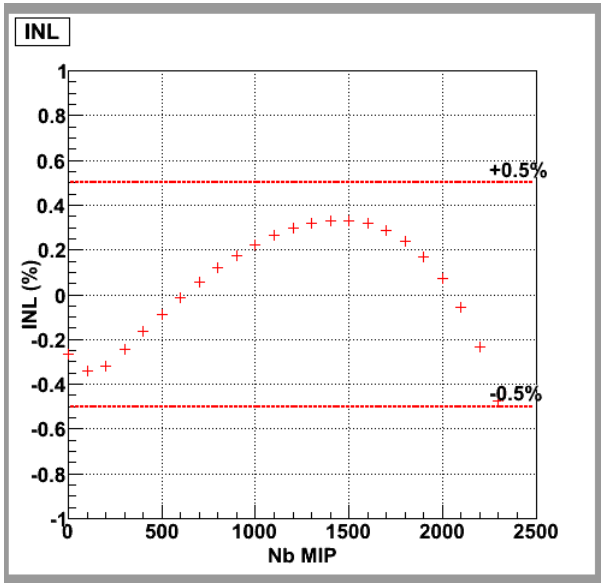
Specifications

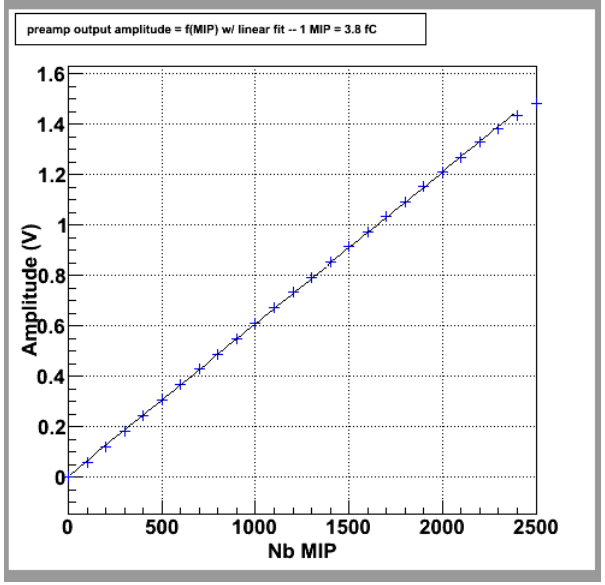
- Adjustable feedback capacitor from 500 fC to 7.5 pC ;
- Slow shapers' shaping time of 180 ns ;
- Fast shaper's shaping time of 30 ns ;
- 2 slow shapers: slow shaper high gain with a gain of 10, slow shaper low gain with a gain of 2/e (≈0.74) ;
- Fast shaper gain 100 ;
- No fancy adjustable parameters, the building blocks are as simple as it could be, there will be different versions of these ;
- For all the following simulations, the feedback capacitance had been chosen to be 6 pF.

Analog outputs – simulation results

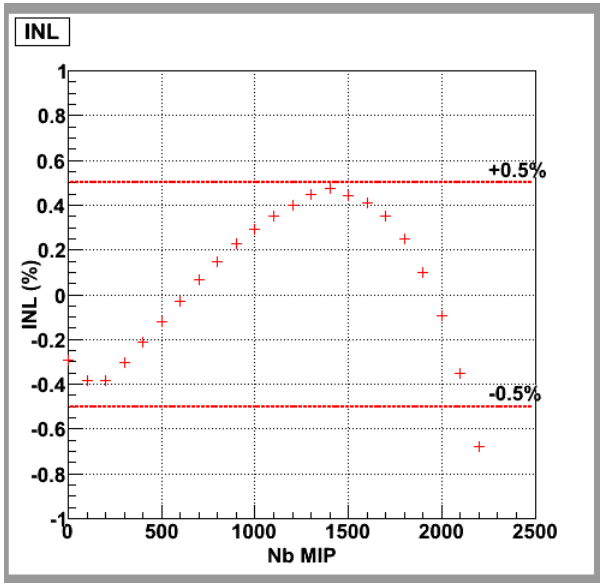


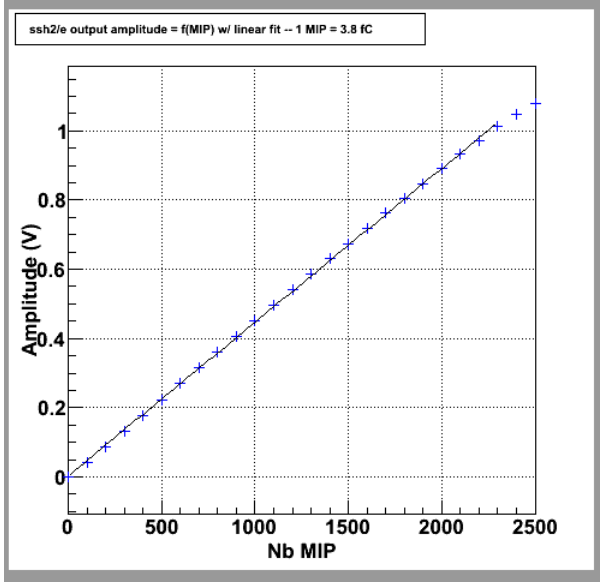
Linearity



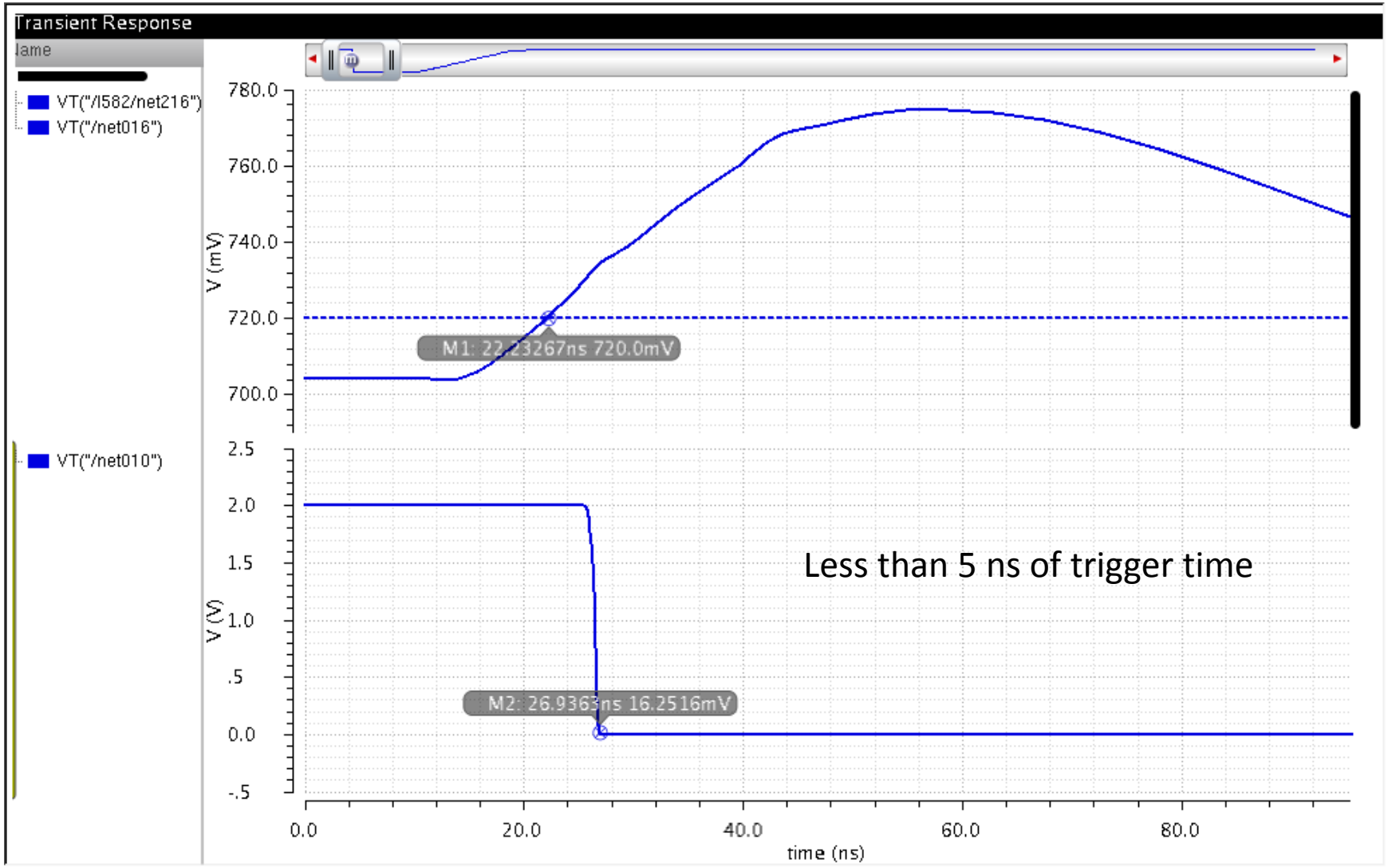


- 1% linearity up to 2300 MIP at preamplifier output and 2200 MIP at low gain slow shaper output.
- 1 MIP = 3.8 fC => 1% linearity up to 8.36 pC (with a 6 pF preamplifier feedback capacitance)

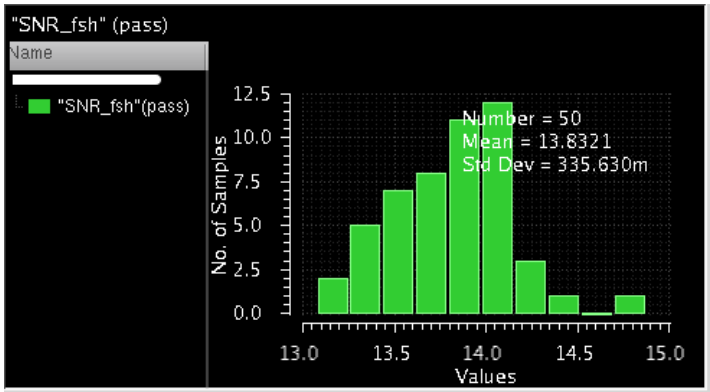


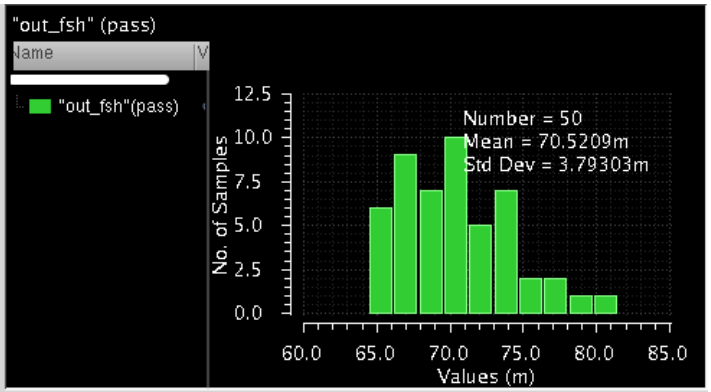


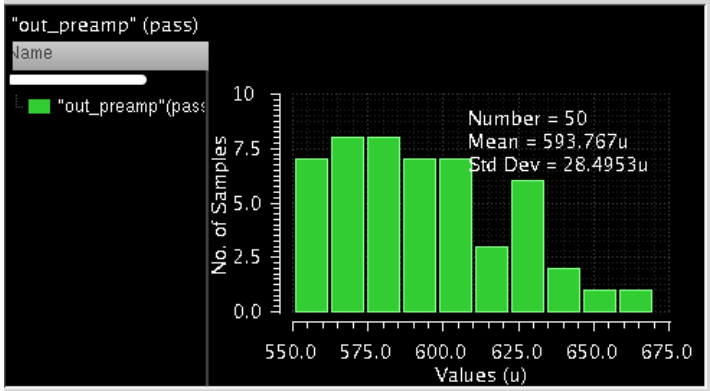
Discriminator efficiency

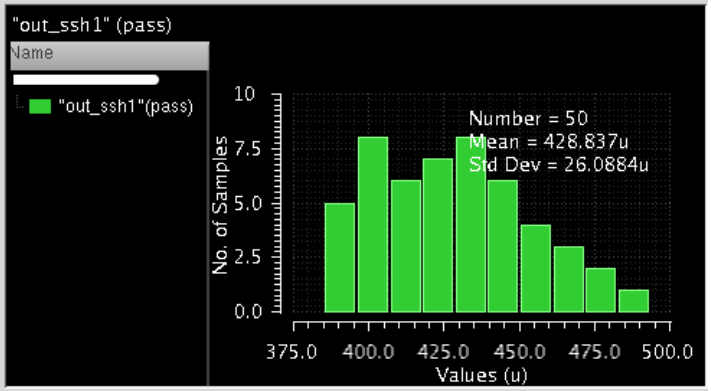


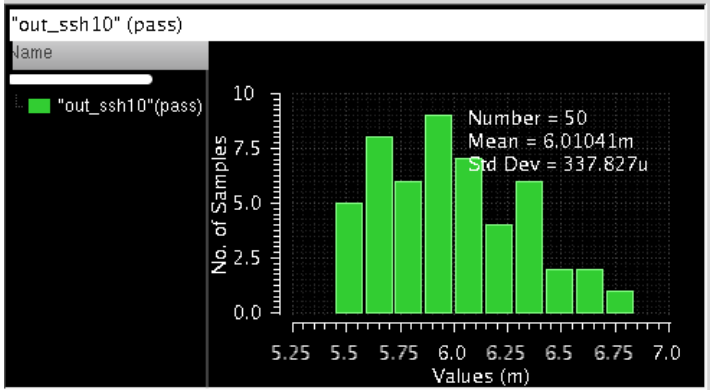
Monte Carlo











The dispersion is mainly due to the feedback capacitance of the preamplifier (+/- 10% accuracy)

Noise issues

- Noise contributions not understood. (doesn't seem to fit the theory)
- 6 pF doesn't give enough first stage gain to have a nice noise behaviour. 2 pF is preferable but the handled charge range will be reduced.

Different preamplifier design options

- A Nmos common source was used for these simulations.
- Differential amplifier and Pmos common source have been studied too.
- Differential:
  - Differential preamplifier works well and permits high gain in open loop (2-stages) and so 1/1000 linearity.
  - More noise and consumption.
  - Bigger surface (2 input transistors, adjustable compensation capacitor)
- Pmos common source:
  - Preamplifier architecture of skiroc2.
  - Standard cascode reduces the dynamic range, so folded cascode is used instead, leading in a drop in open loop gain and thus degrading closed loop linearity.
  - Potentially the same issues with power supply than in skiroc2.

Different building blocks design options

- Bandgap
- Shaper amplifiers
- Analog memories

Schedule

- Tape-out in May
- Back in october
- First results expected in december
- Possibly a new skiroc prototype on 0.18 µm

Thanks for your attention