



**Last results on  
HARDROC 3**

***OMEGA, 19/03/2014***

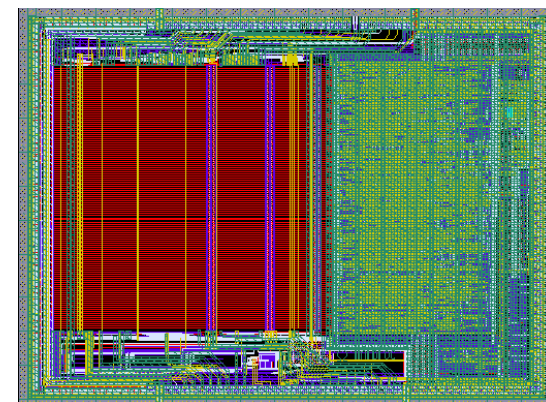
OMEGA microelectronics group

Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

## ❑ 3<sup>rd</sup> generation chip for ILD

❑ Independent channels (zero suppress)

❑ I2C link (@IPNL) for Slow Control parameters and triple voting

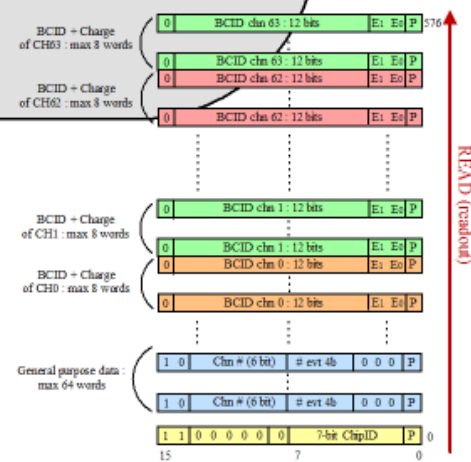
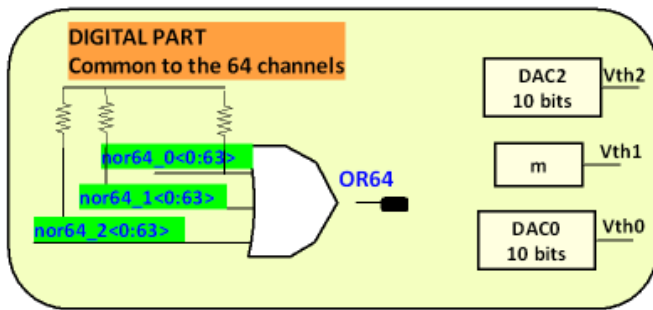
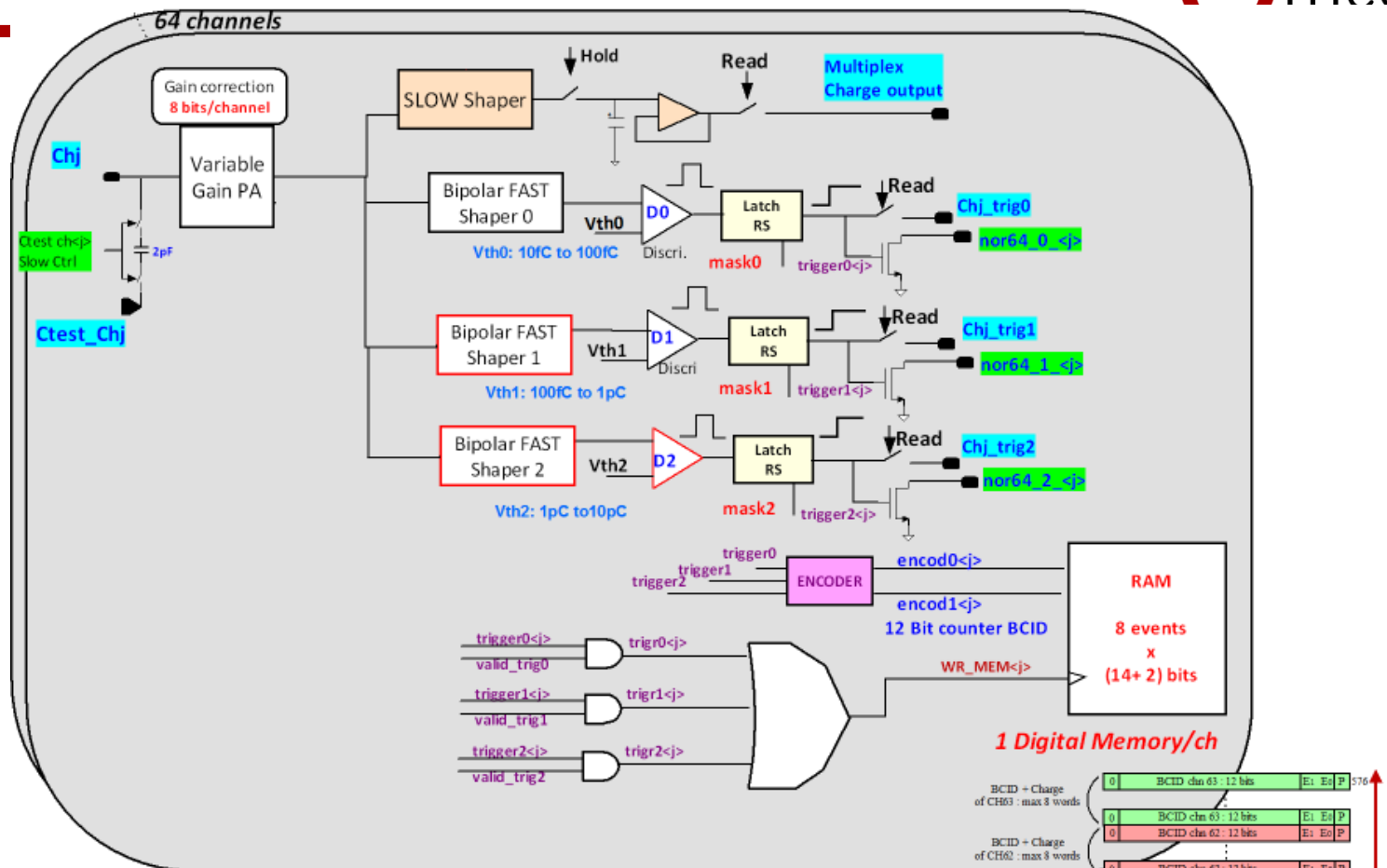


## ❑ HARDROC3: 1<sup>st</sup> of the 3<sup>rd</sup> generation chip to be submitted

- analog part: extension of the dynamic
- PLL: integrated to generate fast clock internally
- Submitted in Feb 2013 (SiGe 0.35 $\mu$ m), funded by AIDA, received end of June 2013
- Die size  $\sim 30 \text{ mm}^2$  (6.3 x 4.7 mm<sup>2</sup>)
- Packaged in a QFP208
- HR3 will equip 2-3m RPC chambers



# SIMPLIFIED SCHEMATICS

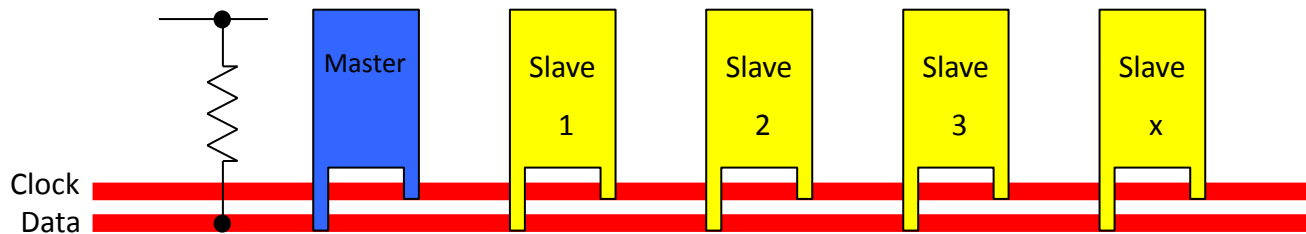


# Slow Control

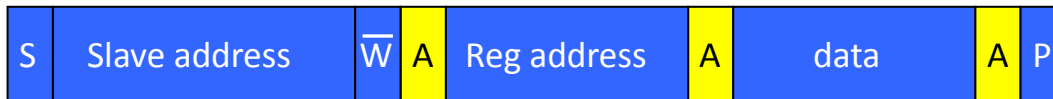
- Slow control common features:
  - Triple voting
  - Read back of control bit (also when chip running)

} Test OK

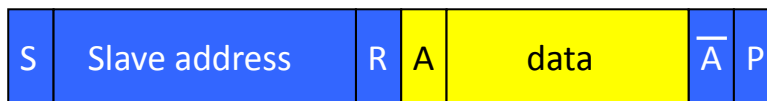
- Slow control access:
  - Classical shift register → Test OK
  - I2C serial link → See below



Write frame:



Read frame:



**Pb: Data stuck to 0 inside the chip**  
 (buffer added by OMEGA to output the data)

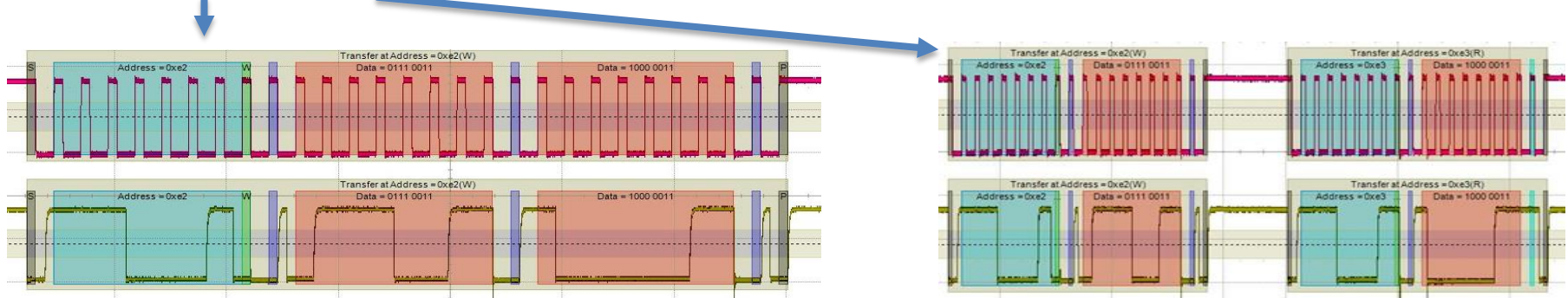
⇒ I2C link test only possible with chip modification (FIB)

# I2C Tests on FIB chips

## Full FIB (2 cut + 1 strap) to bypass buffer on board HR3\_01:

⇒ Write and Read access with Chip ID: 0xE2 / Reg @: 0x73 / WrData: 0x83

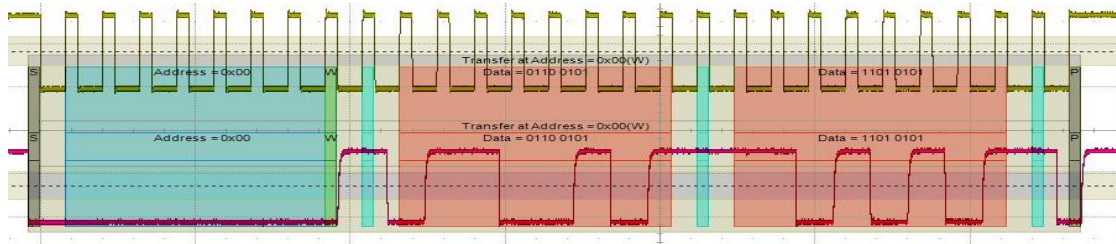
Test OK



## FIB (1 cut) to isolate buffer HR3\_03:

⇒ Only Write access possible (no acknowledge)

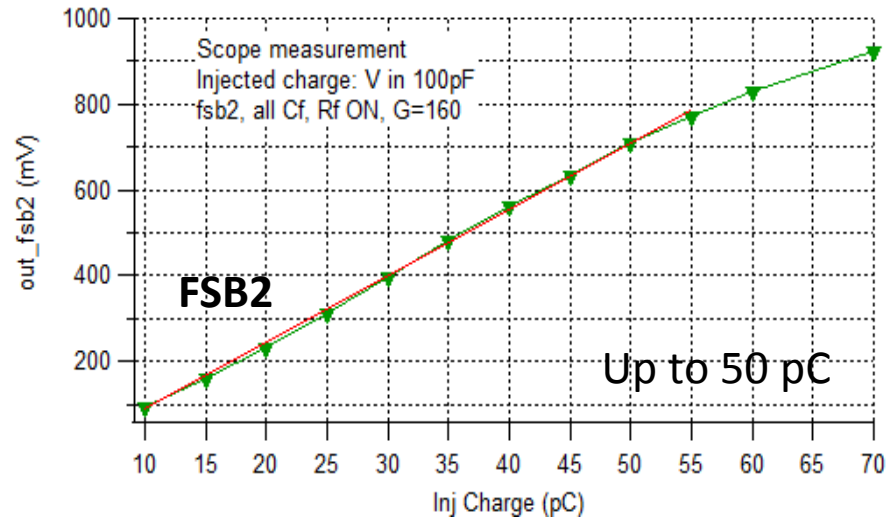
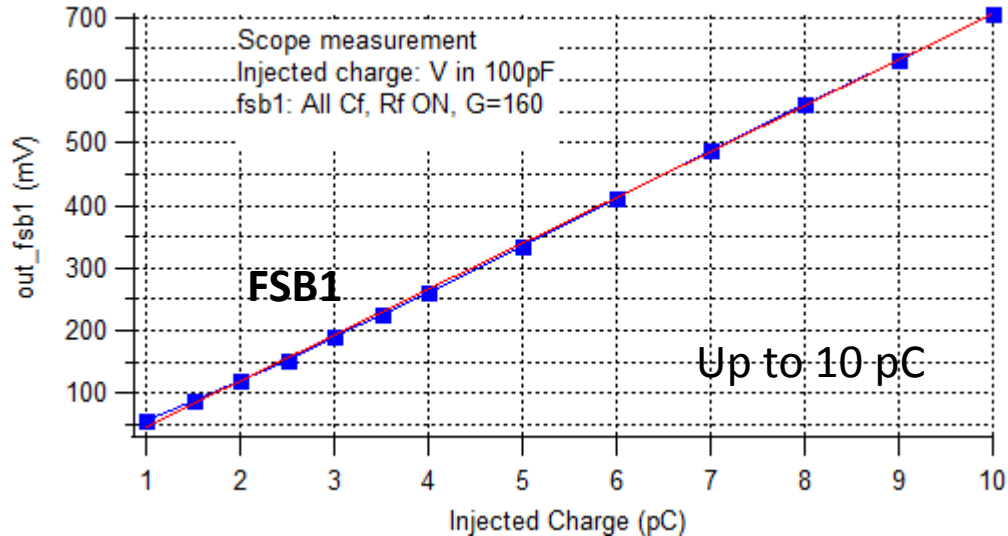
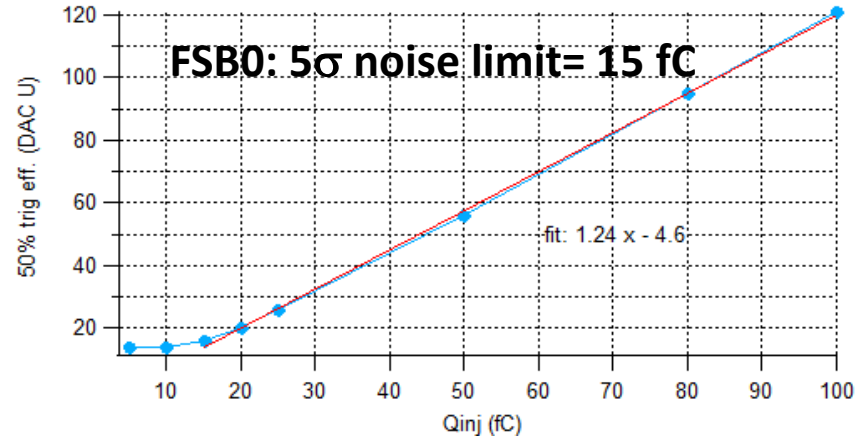
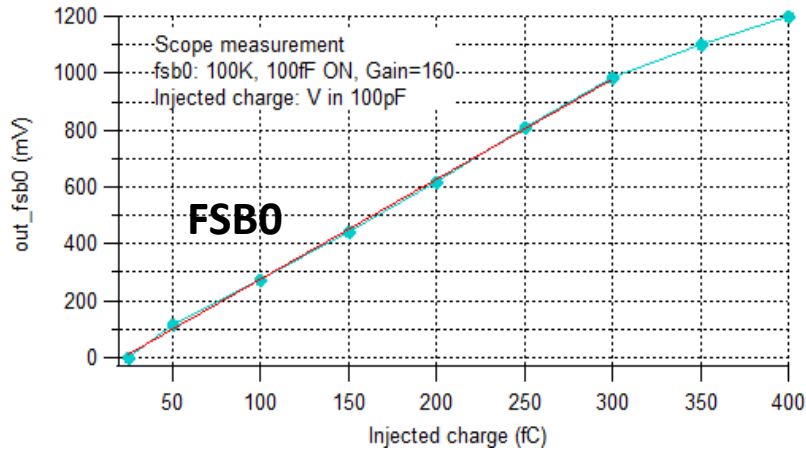
Test OK



## Other I2C tests:

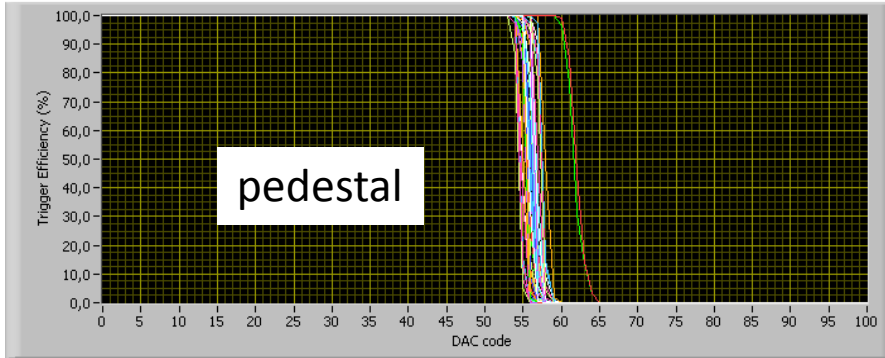
- ⇒ Tests @ High/Low temperature
- ⇒ I2C @ 400Khz with 500pF on Bidir data port

# Analog Part: FSB Linearity

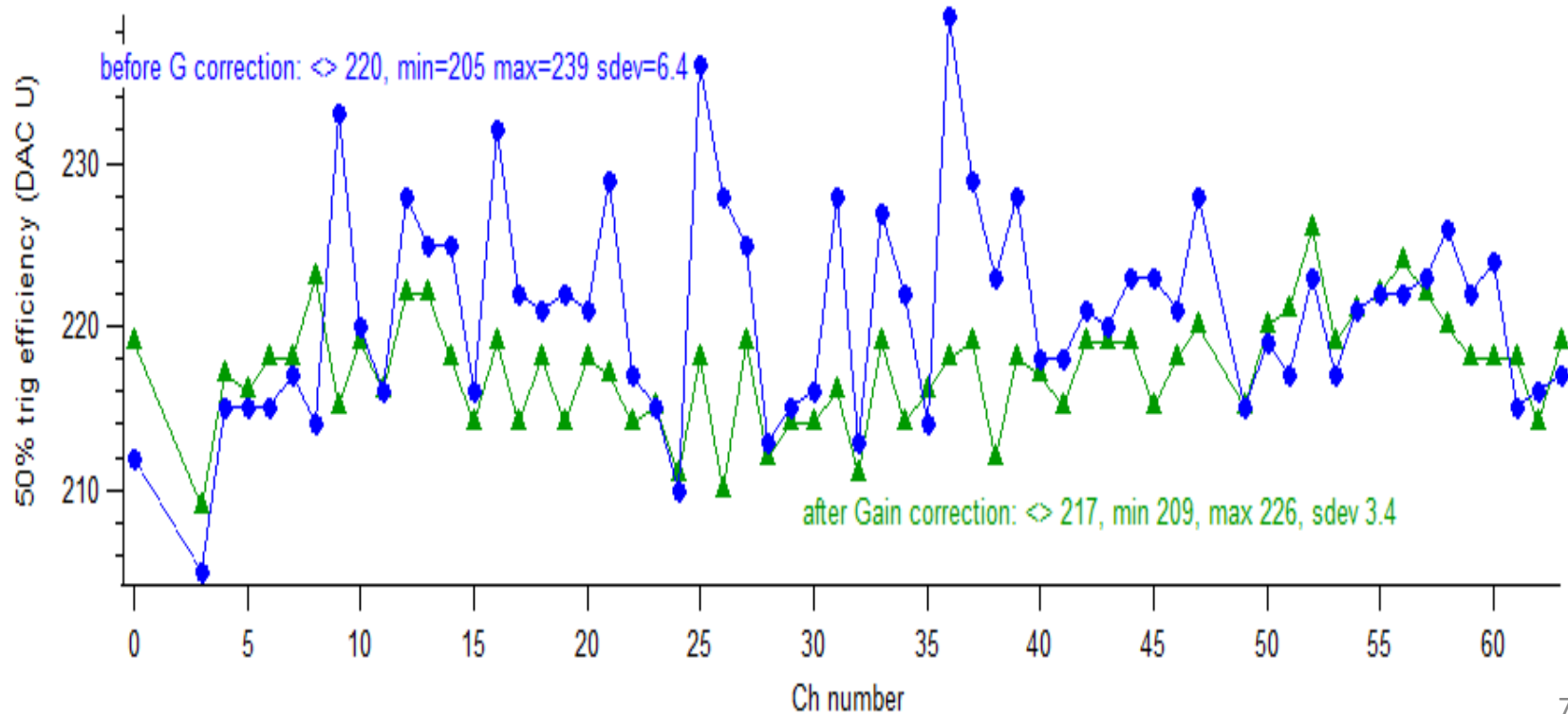
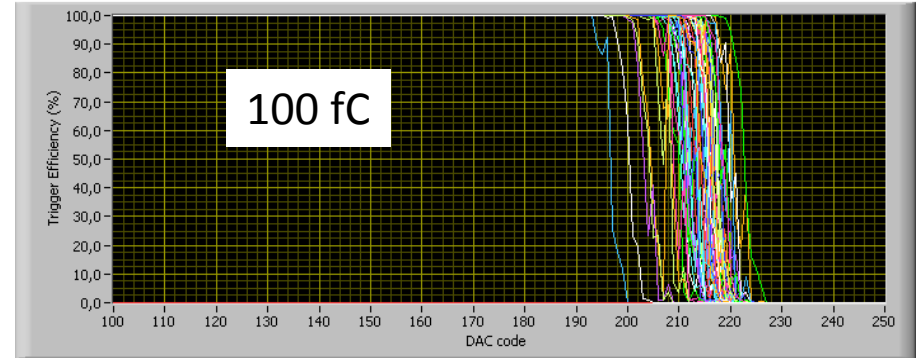


# SCURVE measurements

Test S-Curve vs Threshold (all ch.)



Test S-Curve vs Threshold (all ch.)

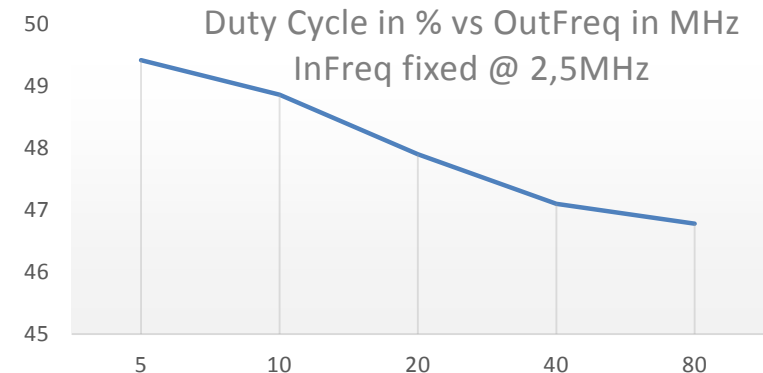
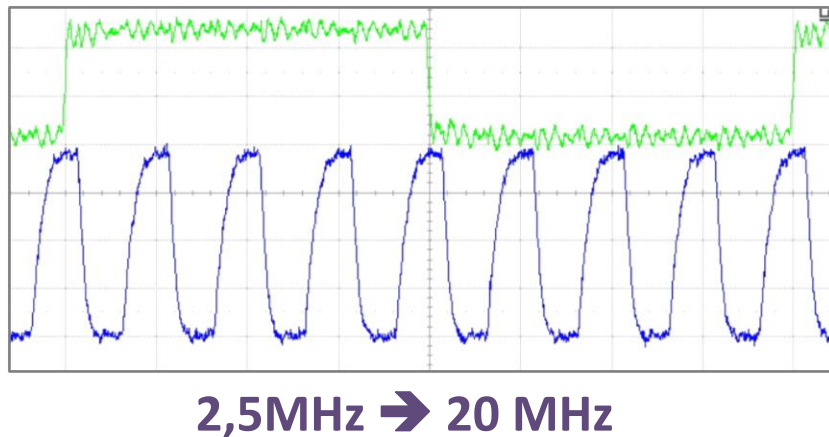
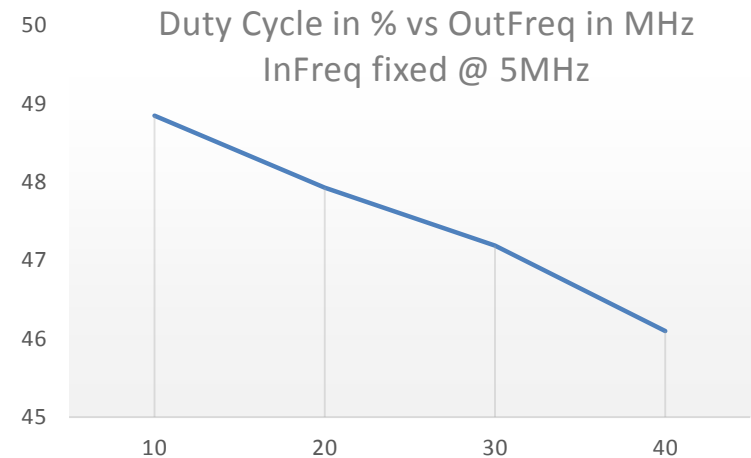
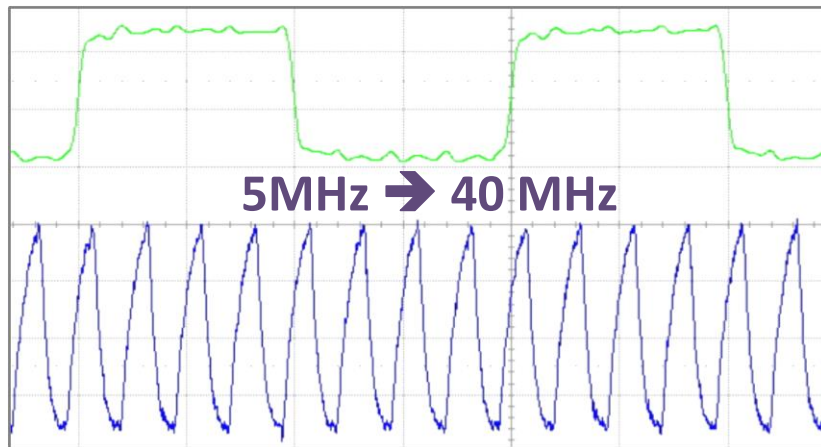


# PLL measurements

## PLL can generate fast clock internally (40 MHz):

- ⇒ Multiplication factor is  $(N+1)$  /  $N$  is a SC parameter (1 to 31)
- ⇒ Output freq of PLL can go up to 80MHz (needed is 40-50 MHz)
- ⇒ Full chain tested with charge injected on one and readout

} Tests OK

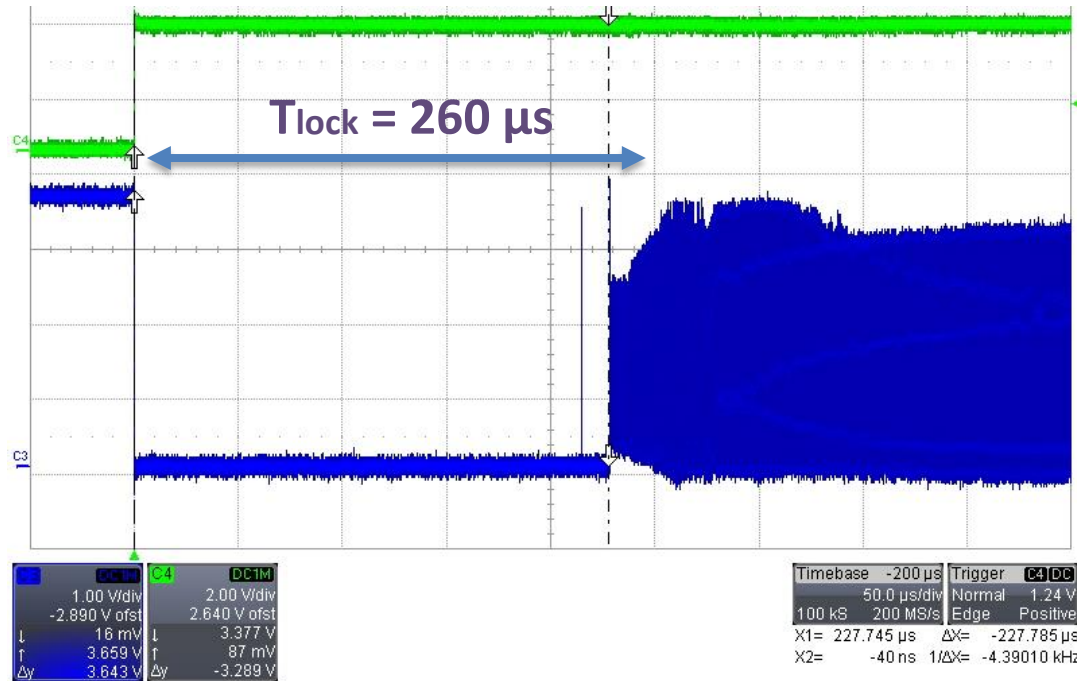




## Lock time (Bias ON):

⇒ Green = PowerOnD / Blue = Out\_PLL

⇒ Time needed to have a stable clock =  $230 + 30 = 260 \mu\text{s}$

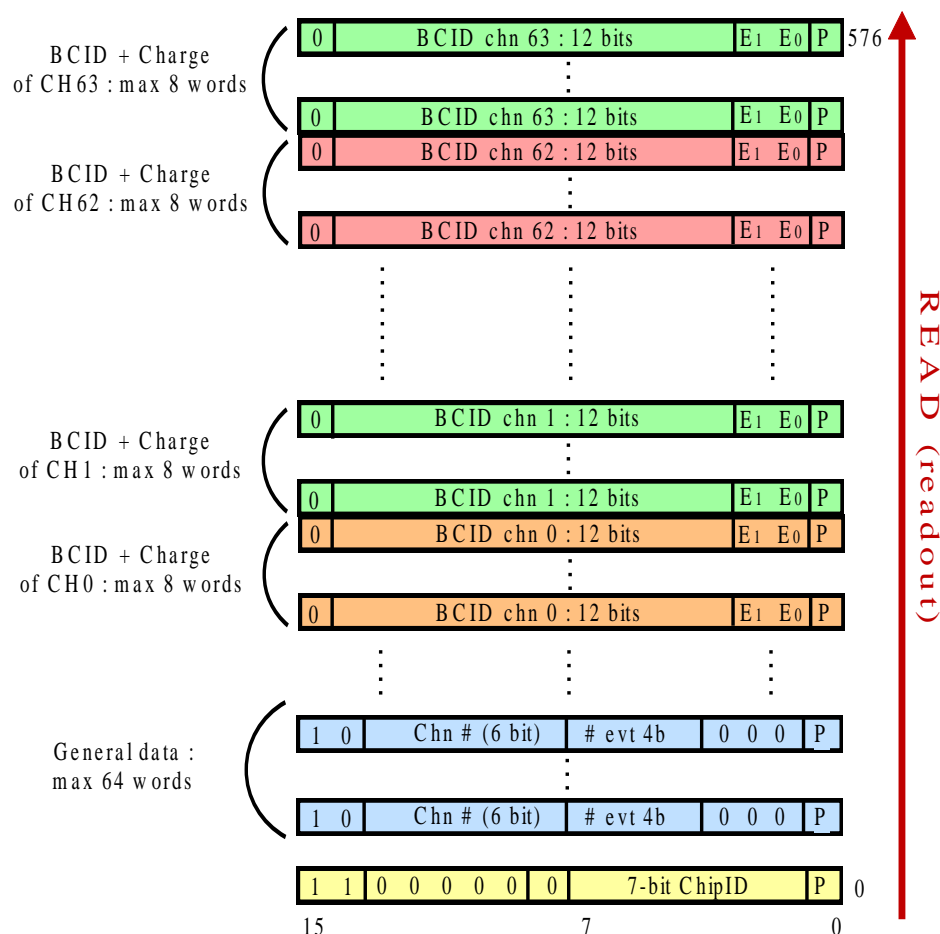


## Other measurements:

⇒ PLL jitter < 150 ps

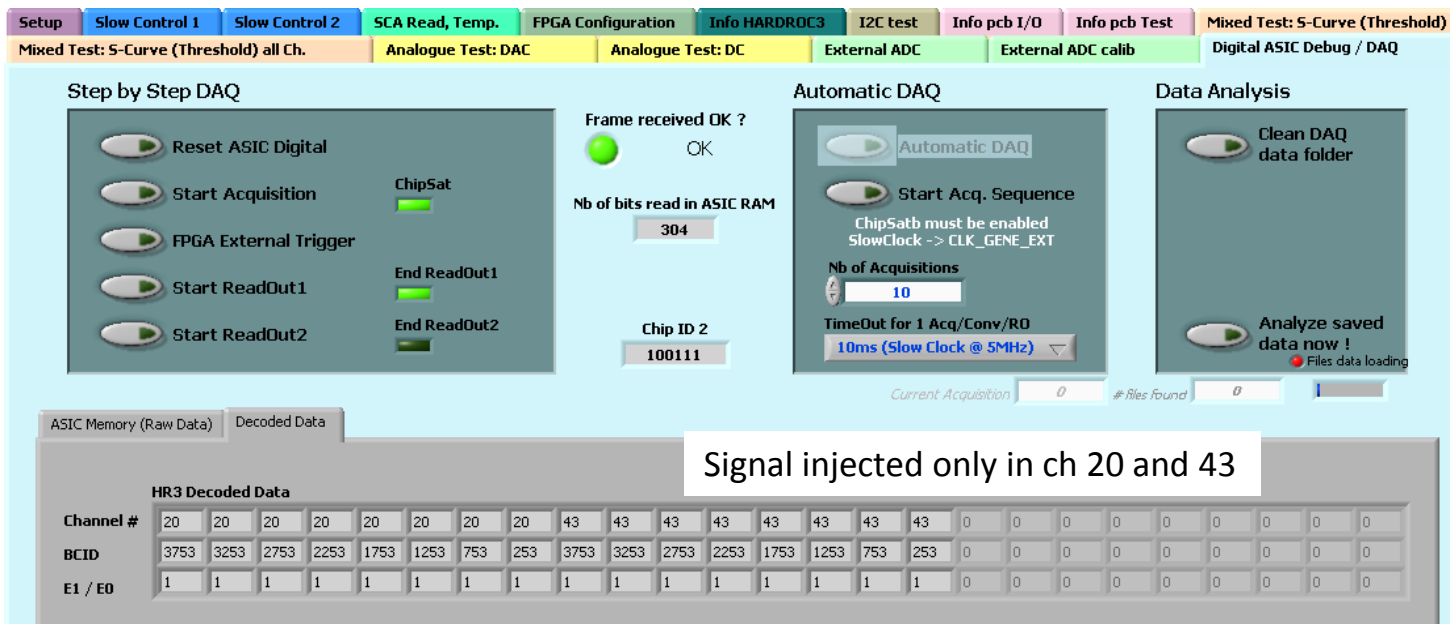
# Digital: Memory mapping

- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - “1”: general data (Hit ch number and number of events)
  - “0”: BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:



	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336

- Zero suppress (only hit channels are readout): **test OK**



The screenshot shows the Omega control interface with several tabs and panels. The top tabs include Setup, Slow Control 1, Slow Control 2, SCA Read, Temp., FPGA Configuration, Info HARDROC3, I2C test, Info pcb I/O, Info pcb Test, and Mixed Test: 5-Curve (Threshold). Below these are more specific test tabs like Mixed Test: 5-Curve (Threshold) all Ch., Analogue Test: DAC, Analogue Test: DC, External ADC, External ADC calib, and Digital ASIC Debug / DAQ.

The main interface is divided into three main sections:

- Step by Step DAQ:** Contains buttons for Reset ASIC Digital, Start Acquisition, FPGA External Trigger, Start ReadOut1, and Start ReadOut2. It also shows status for ChipSat, End ReadOut1, and End ReadOut2.
- Automatic DAQ:** Features an Automatic DAQ button, Start Acq. Sequence button, and a text box stating "ChipSatb must be enabled SlowClock -> CLK\_GENE\_EXT". It includes a field for "Nb of Acquisitions" set to 10 and a "TimeOut for 1 Acq/Conv/RO" dropdown set to 10ms (Slow Clock @ 5MHz).
- Data Analysis:** Includes buttons for "Clean DAQ data folder" and "Analyze saved data now!". A status indicator shows "Files data loading".

At the bottom, there is a table for "HR3 Decoded Data" with columns for Channel #, BCID, and E1 / EO. A white box highlights the text "Signal injected only in ch 20 and 43".

Channel #	20	20	20	20	20	20	20	20	43	43	43	43	43	43	43	43	0	0	0	0	0	0	0	0	0	0	0	0	0
BCID	3753	3253	2753	2253	1753	1253	753	253	3753	3253	2753	2253	1753	1253	753	253	0	0	0	0	0	0	0	0	0	0	0	0	
E1 / EO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	

- Roll mode SC : **test OK**
  - If RollMode = "0" → Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = "1" → 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored
- "Noisy Evt" SC: 64 triggers => Noisy event => no data stored : **test OK**
- "ARCID" SC (Always Read Chip ID): **test OK**
  - If ARCID = 0 → Backward compatibility: No event → No readout
  - If ARCID = 1 → New behavior: No event → Read CHIP ID

# Power consumption



## Power consumption in ILC mode:

- ⇒ Power measured on AlimChip over 1 Ohm resistor
- ⇒ Buffer/SSH/ Widlar/OtaQ/OtaFSB/Temperature OFF
- ⇒ Pll/FastClock LVDS = 0/1 if clocks from LVDS else 1/0
- ⇒ EnPllOut / testOtaQ / ValdSS are disabled
- ⇒ StartAcq On

Power supply	HR3 With Clk from LVDS (Slow clock 5M + 40M) Consumption in $\mu\text{W}$ / channel	HR2 With Clk from LVDS (Slow clock 5M + 40M) Consumption in $\mu\text{W}$ / channel
PowerOnA (Analog)	1650	1325
Only PowerOnADC (OTA)	0	0
Only PowerOnDAC	55	50
Only PowerOn D	725	50
Power-On-All	2430	1425
<b>Power-On-All @ 0,5% duty cycle</b>	<b>12,2</b>	<b>7,5</b>

## Notes:

- ⇒ Analog: increase due to extended dynamic range
- ⇒ Digital: increase due to zero suppress
- ⇒ If the PLL is activated, +3% on the power consumption

- Good analog performance:
  - dynamic range extended up to 50 pC
  - PLL alternative for fast clock
  
- Preliminary good digital performance
  - Zero suppress, roll mode, ARCID mode, Noisy evt mode tested successfully on testboard
  - External trigger available to be able to check the status of each channel
  
- Slow control:
  - Classic shift register, Triple voting and Read back are OK
  - I2C problem understood and tested
  
- Next steps
  - More intensive tests on zero suppress and analog part (multiple channels)
  - Production run expected end 2014
  - 2-3m long RPC chambers to be built and equipped with HR3 in 2015
  - Possible improvements: PLL start boost, power consumption