Last results on HARDROC 3

OMEGA, 19/03/2014

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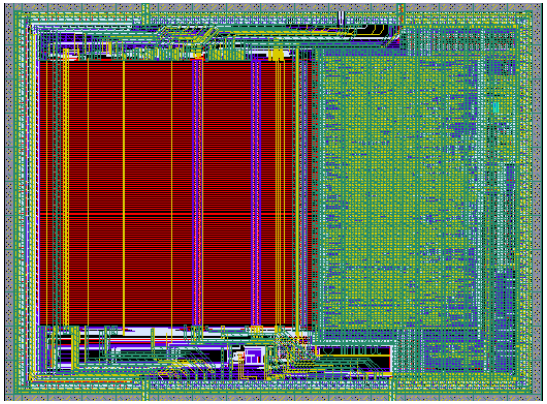
HARDROC3

Omega

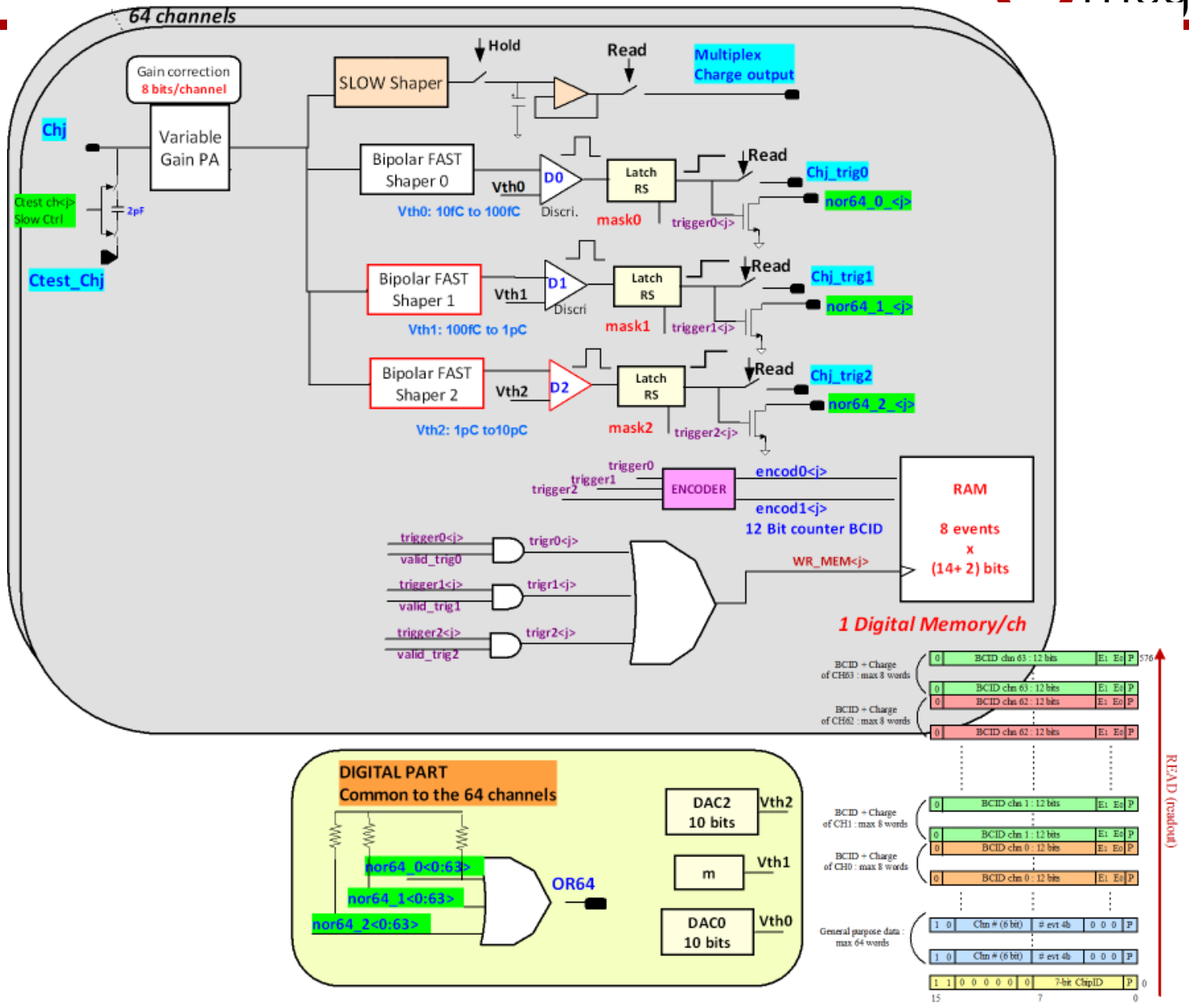
- **3rd generation chip for ILD**
  - **Independent channels (zero suppress)**
  - **I2C link (@IPNL)** for Slow Control parameters and **triple voting**



- HARDROC3: 1st of the 3rd generation chip to be submitted
  - analog part: extension of the dynamic
  - PLL: integrated to generate fast clock internally
  - Submitted in Feb 2013 (SiGe 0.35µm), funded by AIDA, received end of June 2013
  - Die size ~30 mm² (6.3 x 4.7 mm²)
  - Packaged in a QFP208
  - HR3 will equip 2-3m RPC chambers

AIDA

SIMPLIFIED SCHEMATICS

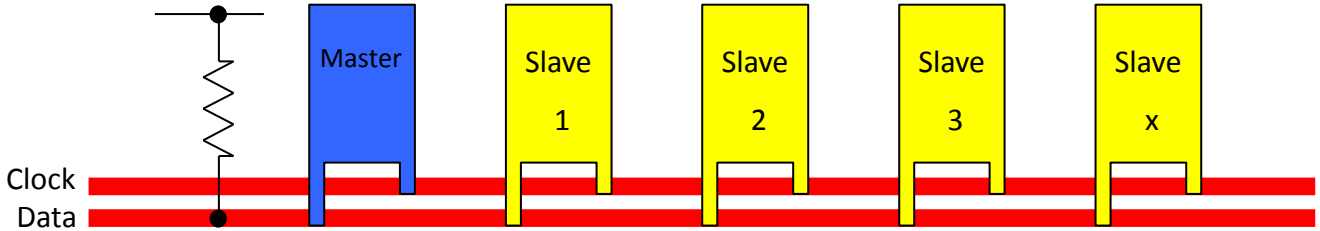


Slow Control

- Slow control common features:
  - Triple voting
  - Read back of control bit (also when chip running)

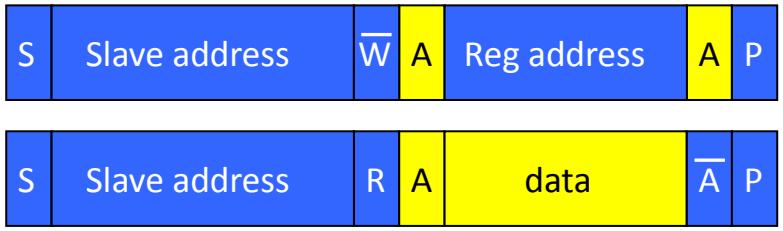
  } **Test OK**

- Slow control access:
  - Classical shift register → **Test OK**
  - I2C serial link → **See below**



Write frame:

Read frame:

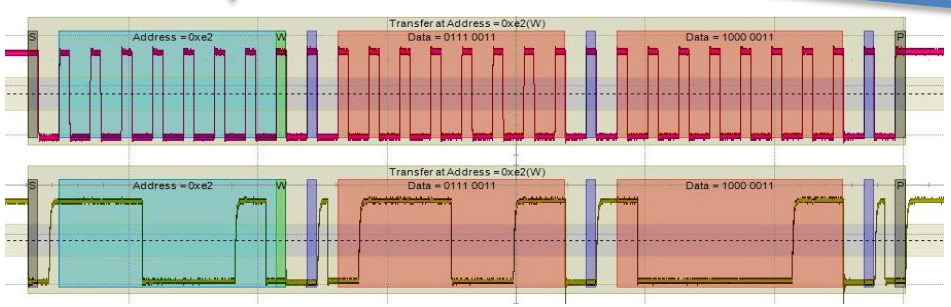


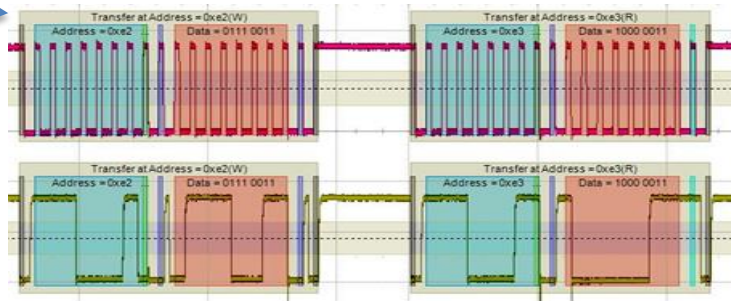
Pb: Data stuck to 0 inside the chip
(buffer added by OMEGA to output the data)
⇒ I2C link test only possible with chip modification (FIB)

I2C Tests on FIB chips

Full FIB (2 cut + 1 strap) to bypass buffer on board HR3_01:

⇒ Write and Read access with Chip ID: 0xE2 / Reg @: 0x73 / WrData: 0x83 → **Test OK**





FIB (1 cut) to isolate buffer HR3_03: → Test OK

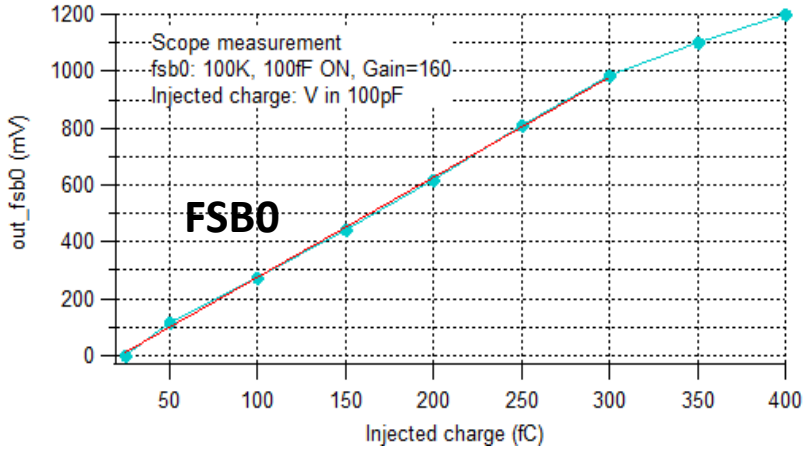
⇒ Only Write access possible (no acknowledge)

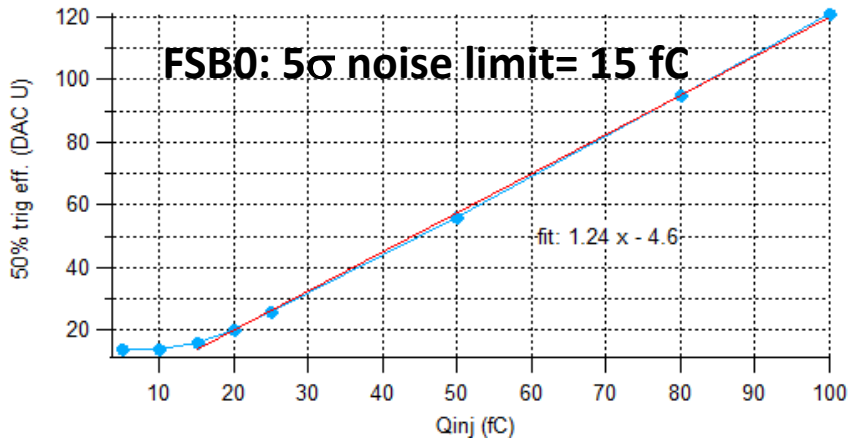
Other I2C tests:

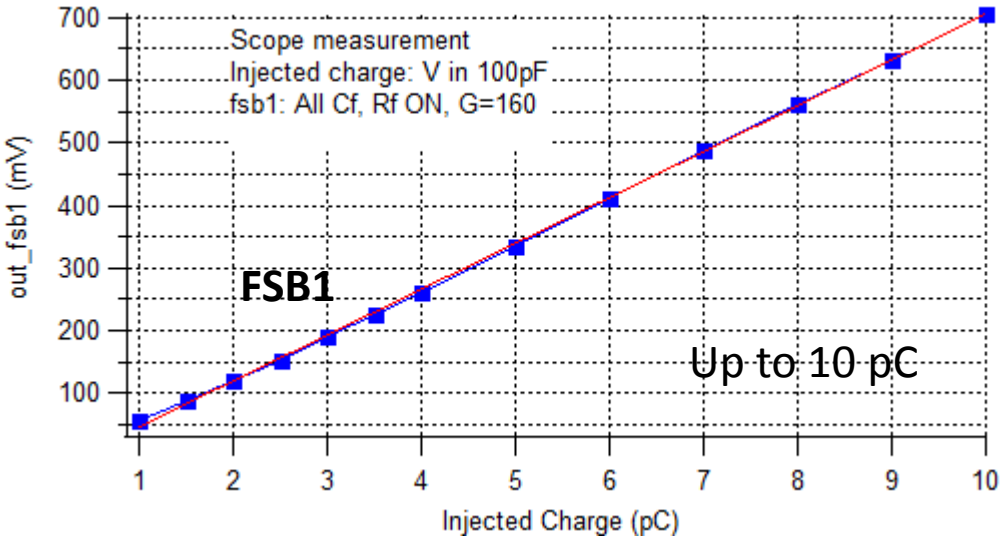
⇒ Tests @ High/Low temperature

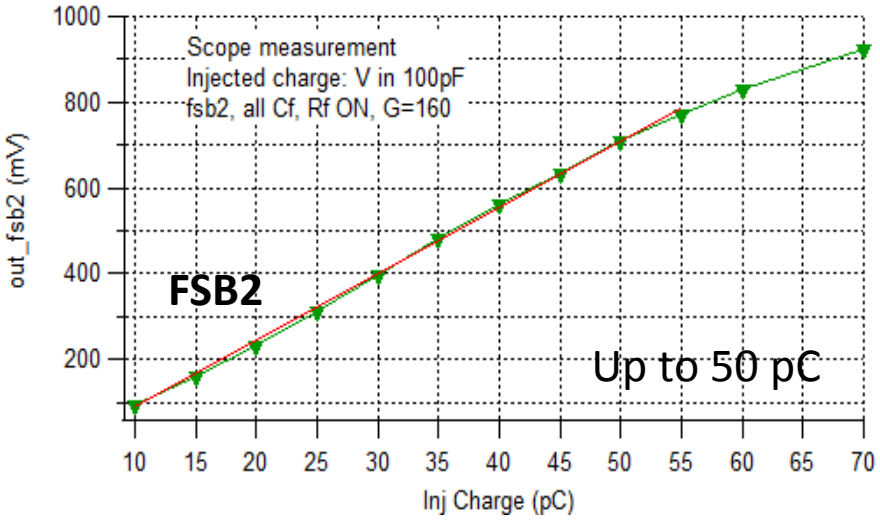
⇒ I2C @ 400Khz with 500pF on Bidir data port

Analog Part: FSB Linearity

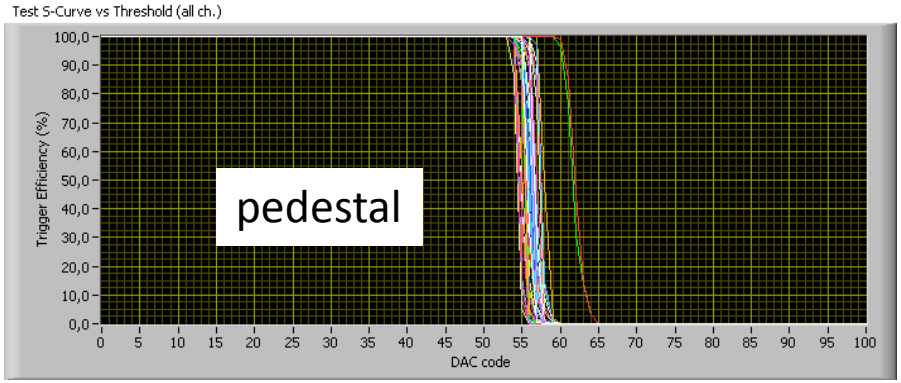


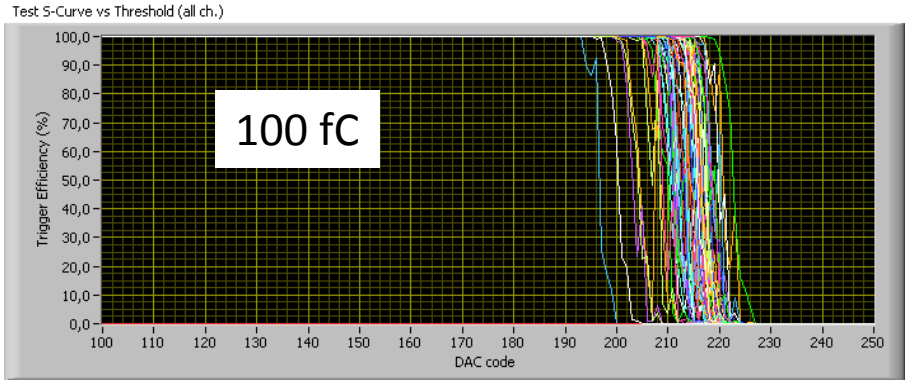


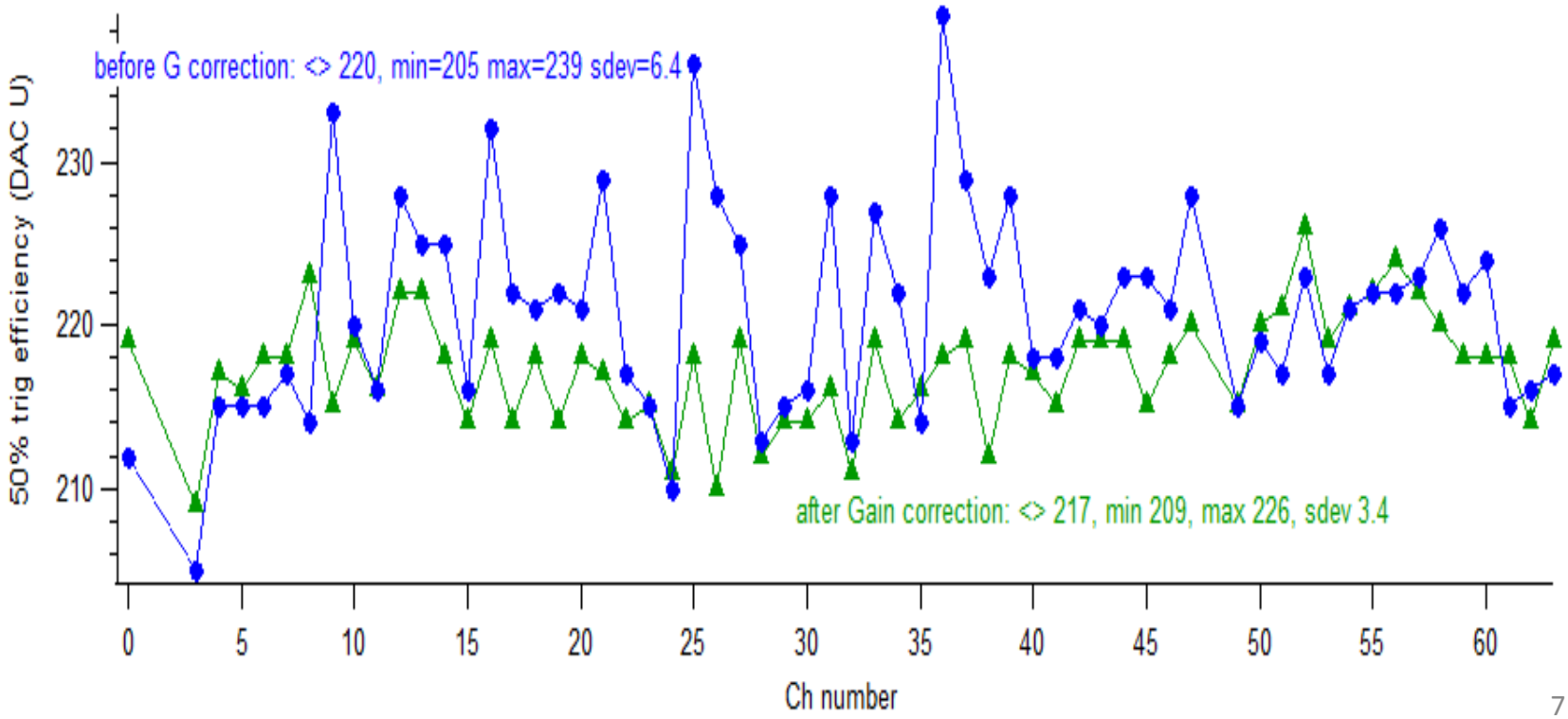




SCURVE measurements







PLL measurements

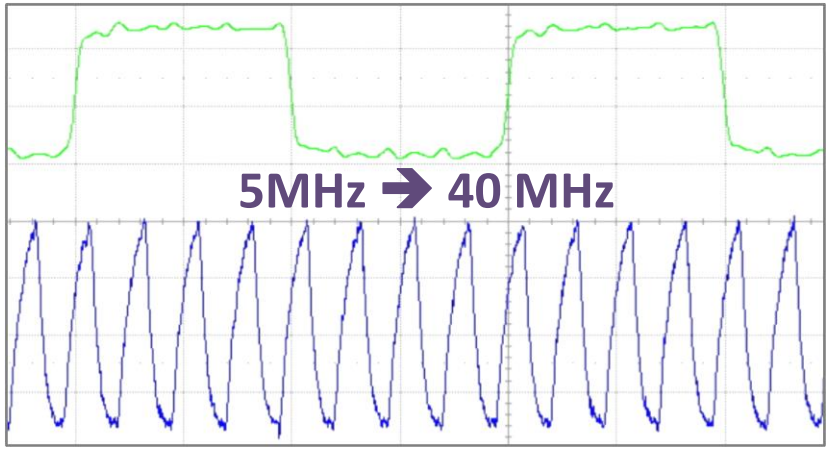
PLL can generate fast clock internally (40 MHz):

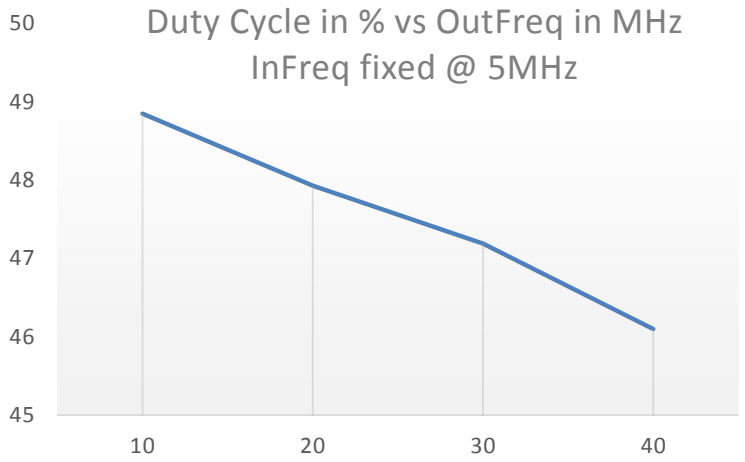
⇒ Multiplication factor is (N+1) / N is a SC parameter (1 to 31)

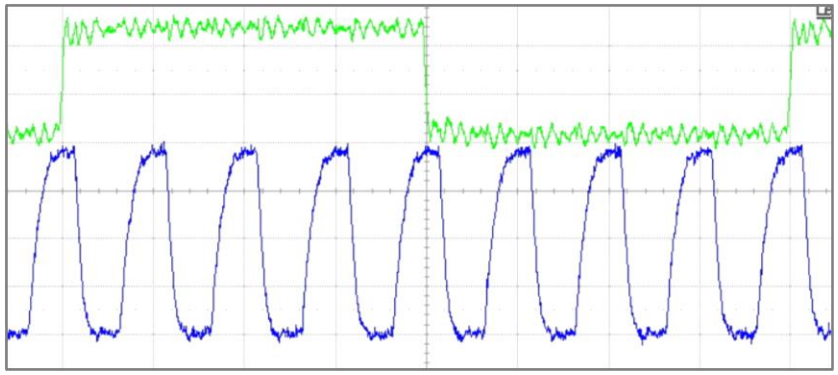
⇒ Output freq of PLL can go up to 80MHz (needed is 40-50 MHz)

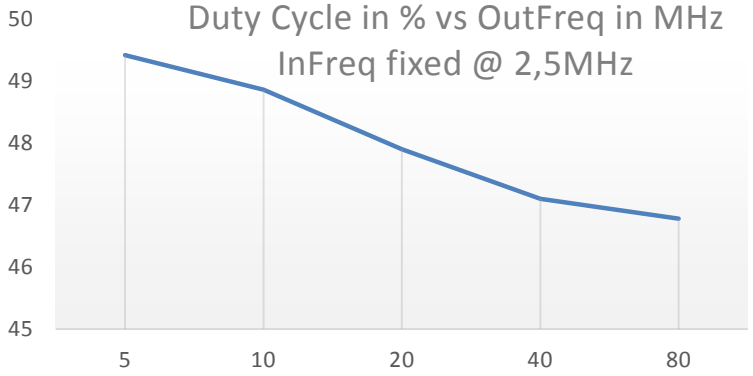
⇒ Full chain tested with charge injected on one and readout

Tests OK







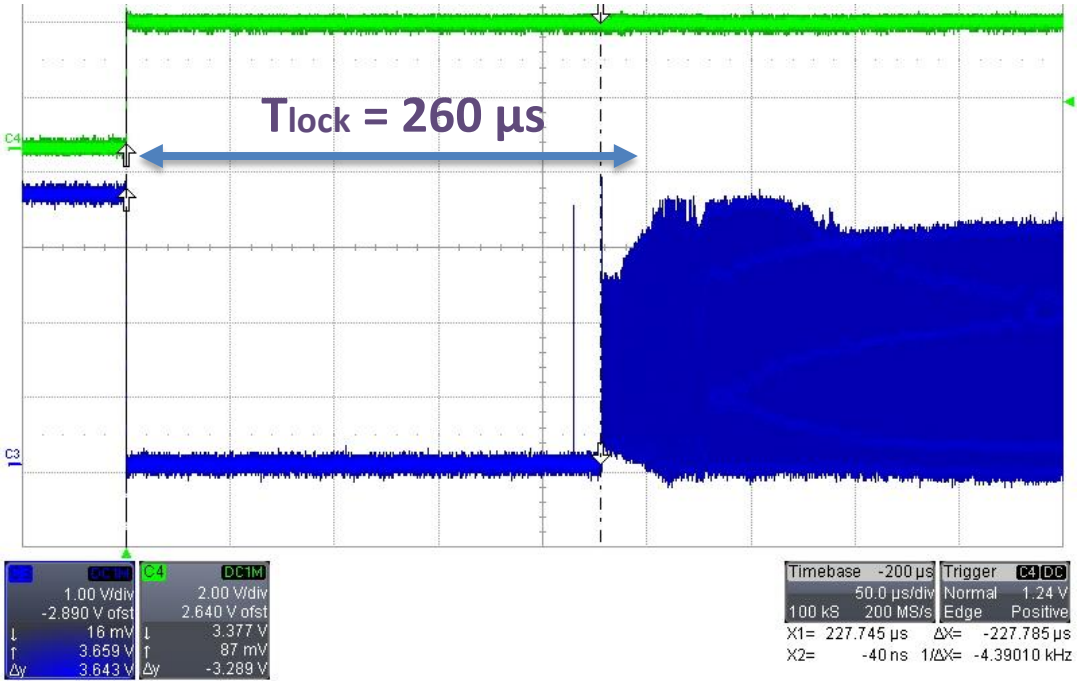


PLL measurements

Lock time (Bias ON):

⇒ Green = PowerOnD / Blue = Out_PLL

⇒ Time needed to have a stable clock = 230 + 30 = 260 µs



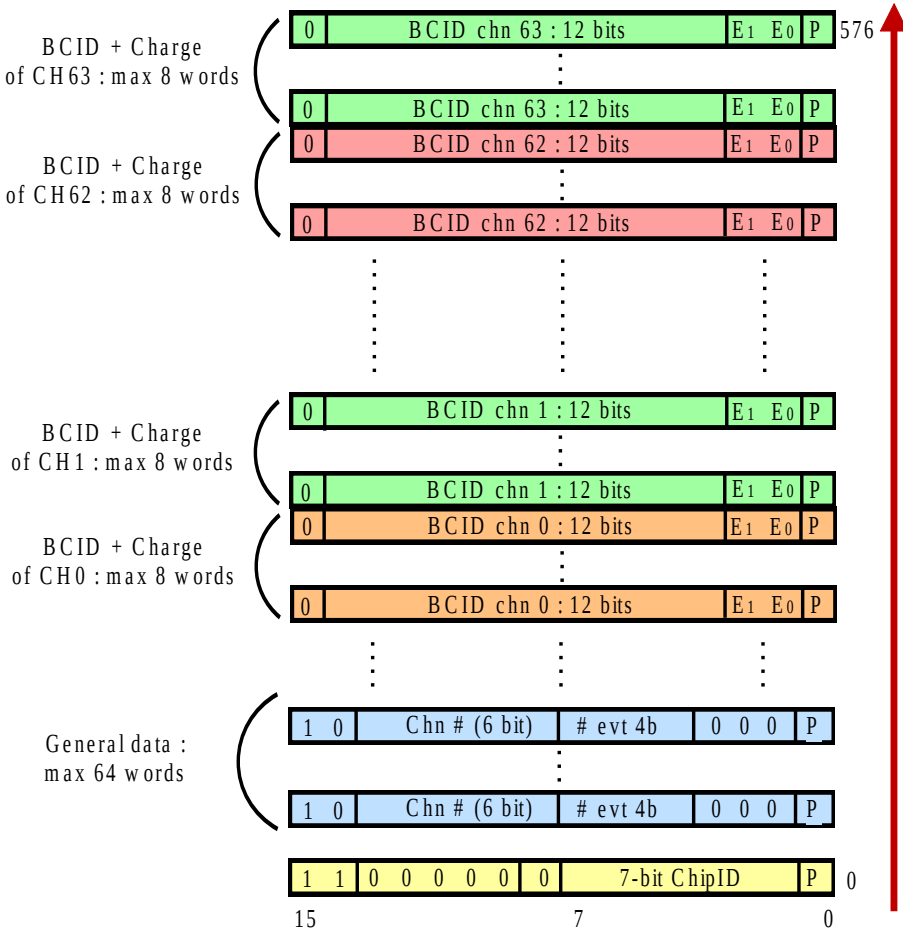
Other measurements:

⇒ PLL jitter < 150 ps

Digital: Memory mapping

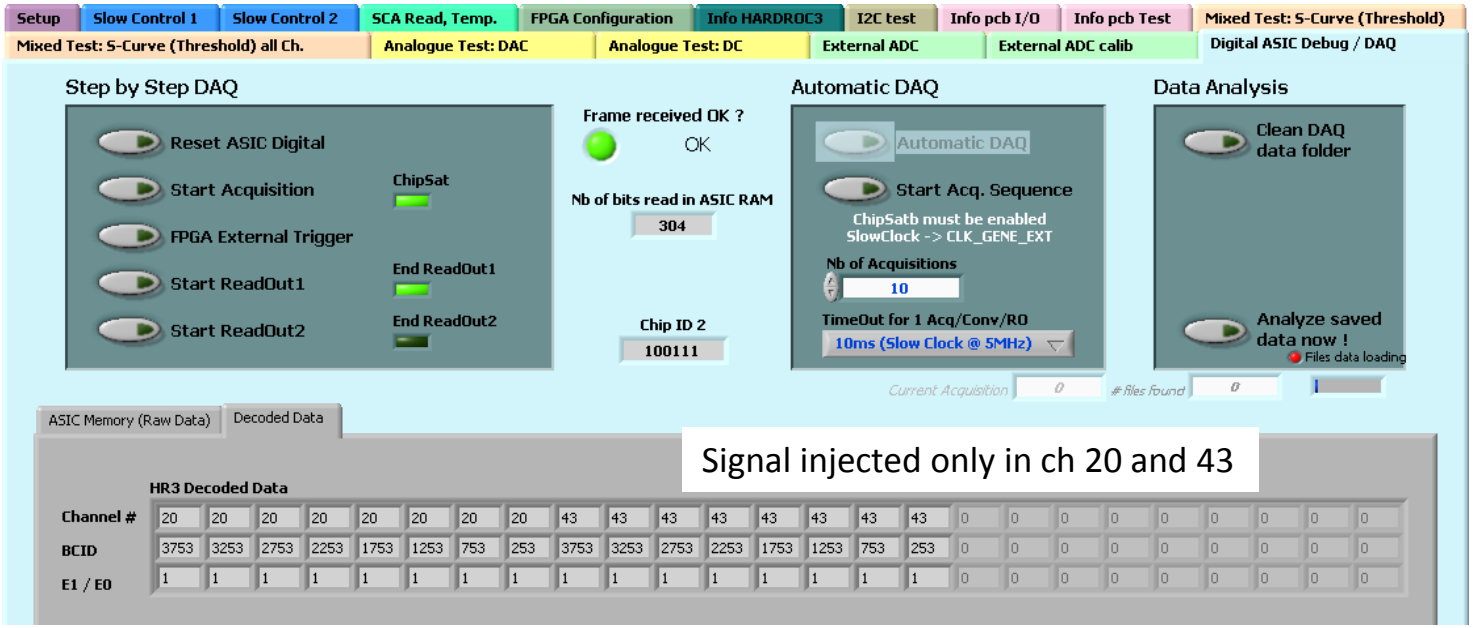
- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - "1": general data (Hit ch number and number of events)
  - "0": BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:

	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336



Digital: zero suppress

- Zero suppress (only hit channels are readout): test OK



- Roll mode SC : test OK
  - If RollMode = "0" ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = "1" ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored
- "Noisy Evt" SC: 64 triggers => Noisy event => no data stored : test OK
- "ARCID" SC (Always Read Chip ID): test OK
  - If ARCID = 0 ➔ Backward compatibility: No event ➔ No readout
  - If ARCID= 1 ➔ New behavior: No event ➔ Read CHIP ID

Power consumption

Power consumption in ILC mode:

⇒ Power measured on AlimChip over 1 Ohm resistor
⇒ Buffer/SSH/ Widlar/OtaQ/OtaFSB/Temperature OFF
⇒ Pll/FastClock LVDS = 0/1 if clocks from LVDS else 1/0
⇒ EnPllOut / testOtaQ / ValdSS are disabled
⇒ StartAcq On

Power supply	HR3 With Clk from LVDS (Slow clock 5M + 40M) Consumption in µW / channel	HR2 With Clk from LVDS (Slow clock 5M + 40M) Consumption in µW / channel
PowerOnA (Analog)	1650	1325
Only PowerOnADC (OTA)	0	0
Only PowerOnDAC	55	50
Only PowerOn D	725	50
Power-On-All	2430	1425
Power-On-All @ 0,5% duty cycle	**12,2**	**7,5**

Notes:

⇒ Analog: increase due to extended dynamic range
⇒ Digital: increase due to zero suppress
⇒ If the PLL is activated, +3% on the power consumption

Summary and next steps

- Good analog performance:
  - dynamic range extended up to 50 pC
  - PLL alternative for fast clock
- Preliminary good digital performance
  - Zero suppress, roll mode, ARCID mode, Noisy evt mode tested successfully on testboard
  - External trigger available to be able to check the status of each channel
- Slow control:
  - Classic shift register, Triple voting and Read back are OK
  - I2C problem understood and tested
- Next steps
  - More intensive tests on zero suppress and analog part (multiple channels)
  - Production run expected end 2014
  - 2-3m long RPC chambers to be built and equipped with HR3 in 2015
  - Possible improvements: PLL start boost, power consumption