AHCAL Status & R&D Directions



CALICE Collaboration Meeting Argonne Nat'l Lab, March 2014 Frank Simon Max-Planck-Institute for Physics

 $\int \Delta p \cdot \Delta g \ge \frac{1}{2} t$

Max-Planck-Institut für Physik (Werner-Heisenberg-Institut)

Outline

- The Physics Harvest
- R&D Directions
 - Photon Sensors
 - Scintillator Tiles
 - Large-scale QA and assembly
 - Electronics & DAQ
 - Calorimetry Mechanics
- Test Beam Plans
- Conclusions

Includes material from Felix, in particular on QA issues for surfacemounted SiPMs and tiles



























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- More in the pipeline
 - Further extension of proton vs pion studies
 - Extension of software compensation to full CALICE setup (already documented in CAN-015 (2009), now with full calibration)
 - ...
- Spin-offs:
 - Time structure of hadronic showers with T3B





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Test beams with next-generation prototype have begun - focus more technical, but also expect additional physics results

• For example: Timing capability over full volume





















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The Challenges of Large Numbers

- 1 calorimeter (barrel + 2 end-caps)
- 60 sub-modules

- 3 000 layers
- 60 000 HBUs
- 200 000 ASICs
- 8 000 000 Tiles + SiPMs





- 1 working year
- 46 weeks
- 230 days
- 2 000 hours
- 100 000 minutes

• 7 000 000 seconds





Main R&D Topics

- Optimization / Re-thinking of key components
 - SiPMs Profit from industrialisation, large number of possible suppliers R&D (with one exception) not done within "our" community - but active exchange with various manufacturers
 - Scintillator tiles Automatic assembly a key challenge, explore alternative ideas for coupling of SiPMs and tiles, re-optimize design
- Establish a production concept
 - QA of all key components prior to assembly What / which level is needed?
 - Automatization of QA steps
 - Automatic assembly procedures if small components (at least up to HBU level)





• The CALICE AHCAL was the first large-scale use of SiPMs!

... and the technology has evolved quite a bit since then - now used "everywhere", with many possible producers.

- What we need:
 - Decent efficiency
 - Reasonable noise rate
 - Reasonable dynamic range
 - Low cost





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Packaging is important:

- Compactness to reduce dead area
- Long-term stability of materials (on the level of decades!)
- Robustness for installation / storage before further assembly
- ► Need experience with producers (and experienced producers! Bad surprises recently)





 The requirements change substantially when moving to realistic detectors: Auto-trigger - Have to avoid accidental signals at the ~ 0.2 - 0.4 MIP level! (stricter requirement than with external beam trigger)





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MPPC cross-talk level:

~ 25% - 30%

KETEK PM1125, with "trenches" (used at UHH) cross-talk level: ~ 5% results in 0.1 Hz noise rate at 0.2 MIP with UHH tiles

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NB: Cross-talk depends on operating conditions. Impact depends on active area of sensor!



Marco Szalay



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1st design for tech. prototype₁



fiberless coupling: easier manufacturing, increased tolerances proof of principle: fiberless coupling, injection molding









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Large-Scale Tile Productions...

- Larger batches (several 100) of fiber and fiberless tiles have been produced at ITEP
- Ongoing production at UHH -> machining with slightly adapted MPP design
 - semi-automatic packaging of tiles in laser-cut (non-adhesive) reflector foil





- New generation of KETEK SiPMs: High light yield
- High degree of response uniformity







Large-scale QA

- Need QA for each component and at each integration step
- For high device uniformity characterisation becomes QA, but precision requirements on test procedures remain the same
- Present scheme:
 - test scintillator LY (source)
 - test SiPM
 - gain, noise, noise over threshold (cross talk)
 - test SiPM on tile
 - adjust HV working point to equalise light yield
 - effective dynamic range
 - test ASICs (test board, need to automatise)
 - test HBU
 - HBU with tile
 - gain / threshold equalisation
- Open issues:
 - are we still sensitive to optical coupling variations?
 - if not, LY equalisation could be done with bare SiPM
 - would be obsolete with sufficient signal / noise and dynamic range
 - same for effective dynamic range





Large-scale Testing of Tiles with SiPMs

 Fast testing of tiles prior to installation - basic functionality test with LED (measure gain, cross-check light collection from tile)





CALICE AHCAL Meeting Hamburg 12 / 2013

Konrad Briggl



- Several 100 tiles already tested currently with 15 point voltage scan
- 2 minutes for 12 tiles (measured in parallel), then repositioning of head



Frank U...



- Large number of tiles require automatic assembly of full HBUs \bullet
- Requires precise placement of Tiles with SiPMs in HBU boards, followed by soldering

Challenge 1: Placement precision and tolerances

Higher stability expected w/o alignment pins: Precise placement of SiPM pins, tile fixed by fast-curing glue put on board via screen printing prior to tile placement









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Challenge 2: Soldering of pre-assembled and heat-sensitive components

- Have to avoid detachment of HBU SMD components, heat damage of tiles
- ► Two options to study
 - Selective (point-by-point) soldering disadvantage: rather slow, can be sped up by multi-point head, would profit from symmetric soldering positions
 - Wave soldering fast, but heats up everything: Needs thermal protection mask, special requirements for clearance between tile solder points and components



extensively studied at Mainz







Re-thinking the Tile Design

• Alternative tile concept: SiPMs on electronics, tiles coupled via bottom - avoids soldering with tiles - Proof of principle from NIU, adaptations by ITEP and Mainz

Many (all?) issues to be addressed again:

- Light yield optimisation
 - trade-off with LY uniformity: understand performance impact
 - trade-off with SiPM size: understand cost and noise impact
 - trade-off with alignment precision requirements (PCB and scint.)
 - under mass production assembly constraints
 - includes reflective coating schemes
- tile to PCB mechanical fixture and alignment
 - SiPM package and solder (un-solder?) procedure
 - With mega-tiles, additional questions:
 - optical cross-talk, uniformity of it, impact on performance
 - mechanical precision: alignment and flatness
 - tile, tile-to-tile and mega-tile to mega-tile uniformity











Specific QA Challenges for on-Board SiPMs

- SiPM testing before assembly
 - connect and disconnect
 - identify and store
- SiPM testing on board
 - limited by electronics of final detector vs lab set-ups
 - without tile? reproducible illumination, damage protection
 - with tile? light intensity and rate limitations
- Implications on sequence and parallelisation
 - in present scheme, SiPM production and characterisation drives the schedule
 - decoupled from schedule for ASICs and PCBs
 - with SiPM on board more tightly linked, and less time for ASIC development





- Need a versatile front-end chip
 - sub-p.e. resolution for calibration, large dynamic range for sub-MIP to > 100 MIP signals
 - ns level time stamping (background rejection for CLIC, exploit time structure in clustering, ...)
 - Cell-by-cell auto-trigger: Triggerless readout
 - Powerpulsing: Compact layer!
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 - DAQ Interface
 - Calibration and trigger controller
 - Power







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Identical requirements for scintillator ECAL with x2 higher channel density: More complex PCB layout, same functionality





and getting it on Tape . . .

- Complete, flexible system: ullet
 - can integrate other CALICE calorimeters
 - provides possible starting point for full experiment DAQ
 - Based on original CALICE DAQ, further development of secondgeneration DAQ
- DAQ Interface: DIF part of CIB ullet
- Fist signal distribution: CCC \bullet
- Data aggregation: LDA ullet







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Successfully used for single and multiple HBUs, stepwise development to full scale ongoing







Mechanics - Cassettes

 Provide mechanical stability and protection to HBUs with tiles - Creates insertable readout layers

Proof of principle: Cassettes for technological prototype - designed at DESY, manufactured at Munich using precision welding









Mechanics - Absorber Structure

• Octagonal structure, 19 mm thick stainless steel plates







Mechanics - Absorber Structure

Octagonal structure, 19 mm thick stainless steel plates •



Prototypes:

- one HBU-deep full 48 layer stack
- full size 4-layer unit

Steel plates from manufactures are far from the flatness requirements

 Flatness better than 1 mm over full length reached with roller levelling substantially cheaper than machining







Test Beam Plans

- Single layer tests (few HBUs)
- First electromagnetic performance measurements with ~ 10+ HBUs
- Hadronic tests with a few full layers and a shower start finder allows full profile measurements ("a la T3B")
- Gradually build up full hadron calorimeter as HBUs become available







Summary & Outlook

- The AHCAL Physics Prototype delivered a wealth of results and continues to do so
 - From validation to performance to shower physics extending the traditional scope of calorimeter R&D
- A complete concept for a full detector exists with key R&D issues identified
 - Photon sensor picking the optimum
 - Scintillator tiles Re-examine optimization, investigate alternatives
 - Mass QA and production What is needed, on what level?
 - Electronics & DAQ
 - Detector mechanics (active layers & absorbers)
- More test-beams to come: Study performance of technical prototypes, study different designs



