Beam Test result of SiECAL
ramp-up time of electronics under PP operation

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CALICE Meeting @ Argonne

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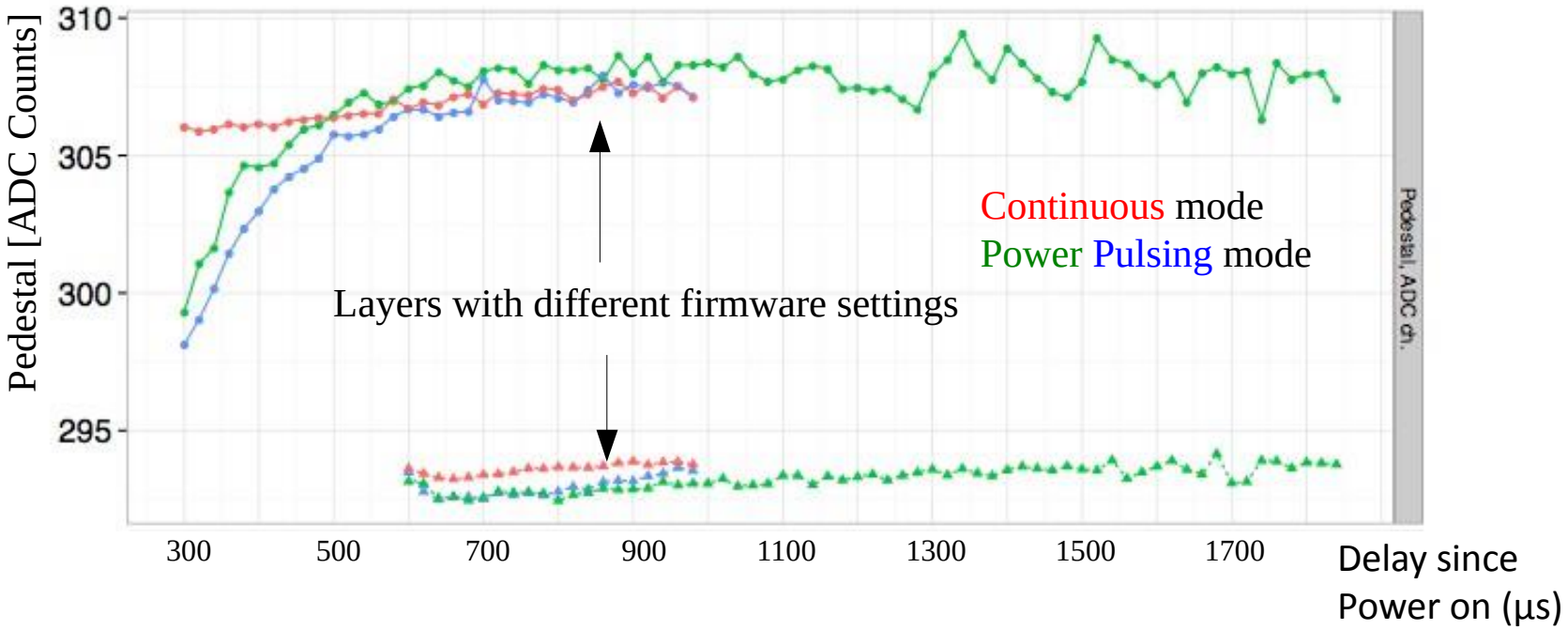
SiECAL group

Power pulsing – “ramp-up” time (reminder)

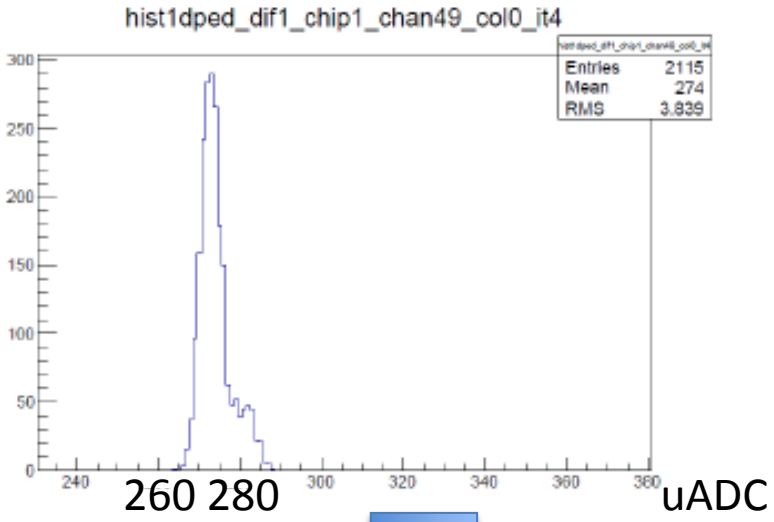
- Analysis of detector response as function of delay between enabling of bias currents and signal arrival



Several channels are merged in this plot

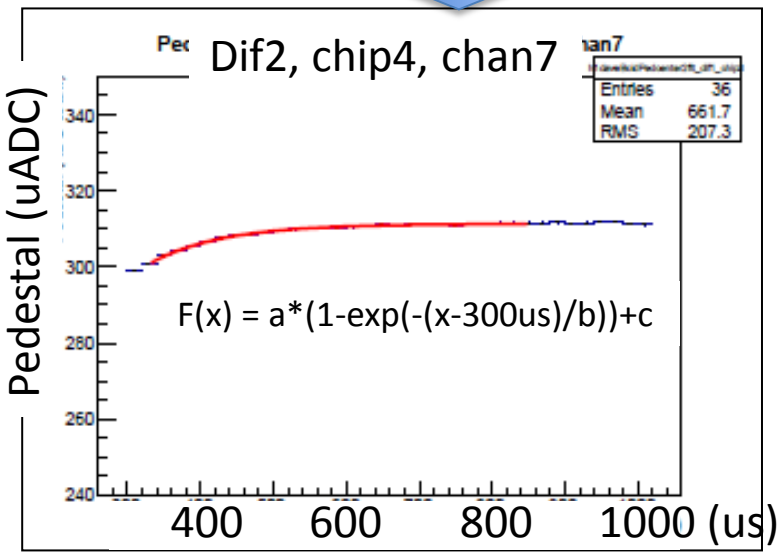
Pedestal position and time constant

- MIP run (run0005, PP)



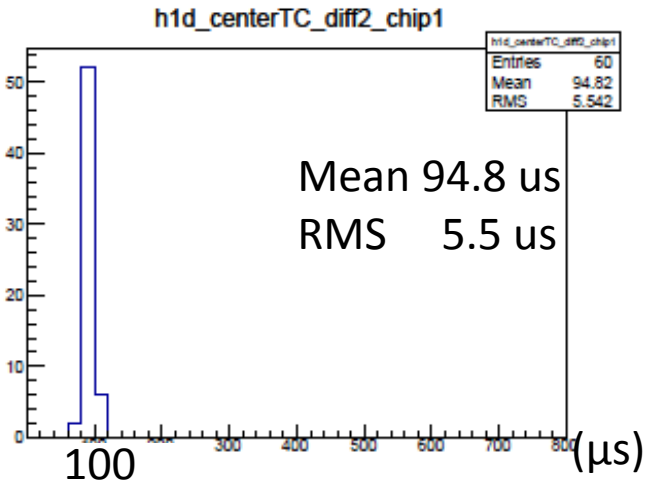
- Make pedestal plots in 20us time window
- Fit pedestal peak with Gaussian (Mean +- 5bin)

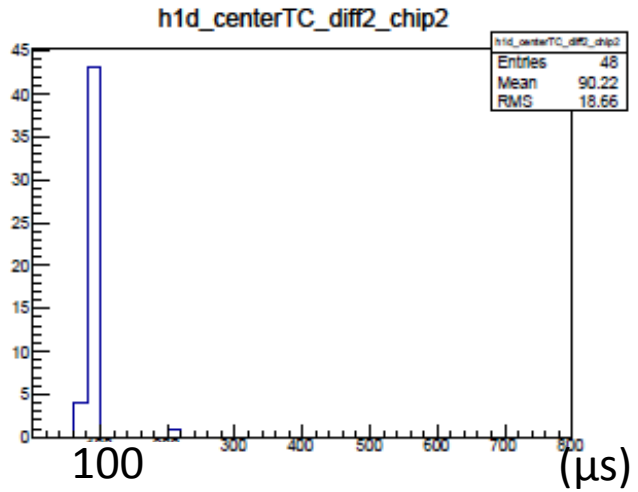
- Fit the plot of pedestal vs time with F(x) = a*(1-exp(-(x-300us)/b))+c

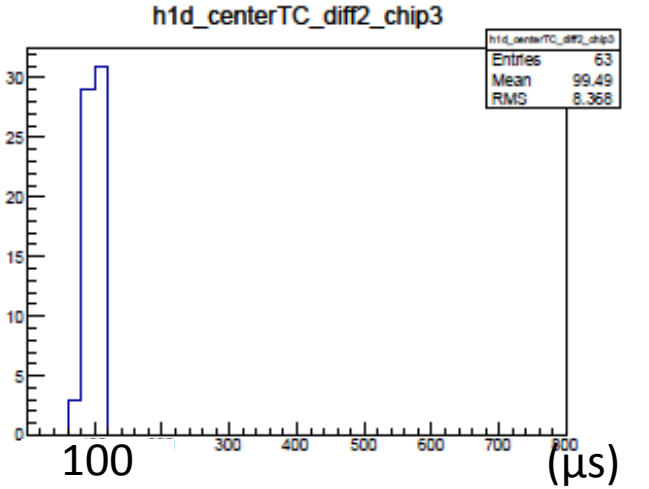


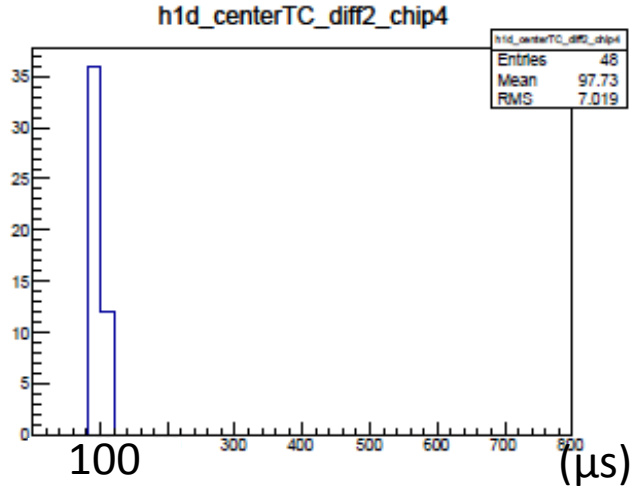
Time constant of pedestal center value of all channel in a slab

- MIP run (run0005, PP), all active and fitted channels



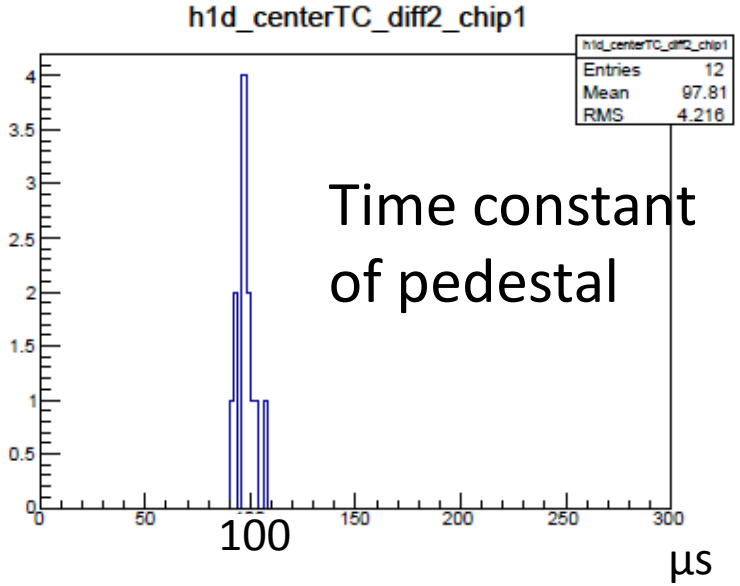


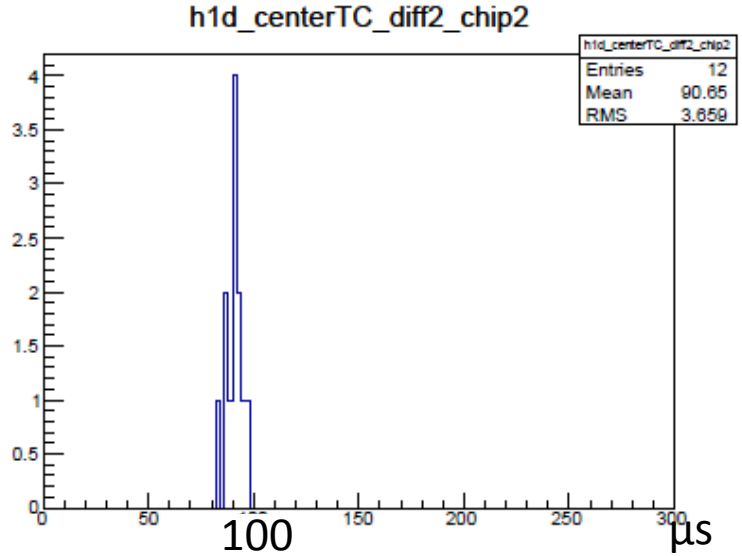


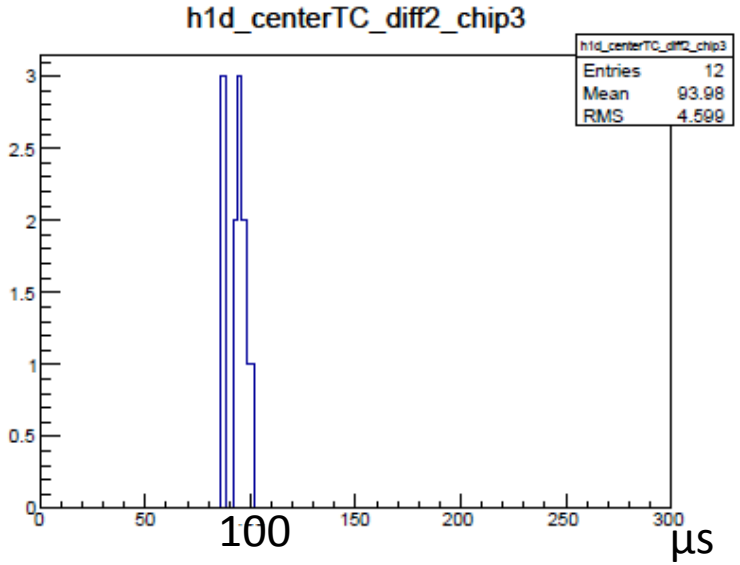


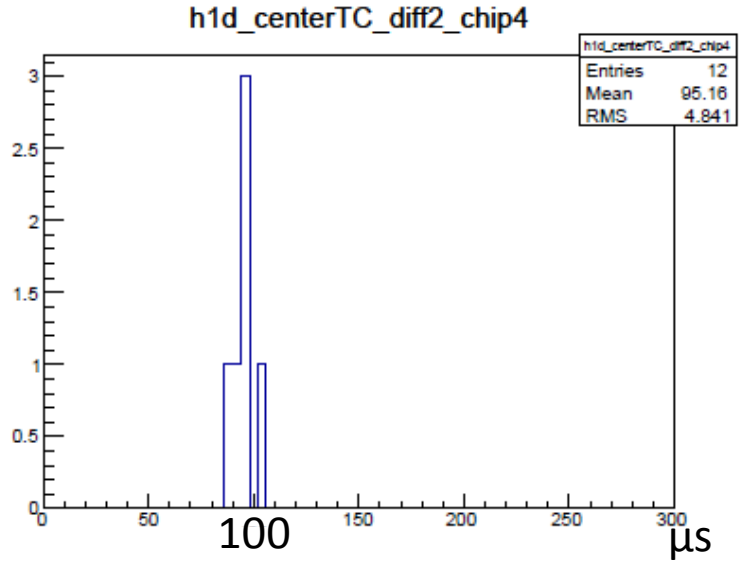
- Time constant is distributed around 100 us

Run by Run difference : Channel 12



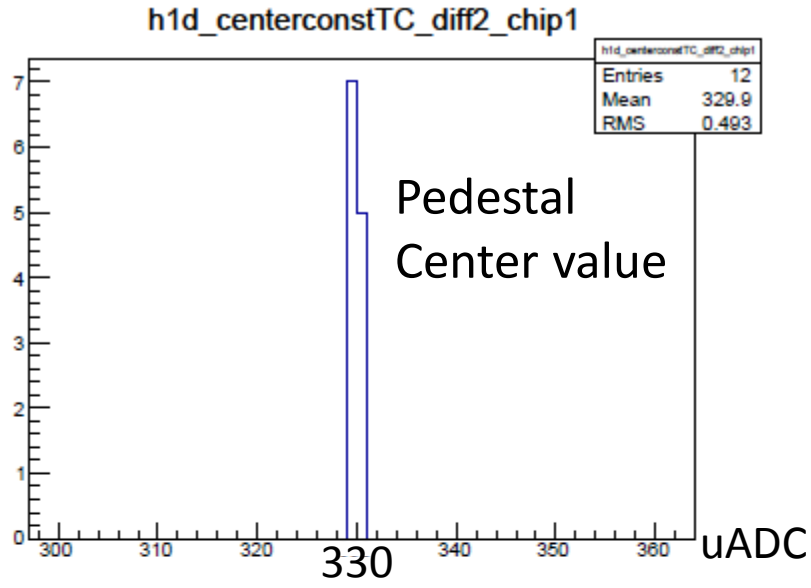


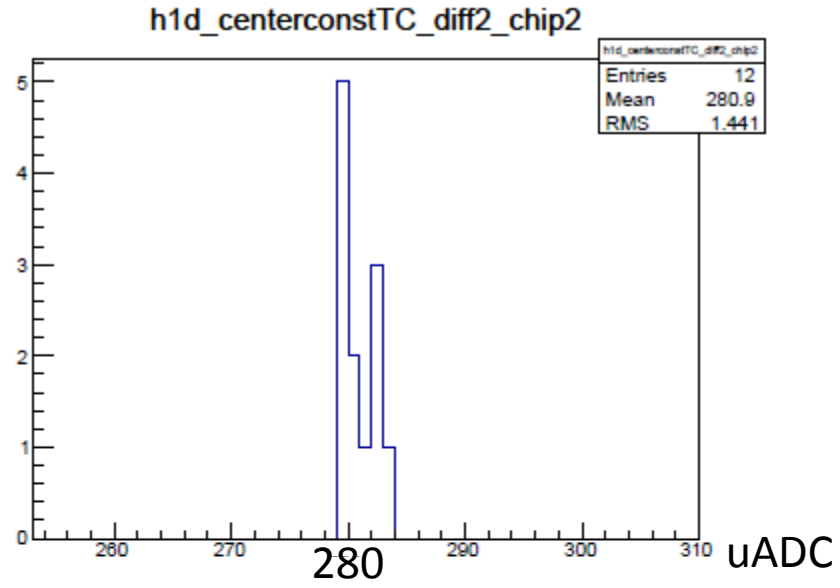


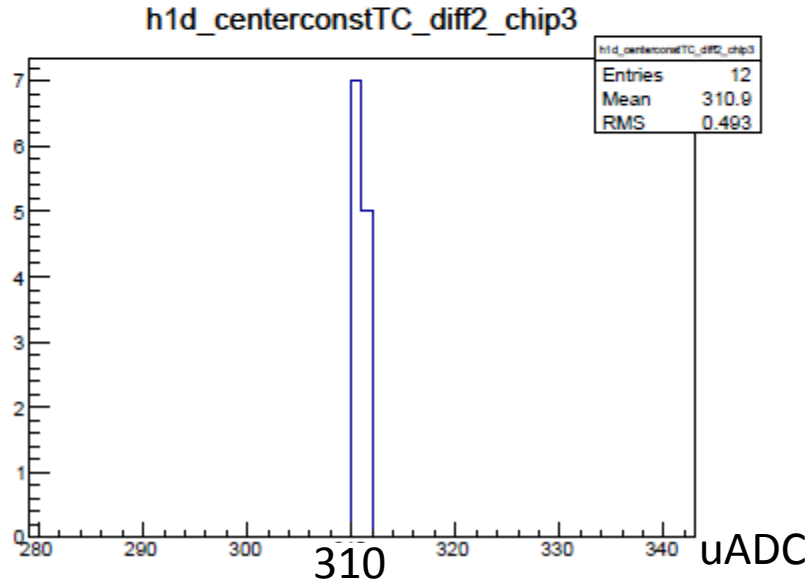


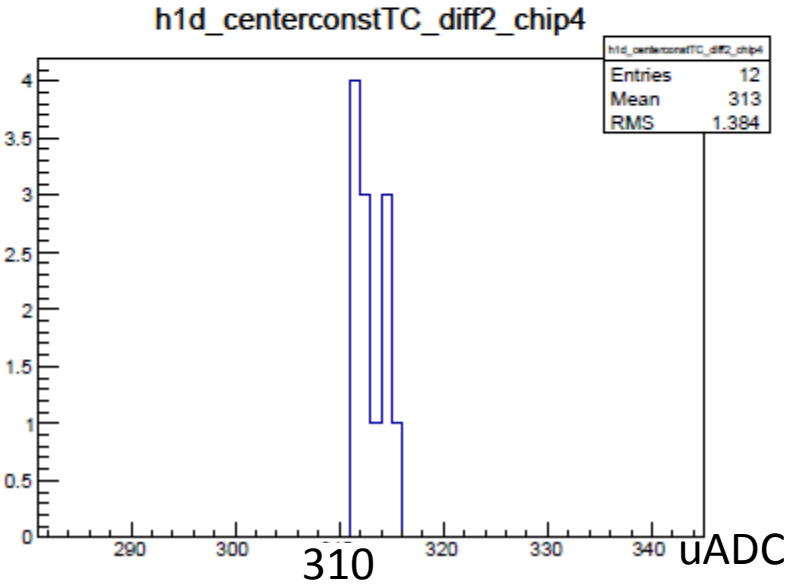
- Fitting errors are 2-6 us
- Ramp-up time is stable (~100 μs)

Run by Run difference : Channel 12







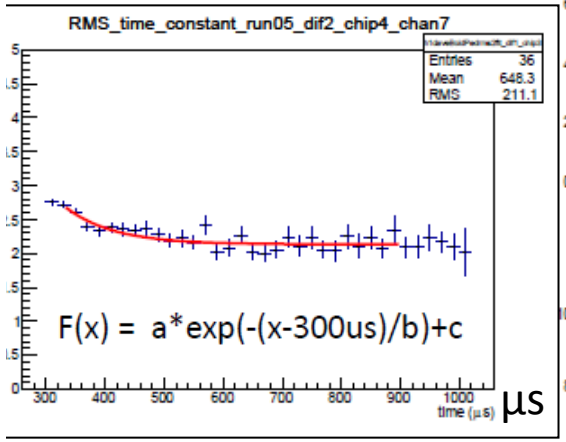


- Activity of digital lines increases a fluctuation of pedestal position

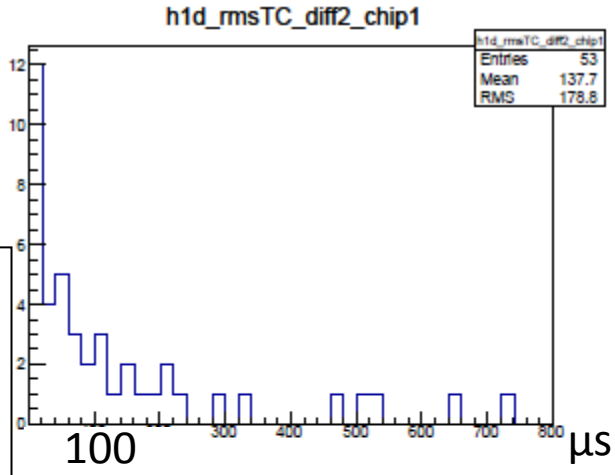
Time constant of pedestal width

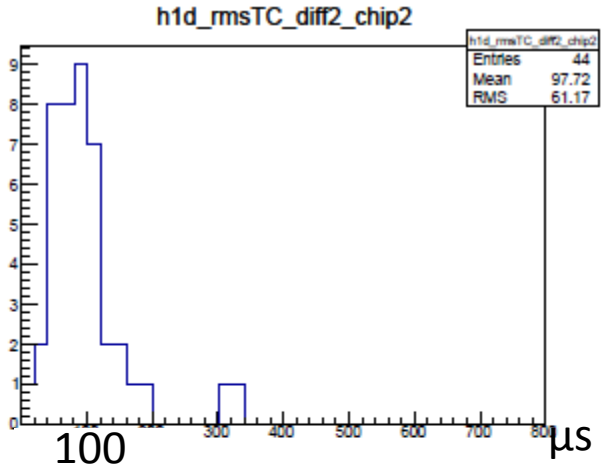
- MIP run (run0005, PP), all active and fitted channels

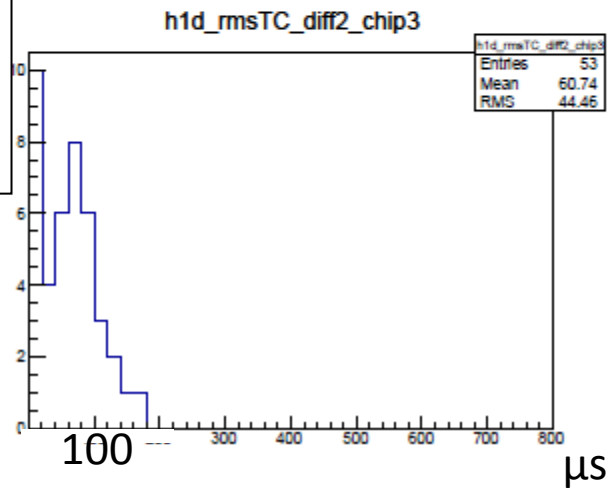
20 us time window

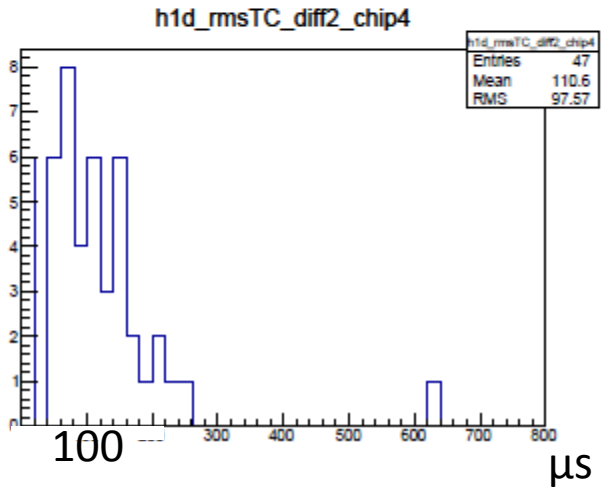


Pedestal width (uADC)





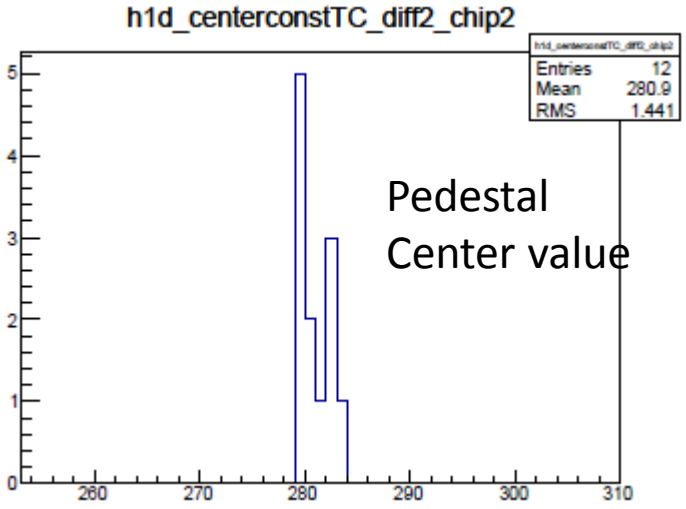


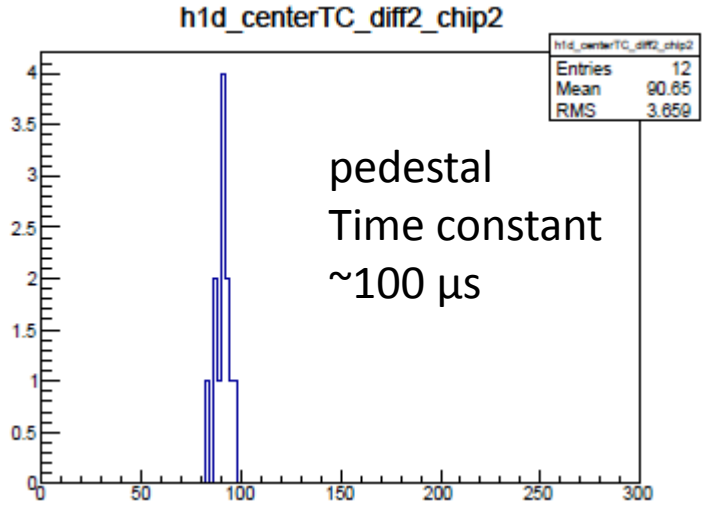


- If we use a single run,
  it is difficult to estimate a time dependence of pedestal width

Summary

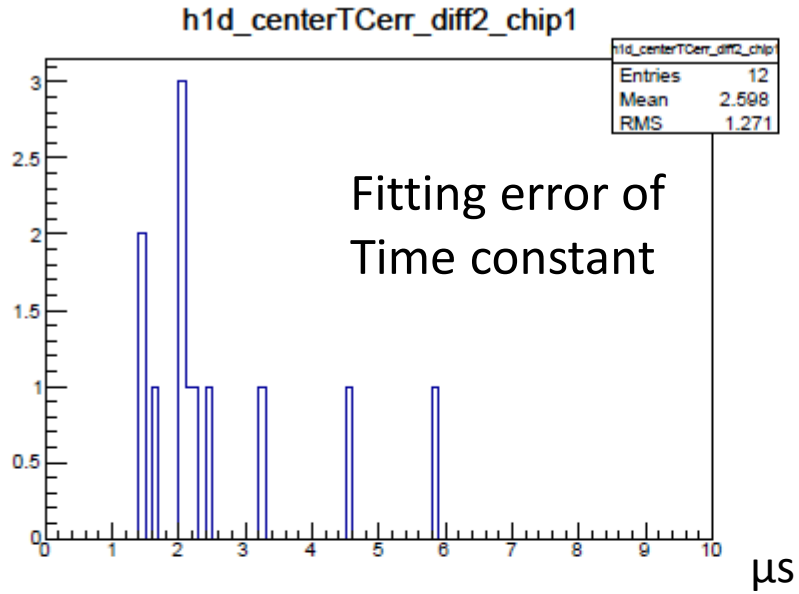
- Checked the run by run fluctuation of pedestal position
- Data taken under Power Pulsing operation
- Fluctuation of pedestal position is increased by activity of digital lines
- Ramp-up time is stable (~100 µs)
- Ramp-up time probably can be estimated from the structure of circuit

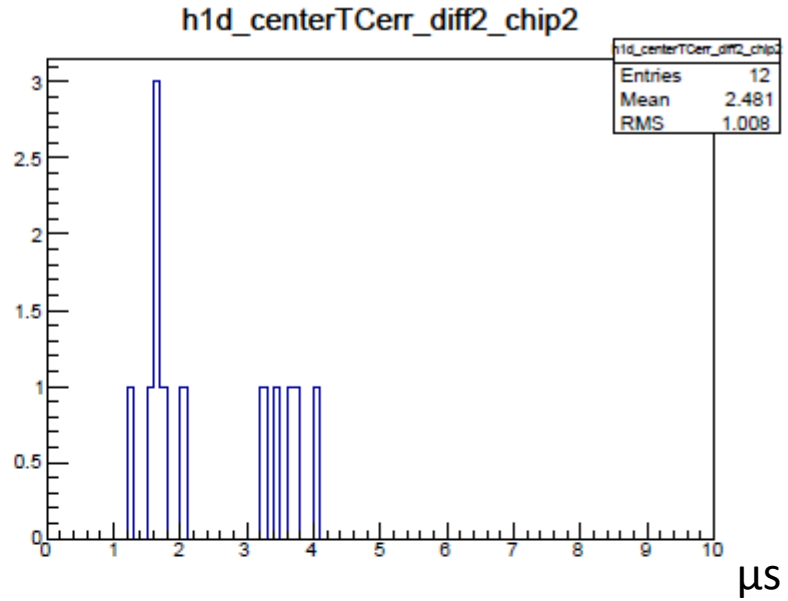


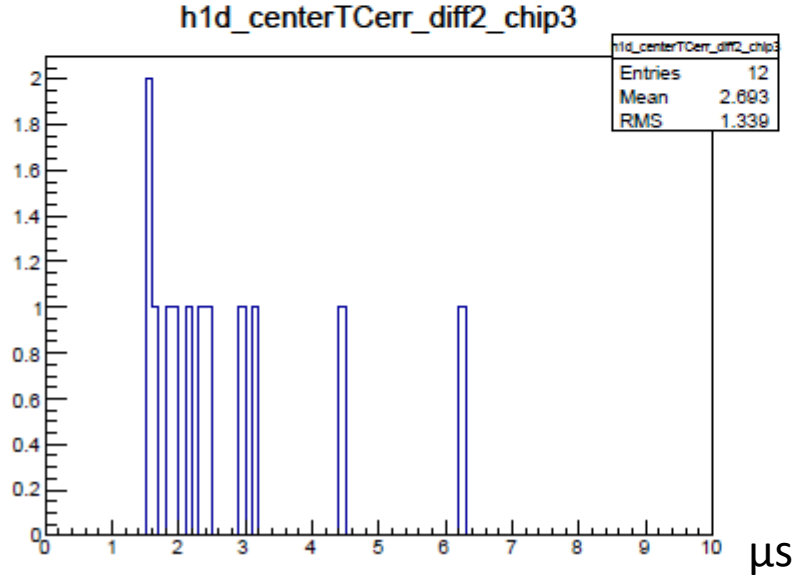


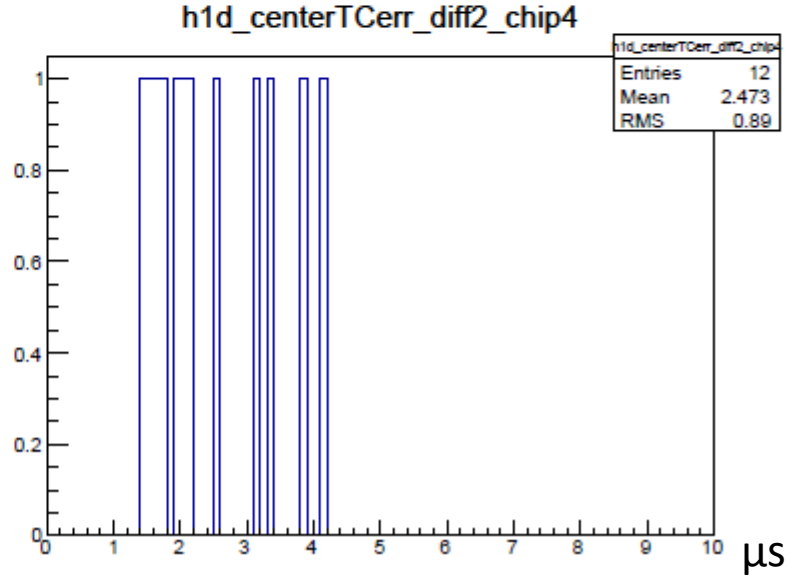
Backup

Run by Run difference : Channel 12





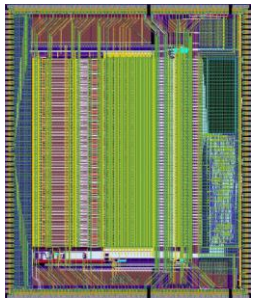




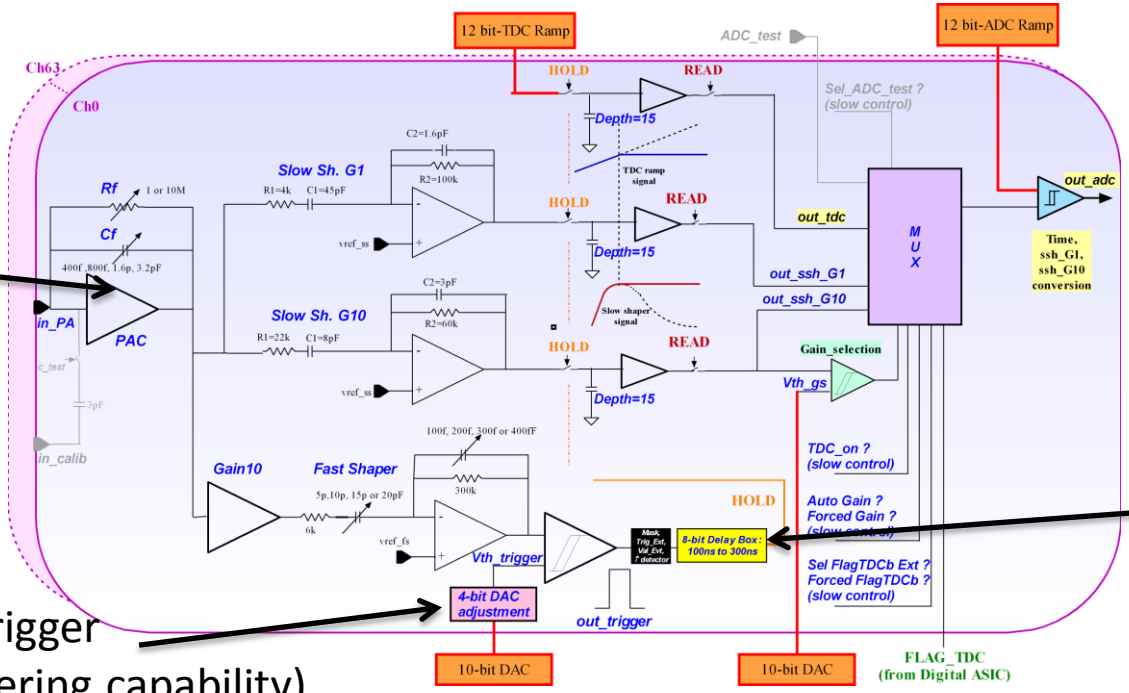
Front end electronics: SKIROC

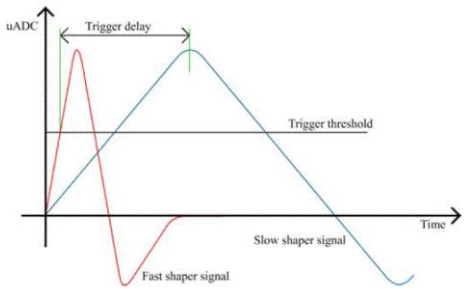
SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- Size 7.5 mm x 8.7 mm, 64 channels
- Variable gain charge amp, 12-bit Wilkinson ADC, digigal logic
- Large dynamic range (~2500 MIPs), low noise (~1/10 of a MIP)
- Auto-trigger
- Low Power: (25 µW/ch) power pulsing



Preamplifier





Trigger delay

Internal trigger
(self-triggering capability)

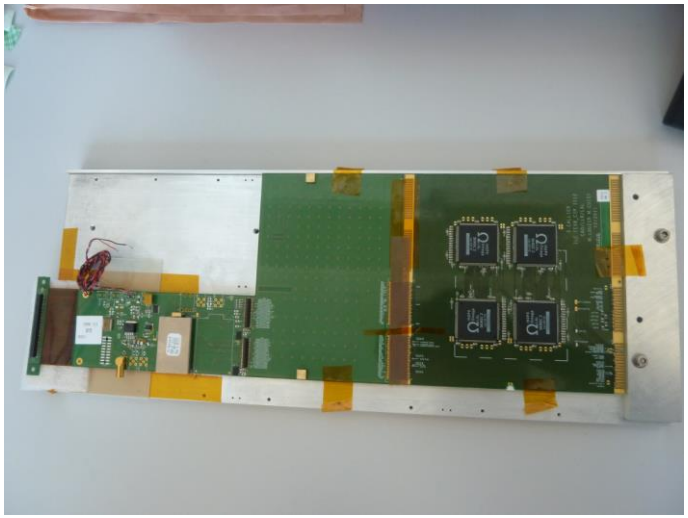
Test beams with fabricated layers

Layer design for beam tests

Integrated FE electronics

Conservative ASU design for beam test

- 1 Si Wafer with 256 pixels of 5x5 mm2 and thickness of 325 µm
- Wafer glued onto PCB
- 4 ASICs in PQFP package
- Up to 10 layers



Test program

- 2012: Commissioning
  - Test of highly integrated electronics in continuous power mode
- 2013: Test of power pulsing
  Test in magnetic field