

SiW ECAL status and plans

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Analysis

- “Interactions of Pions in the CALICE Silicon-Tungsten Calorimeter Prototype” (Naomi van der Kolk, LAL/LLR), in CALIE editorial board
- “Study of the response of the CALICE Si-W ECAL Physics Prototype to positrons using data taken at the Fermilab test beam facility”, (Yohei MIYAZAKI, Kyushu), new CALICE note, first presented at LCWS'13

Hardware

- Technological prototype, mostly funded by ANR grant (~ 330 kEUR, prolonged to Sep 2014) except wafers. 4 beam tests in 2012-2013 in DESY with 1-5 GeV electrons.
- LDA is substituted by GDCC, bug fixes in DIF/LDA-GDCC firmware. Lost packets rate $\ll 1\%$.
- power pulsing works, pedestal stabilizes during 600 usec, S/N is worse for first few msec. S/N improves for higher SKIROC gains
- new “distributed” DAQ **software**, quasi-online monitor GUI, SKIROC configuration GUI, automatic channel masking, emacs org-mode as run control GUI?
- routine cosmic runs: 5 msec timeout (bug) was fixed in DIF firmware, rate = 2 Hz / slab, ~ 700 muons per pixel in 24 hours, $\sim 4\%$ spread of MPV for MIP, perfect uniformity
- infrared laser setup with detachable Si sensor (contacts with springs, without glue), measurement of boundary pixel–guard ring cross-talks : 0.4-0.5% per periphery side
- analysis of per channel scans for 2 slabs is ongoing, a few interesting effects found
- 1-3 MeV e^- PHIL accelerator at LAL can mimic high energy showers

SKIROC configuration tool

Full control of 4 SKIROCs in one ASU. Plan to extend to many ASUs.
Currently in Ruby + GTK.

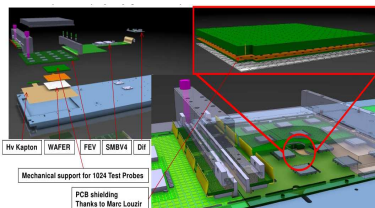
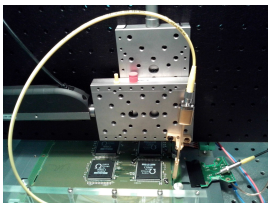
The screenshot displays the SKIROC configuration tool interface. At the top, there is a menu bar with options like 'Choose chip', 'Show descriptions', 'File: /home/balagura/c/ecal/skiroc/config/example4skiros.txt', 'To terminal', and 'Save As ...'. Below the menu bar, there are several columns of configuration parameters, each with a 3-bit selector (0, 1, 2, 3) and a description. The parameters are organized into groups: EC (Error Correction), EN (Enable), GC (Gain Control), and PP (Post-Processor). Below the parameter lists, there are several input fields for specific values, such as 'GC: Capacitor PA Comp' (200), 'GC: DAC0: Trigger' (0), 'GC: DAC1: Gain Select' (0), and 'GC: Delay_Trigger' (130). At the bottom, there are four tables for 'DA: 4-bit DAC Threshold Adjustment', 'PA: PreAmp, In_calib & I_leakage', and 'TM: Trigger Mask'. Each table has a grid of 8x8 cells with numerical values, and some cells are highlighted in red or yellow to indicate specific settings or warnings.

Still to be improved

- even with decoupling capacitors, retriggers in BX+1, BX+2, ...
in $\leq 50\%$ of events
- debugging tools are needed if something goes wrong
- problems with initial configuration (due to slab + DIF and never due to SKIROC in cases when the reason of problem was found)
- $\sim 5\%$ nonlinearity at ~ 1 MIP level
- external trigger (currently only autotriggering)

Infrared laser

... fires in Si detachable sensor in the gap between aluminum contacts



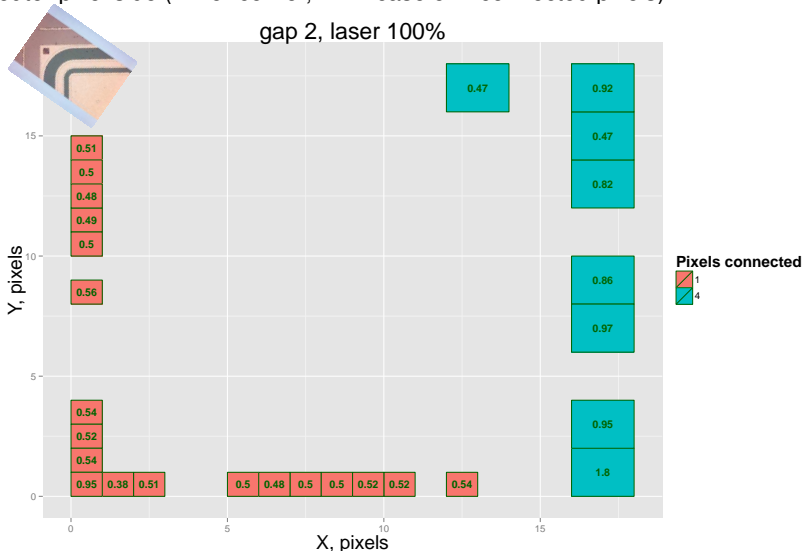
Laser characteristics: $\lambda = 1056 \pm 5 \text{ nm}$, 200 kHz, $< 1 \text{ nsec}$ pulse generates $\sim 700 \text{ MIP signal}$. Intrinsic silicon absorption length at 300 K: $\approx 0.8 \text{ mm}$. Hamamatsu silicon sensor: 16x16 pixels of $5.5 \times 5.5 \text{ mm}^2$, thickness $330 \mu\text{m}$.

In technological prototype Si pixels are glued to PCB with conductive epoxy. For this test a new mechanical setup was designed and produced where sensors may be easily changed. It has up to 1024 **spring contacts** of 5 mm length between pixels and PCB pads.

To be improved: high noises, PCB bending.

Cross talk in percent

Not all springs installed and not all have contacts, about half is operational.
Clear signals in connected pixels. A typical induced signal is $\sim 0.4\text{...}0.5\%$ per outer pixel side (x2 for corner, x2 in case of 4 connected pixels).



New PCB: FEV8 → 9 → 10

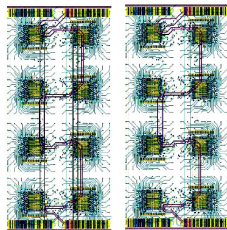
4 → 16 chips per ASU with BGA packaging. **10 first FEV9 are designed and received in LLR**, good flatness <0.5 mm: sufficient to glue flat Si sensor. Many improvements:

- x4 channel density
- 2-3 times shorter signal traces (less input C and pick up noises)
- power decoupling capacitors to reduce noises, correct SKIROC “grounding”: to stabilized 3.3 V, swap of digital and analog power supply (bug) is fixed
- signal transmission (esp. clock) over long distances ~ 1.5m, two options in FEV9: snake or straight lines (x2 interconnections), FEV10 will have straight lines.

FEV9 with all components installed (incl. 16 tested SKIROCs) is ordered, expected in ~ 1 week.



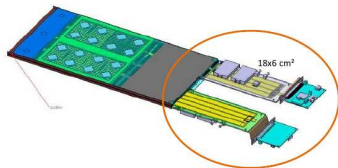
Mechanical model, no chips



Straight and snake lines

Next steps

- SMB4 design (between ASUs and DIF) has started: with power distribution for many ASUs and with special drivers for signal propagation along long lines.



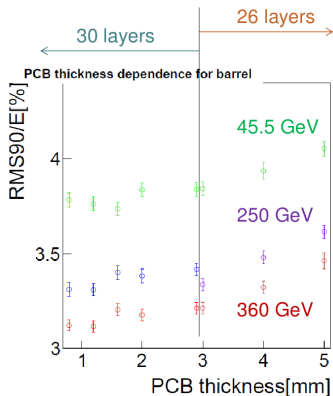
- U-type short slab production
- Physics tests (cosmics, laser, PHIL?)
- Long slab production
- **Goal:** produce ≥ 1 long and short slabs to fill one tower in full scale mechanical prototype. Possibly reuse existing 1/4 ASU short slabs. With GEANT4 simulation, find their affordable fraction in the tower.

- Test at CERN in 2015.

In parallel, look at boards integration in ILD.

ECAL thickness

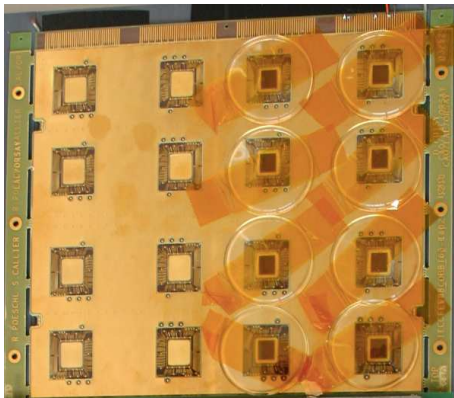
Jet energy resolution does not depend on PCB thickness below 3 mm (Tokyo Uni group study, supervised by D.Jeans)



Currently: PCB + BGA SKIROC thickness = 3.15 mm.
BGA thickness may possibly be reduced by 0.3 mm.

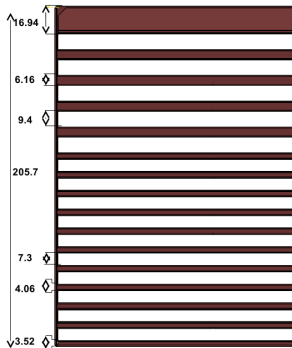
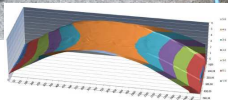
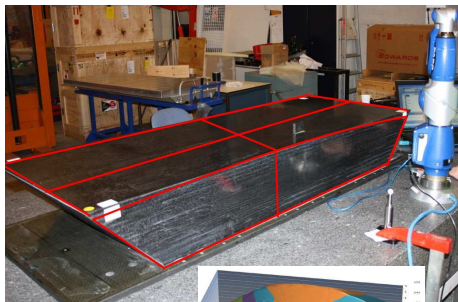
Chip-On-Board PCB in LAL

Only 1.2 mm thick, 8 naked die chips wire bonded.



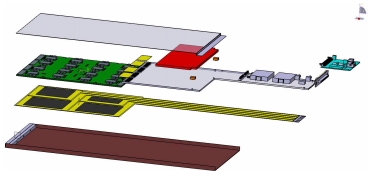
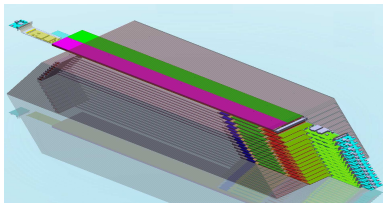
Status: two productions, ≥ 1.2 mm bending prevents gluing Si.

Existing mechanical structure

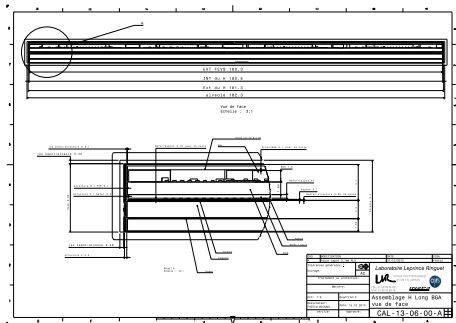


Prototype: 3/5 of one module, ~ 600 kg. Separately built layers “cooked” together. Simulated mechanically & thermally.

U- and H-shape slabs: plans

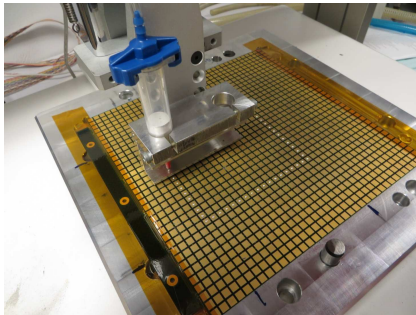


Fill alveolas with 14 U-shape short slabs (top right) + 1 H- (bottom right) or U-shape long slab without or with W. If without: possibility to glue (and then detach) W to slab from Si side and insert to alveola.



Gluing in LPNHE

- 9 sensors were glued by robot



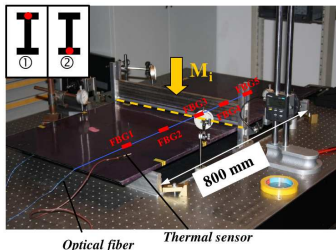
Next steps:

- second robot for positioning and aligning
- glue 4 sensors on PCB with 100 um gaps
- prepare technology for mass production

Prototype with molded Bragg grating fibers

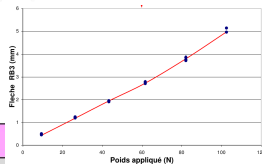
Detailed verification of simulated elongations under loads (by monitoring frequency shift of light reflected by fiber).

Details on first measurements:
<http://indico.cern.ch/event/274076/>,
 French IRFU Linear Collider Days, Nov'13.



Correlation with the experimental data (FBGs):

	Load (N)	ϵ_{yy} FBG1 ($\mu\text{m/m}$)		ϵ_{yy} FBG2 ($\mu\text{m/m}$)		ϵ_{yy} FBG3 ($\mu\text{m/m}$)		ϵ_{yy} FBG4 ($\mu\text{m/m}$)		ϵ_{yy} FBG5 ($\mu\text{m/m}$)	
		Exp.	Simu.	Exp.	Simu.	Exp.	Simu.	Exp.	Simu.	Exp.	Simu.
M1	9,38	-2,52	14	-12,6	-12,2	-29,86	-36,8	-7,41	-8,1	4,91	29
M2	26,35	0,84	27,8	-32,77	-30,6	-92,9	-100,7	-24,72	-26,5	15,55	42,51
M3	43,32	10,92	41,1	-53,78	-49,1	-156,77	-165,6	-39,55	-44,9	26,2	55,8
M4	61,64	21,01	55,4	-78,16	-69	-235,57	-237	-59,33	-64,8	31,11	70
M5	82,08	33,61	71,5	-109,26	-91,4	-336,77	-319,6	-79,93	-87,1	44,21	86,2
M6	102,53	48,74	87,4	-145,4	-117,7	-468,66	-413,7	-115,37	-112,8	58,13	102,2

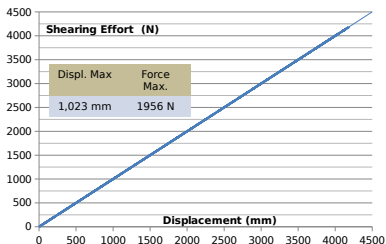


Vérification des paramètres du modèle en comparant la flèche FBG3 mesurée et simulée

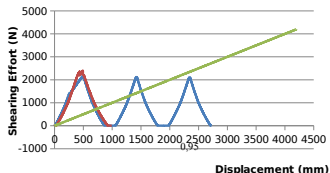
Endcap shearing tests in LPSC

Monotonic and destructive charge/discharge (hysteresis) tests

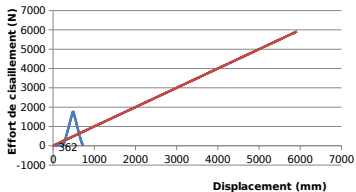
Monotonic shearing test



Fatigue + Progressive shearing cycles



Progressive shearing cycles



Conclusions

- LDA → GDCC, improvements in DIF/GDCC firmware, \ll 1% packet loss rate. More robust configuration
- Power decoupling capacitors helped against retriggerings / plane events, still to be improved
- Power pulsing works, with only slightly higher noises
- Calicoes DAQ + other software tools
- Cosmic calibration with 5% accuracy per channel in one day is demonstrated
- Setup with spring contacts + laser: first measurement of capacitive guard ring cross talks
- Promising verifications of mechanical simulations with Bragg fibers
- FEV10 design is fixed
- 9 sensors glued by LPNHE robot
- New shearing tests of endcaps in LPSC

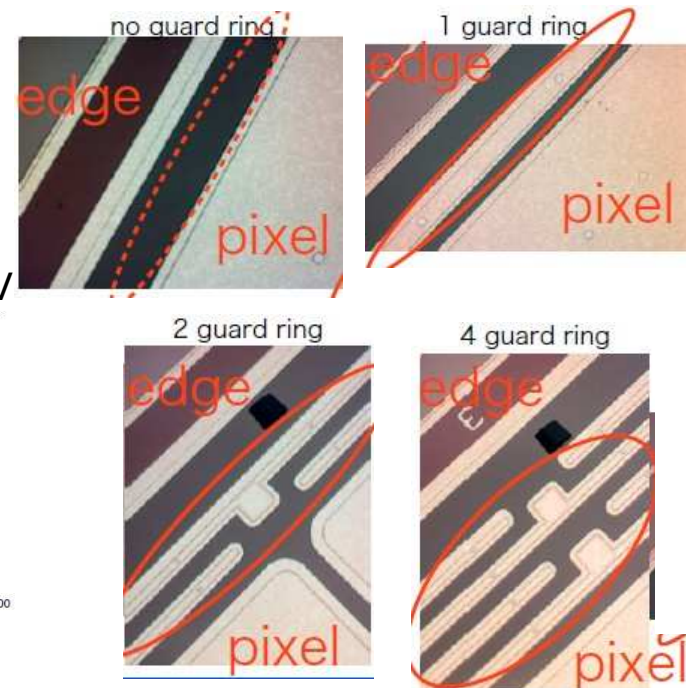
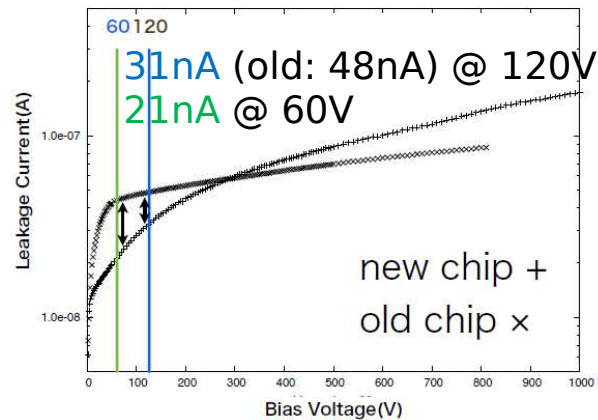
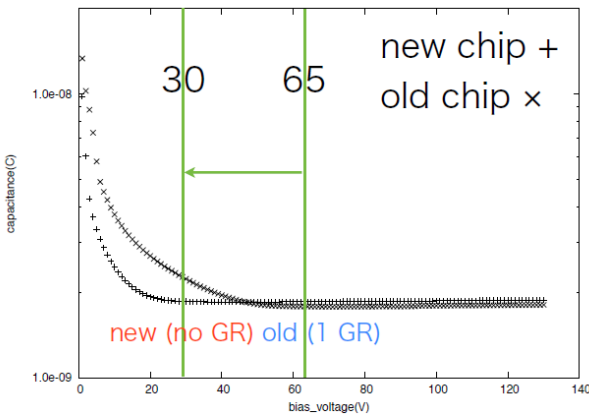
Plans

- Test new PCB FEV9 with BGA packaging
- Design new adaptor board SMB4 for long slab
- Test gluing 4 sensors to PCB with 100 um gaps, positioning and alignment robot in the future
- Produce U-type short slabs with FEV10, test them, then produce ≥ 1 long slab
- Physics tests: charge injection, cosmics, laser, possibly PHIL accelerator
- Equip with detectors one tower of full scale prototype and test at CERN beams (2015)
- Endcap mechanics in LPSC, rails, cooling
- Possibly, test silicon sensors from other producers

Plans in Kyushu University ...

Si Sensor R&D

- R&D to decide the sensor design and specification.
 - 4 guard ring types
 - Measurement of basic properties (I-V, C-V)
 - measurement of sensor response with Infra-red laser
- We plan irradiation tests (γ , n) for the latest model Si sensor



Analysis of Physics Prototype TB

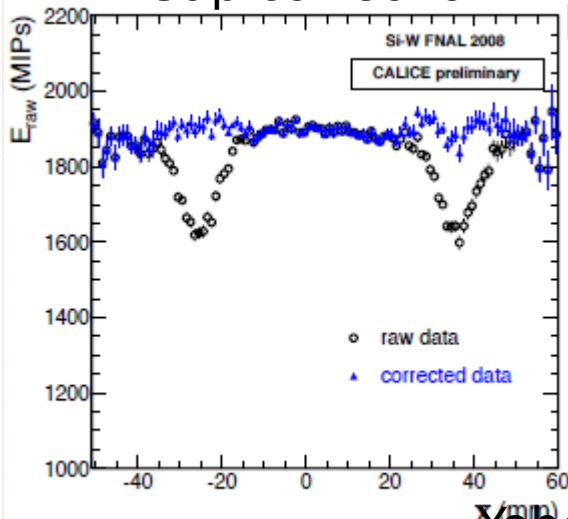
- The performance of SiWECAL physics prototype to positron beam
- Positron data taken at FNAL in 2008
- Simulation is needed to estimate systematics of beam momentum

Energy resolution

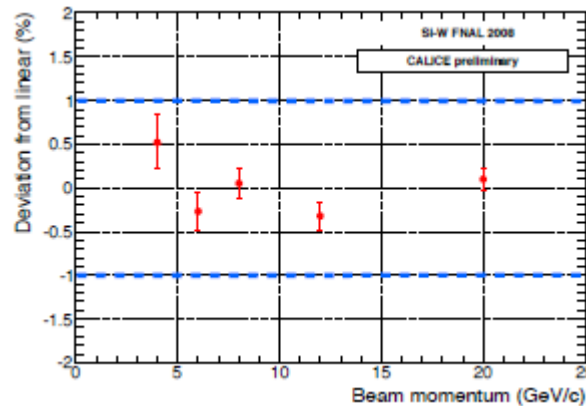
stochastic term $16.67 \pm 0.30(\text{stat.})^{+0.07}_{-0.44}(\text{syst.})\%$

constant term $1.75 \pm 0.24(\text{stat.})+0.39(\text{syst.})\%$

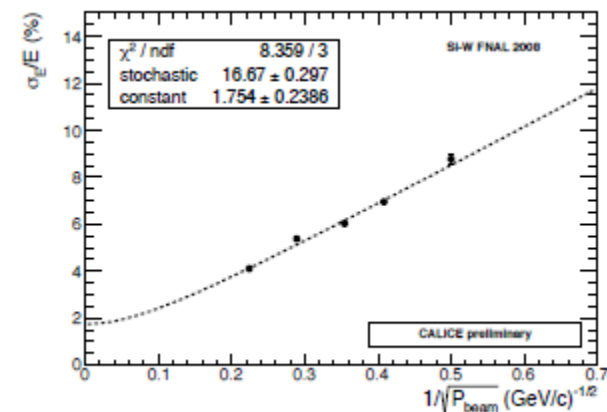
Gap correction



Deviation from linear response

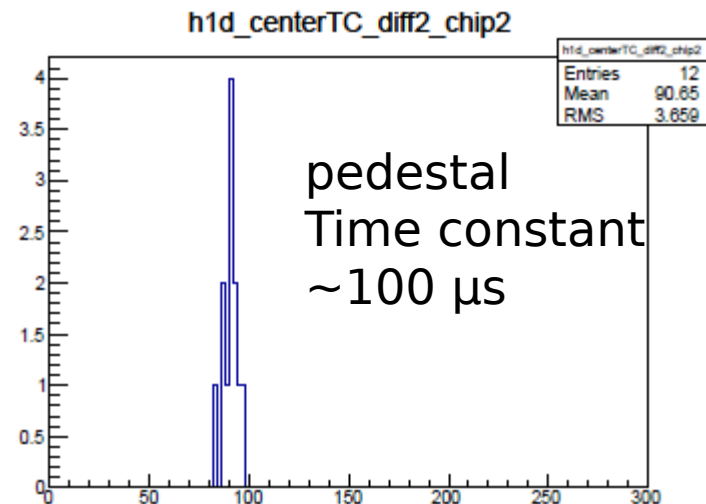
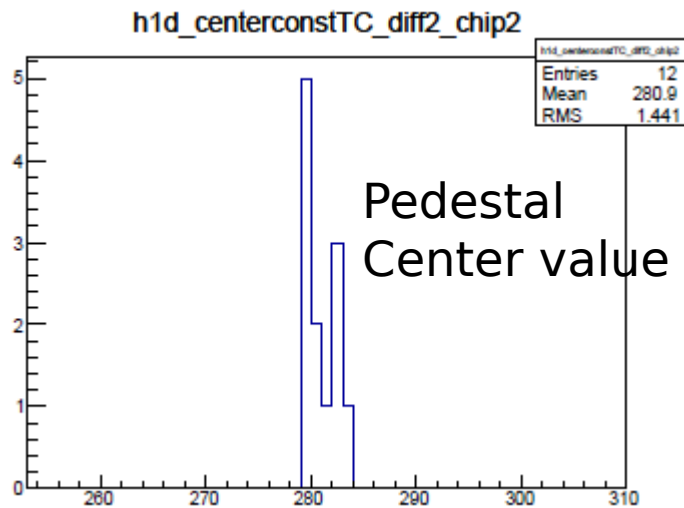


Energy resolution



TB analysis

- Run by run fluctuation of pedestal position
- Data taken under Power Pulsing operation
- Fluctuation of pedestal position is increased by activity of digital lines
- Ramp-up time is stable ($\sim 100 \mu\text{s}$)
- Ramp-up time probably can be estimated by circuit simulation



DAQ development @ Kyushu

1. Importing SiECAL DAQ to Kyushu
 - DIF/Slab(FEV8), LDA from LLR
 - CCC from DESY (with Remi's check)
 - Calicoes
 - Plan to improve Debug features etc. in Kyushu
 - Will be ready in April or May
2. Test board for BGA SKIROC2
 - Modifying OMEGA test board for QFP SKIROC2
 - Held a meeting with Stephane and our manufacturer in Japan!
 - Will be ready in May or June
3. (Possible) FEV10 production in Japan
4. Combined DAQ for hybrid ECAL