FPCCD VTX R&D Status and Prospects

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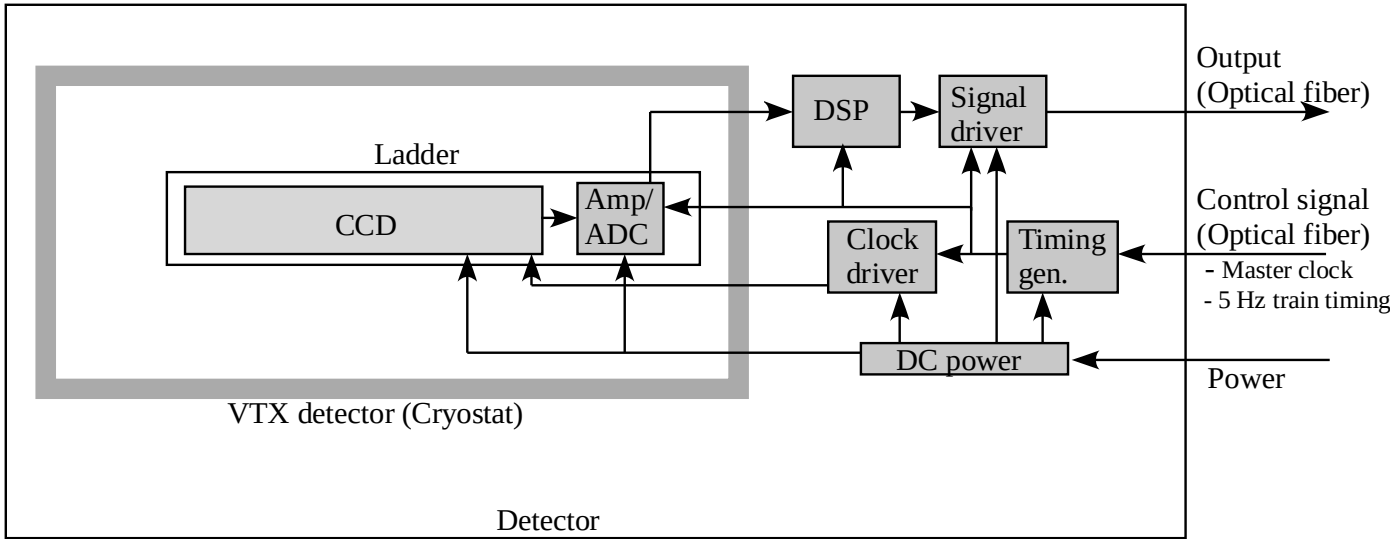
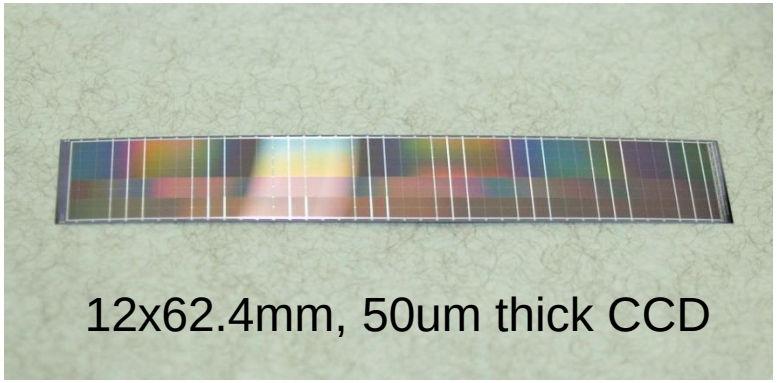
R&D issues

- FPCCD sensor
- Readout electronics
  - Front-end ASIC
  - Peripheral circuit
- Engineering R&D
  - Support structure including ladders
  - Cooling system



FPCCD Sensor

R&D Goal	Achievement	Prospect
Pixel size; 6um → 5um	6um fabricated, under evaluation	5um after ILC approval
Chip size; 1x6.25cm^2 → 2x12.5cm^2	1.2x6.24cm^2 achieved, to be evaluated	2x12.5cm^2 after ILC approval
Chip thickness; 50um	50um achieved for 1.2x6.24cm^2 chip	
Speed; >10Mpix/s	Under investigation → Improved clock circuit needed	New clock circuit/cable in coming 2~3 years
Power; <10mW/ch	Achieved in design	To be verified soon
Radiation tolerance; >1x10^{13}e/cm^2		Neutron irradiation test soon (2014/Oct.)



Readout electronics

R&D Goal	Achievement	Prospect
ASIC speed; >10Mpix/s	OK	
ASIC power; <6mW/ch	OK	
ASIC noise; <30electrons	OK	
3-value clock driver		To be developed in 2~3 years
Low mass FPC		To be developed in 2~3 years
Data compression circuit		To be developed in 2~3 years

Engineering R&D

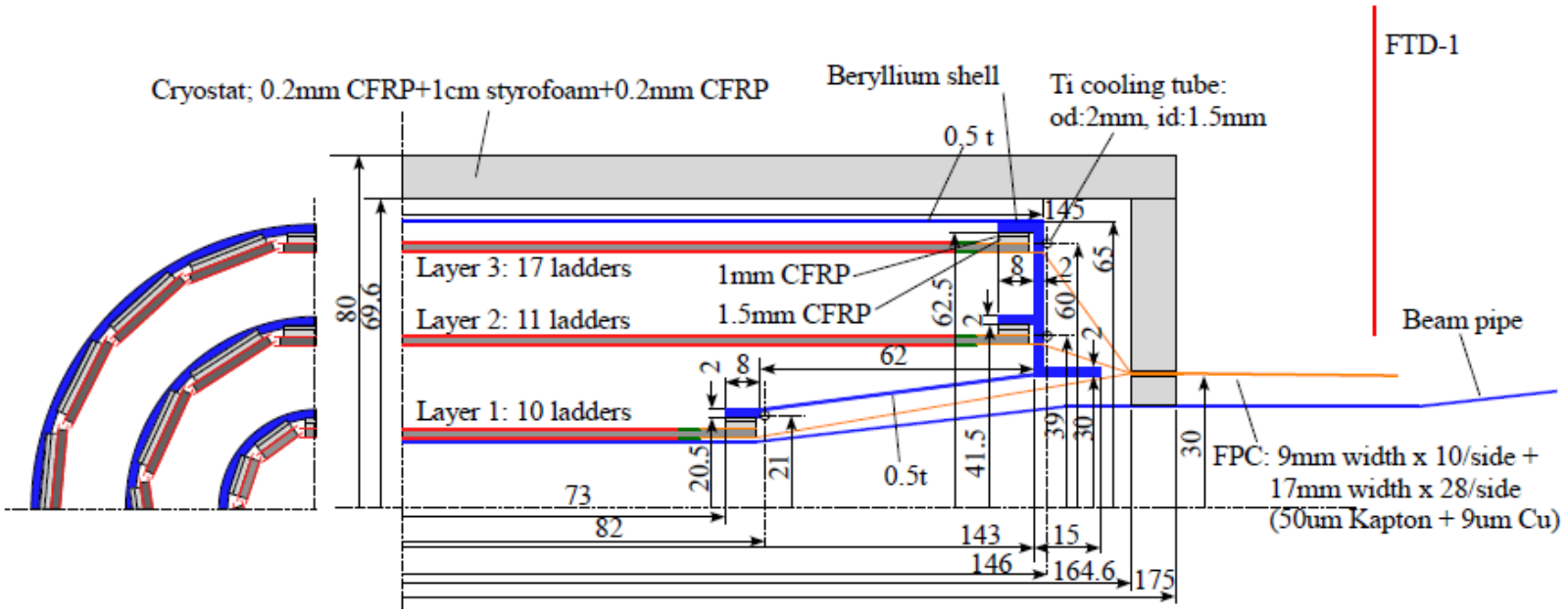
R&D Goal	Achievement	Prospect
Low mass ladder		To be developed in 2~3 years
2-phase CO2 cooling system; −40°C using gas compressor	Principle demonstrated	More stable and practical system in 2~3 years
Support structure		To be developed in 2~3 years
Engineering prototype		To be developed in 3 years

2-phase CO2 cooling system for proof of principle

−40°C here

BACKUP SLIDES

FPCCD VTX


Cryostat; 0.2mm CFRP+1cm styrofoam+0.2mm CFRP
Beryllium shell
Ti cooling tube:
od:2mm, id:1.5mm
0.5 t
FTD-1
Layer 3: 17 ladders
Layer 2: 11 ladders
Layer 1: 10 ladders
1mm CFRP
1.5mm CFRP
Beam pipe
FPC: 9mm width x 10/side +
17mm width x 28/side
(50um Kapton + 9um Cu)
0.5t
80
69.6
145
65
62.5
60.5
62
73
82
143
146
164.6
175
15
41.5
39
30
20.5
21