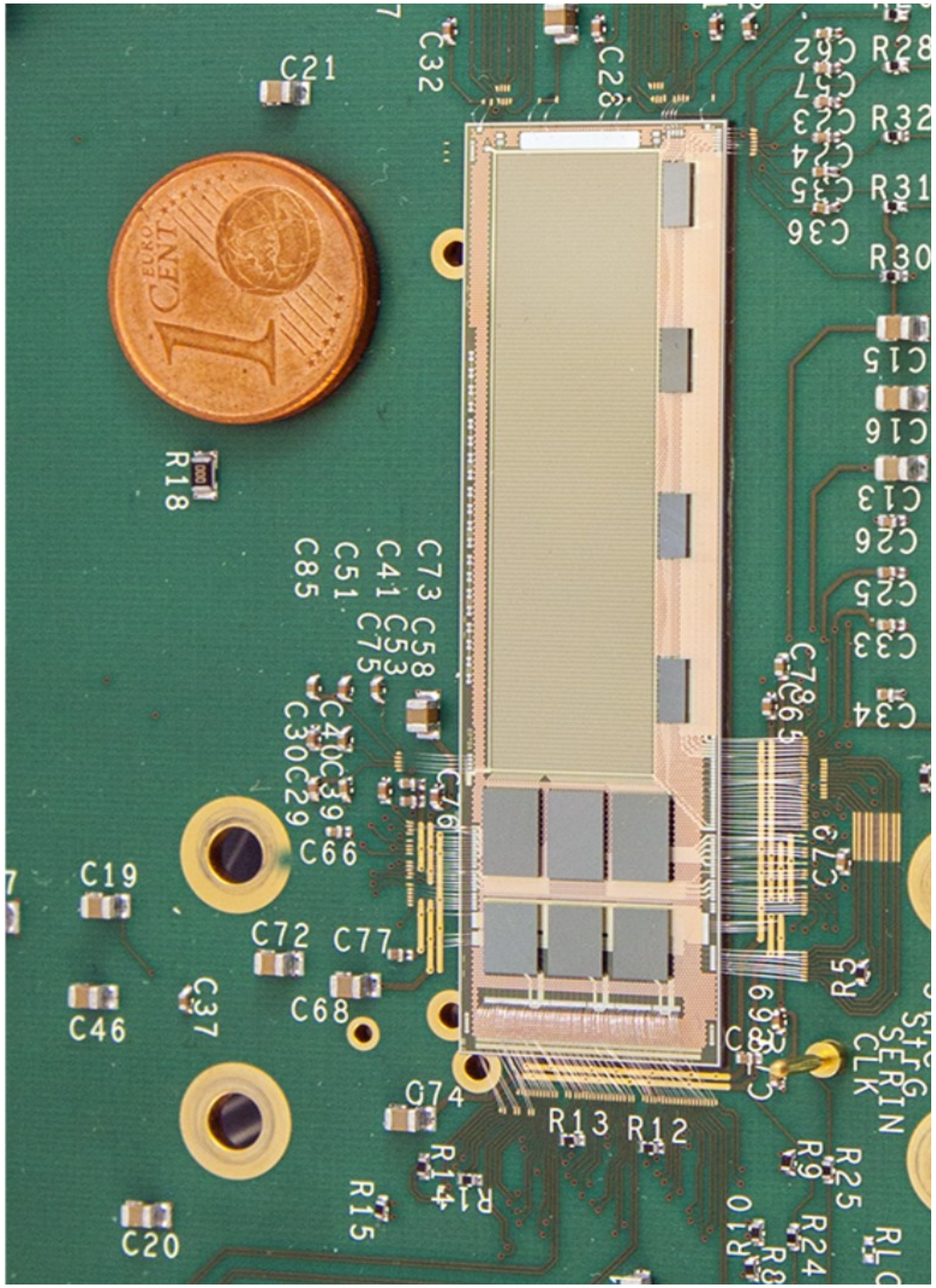
DEPFET vertex detector
&
Forward Tracking Disks



ILD meeting

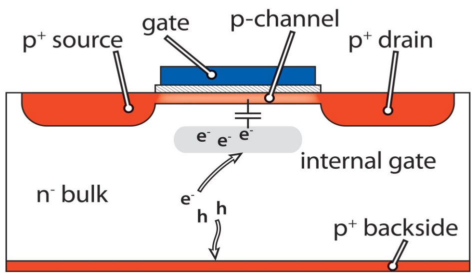
Oshu, Japan, Sep. 2014

Marcel Vos (IFIC Valencia),
for the DEPFET collaboration
and the Spanish LC network

Thanks to F. Arteche, ITA, I. Garcia, IFIC,
I. Vila, IFCA, M.A. Villarrejo, IFIC

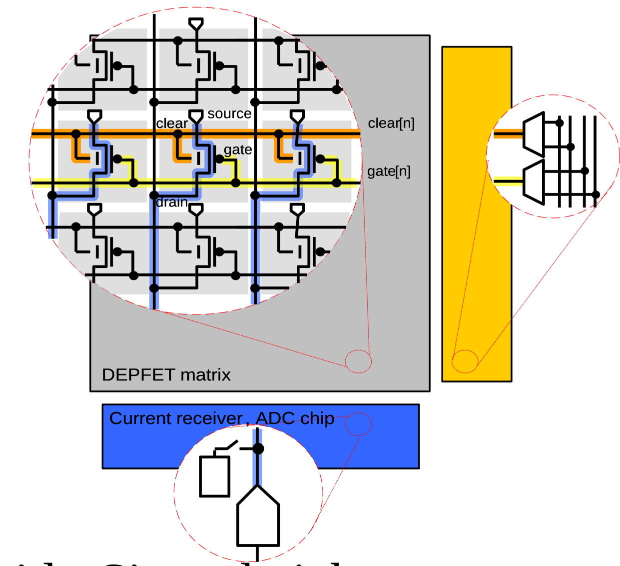
DEPFET

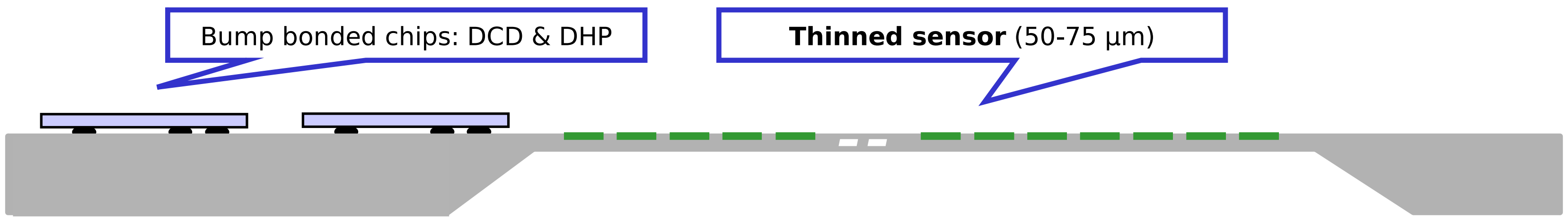
A DEPFET-based (all-silicon) vertex detector ladder



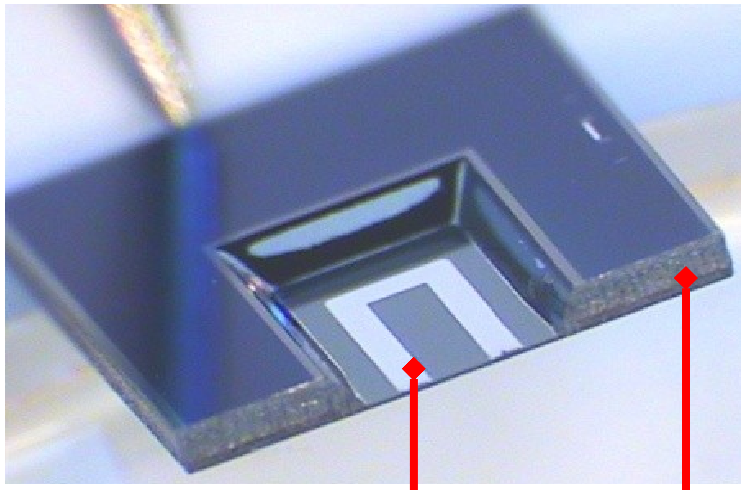
(1) Amplify signal in elementary DEPFET cell (pixel) with FET integrated in detector-grade Si. Drain current is modulated by charged collected on internal gate.

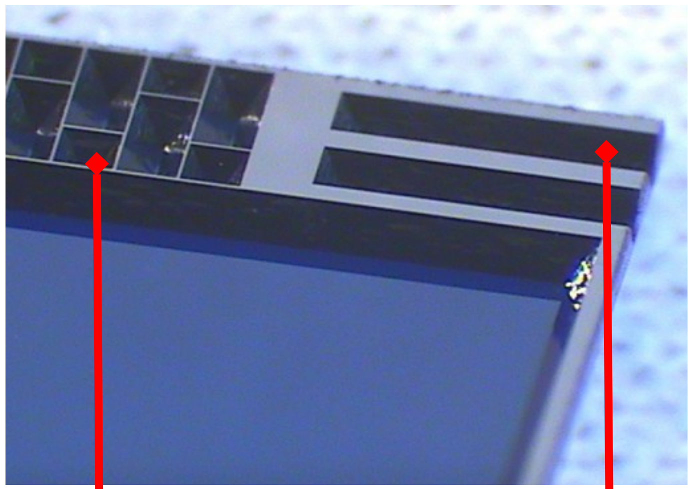
(2) Read out a column of DEPFET pixels with a FE ASIC. Rows are addressed in turn for rolling shutter operation.



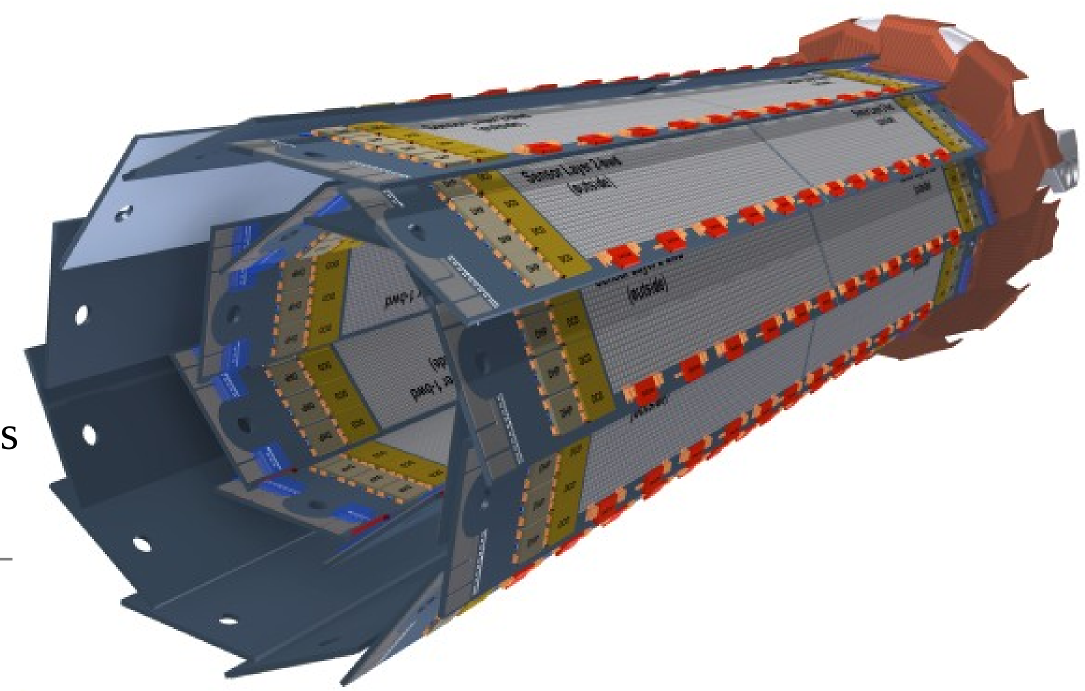


(3) Create an ultra-thin self-supporting Silicon sensor, starting with the ~1 mm thick Si-Oxide-Si sandwich formed by sensor and handle wafer, sculpt away superfluous material by grinding and lithography. Integrate signal and power lines in metal layers on Silicon, bump-bond ASICs directly on top.





(4) Assemble the ladders in a cylindrical structure to form the barrel vertex detector.



Thin sensor (50-75 um)

Thicker rim (500 um)

Structure to glue two half-ladders

Remove every gram that you can get rid off

The DEPFET Collaboration

(DEPFET vertex detector for Belle II and ILC)

www.depfet.org

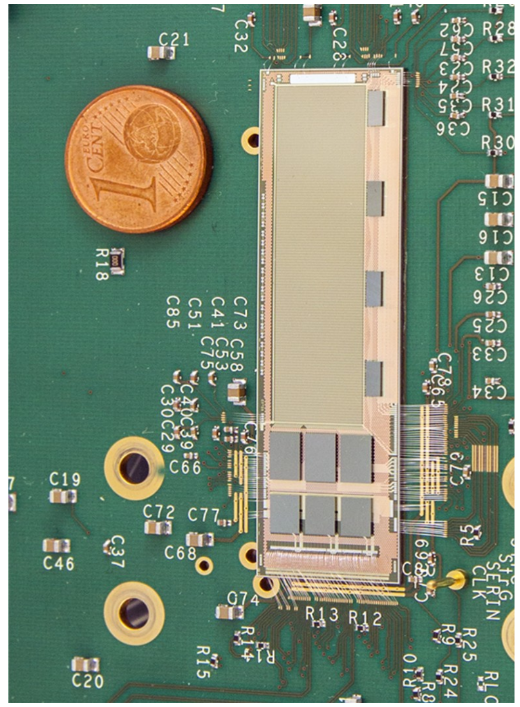
Charles University, Prague
DESY, Hamburg
IFCA, Santander
IFIC, Valencia
IFJ PAN, Krakow
IHEP, Beijing
LMU Munich
MPI, Munich
HLL, Munich
TU, Munich
University of Barcelona
University of Bonn
University of Heidelberg
University of Giessen
University of Göttingen
University of Tabuk

DEPFET R&D time-line

"Early days"

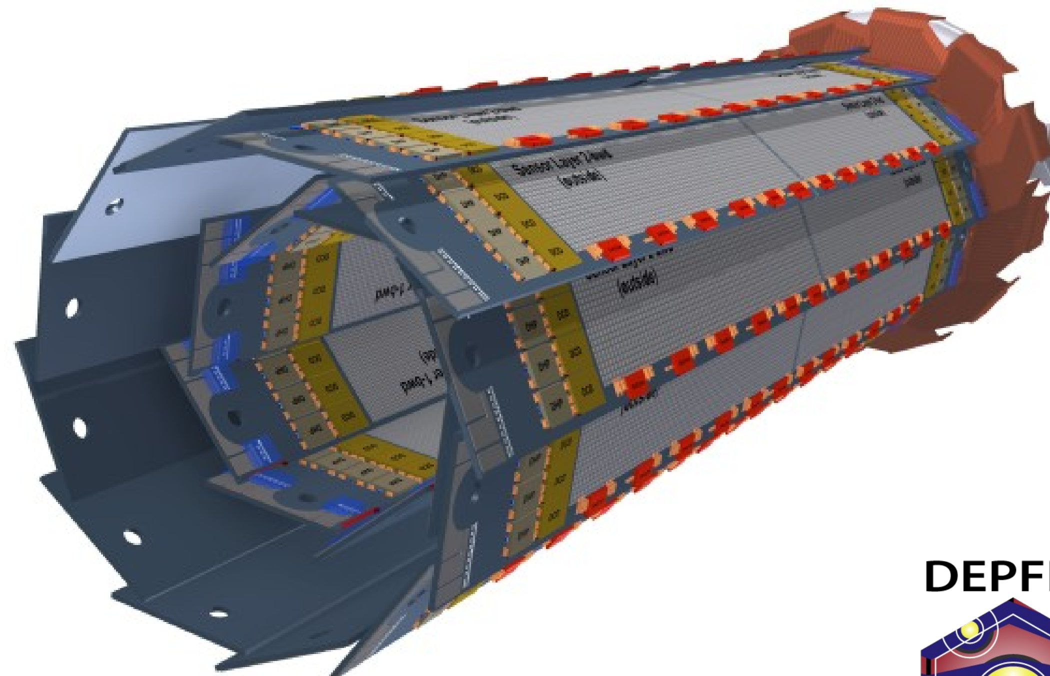
2007-2011 prototypes with $O(10^3\text{-}10^4)$ pixels

"The most complex piece of silicon in the world", our ECFA reviewer



January 2014, first large-scale, multi-ASIC ladder at DESY TB

"a 30-40% ILC prototype"



Installation PXD in Belle II

Belle II upgrade

Proof-of-principle | Complete demonstrator | A real detector | Physics

2002.... | 2007.... | 2013 | 2014 | 2015 | 2016 | 2018

a vertex detector for TESLA

LC-specific detector R&D

Small-pixel prototype with 1.5 µm resolution

DEPFET for ILC, IEEE TNS 60, 2, 2

ECFA review: http://ific.uv.es/~vos/ECFA_DEPFET.pdf

Beyond Belle II

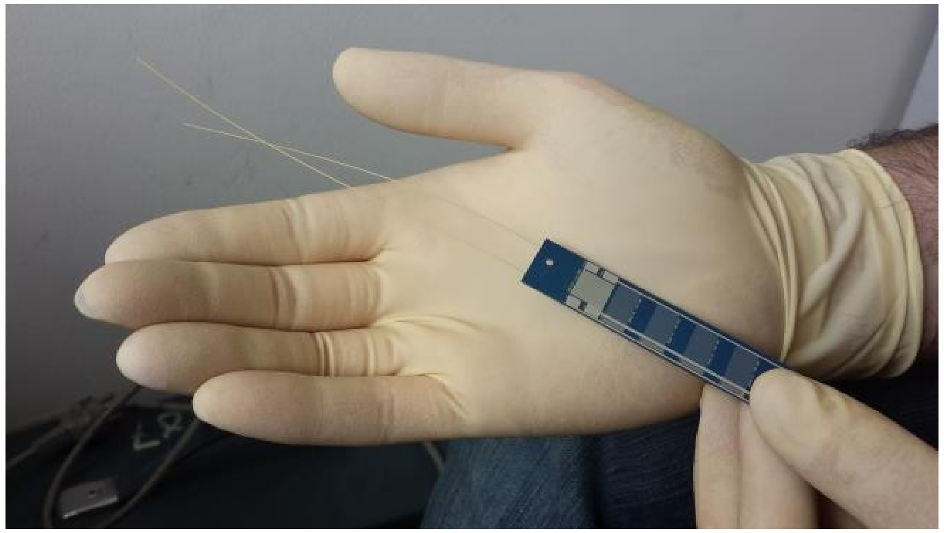
ILC candidacy benefits from developments for Belle-II and elsewhere

DEPFET technology also pursued for X-ray imaging (in space and at the XFEL) for microscopy, etc.
(ex. Development of a single ASIC for read-out and data processing, additional metal layer for speed-up)

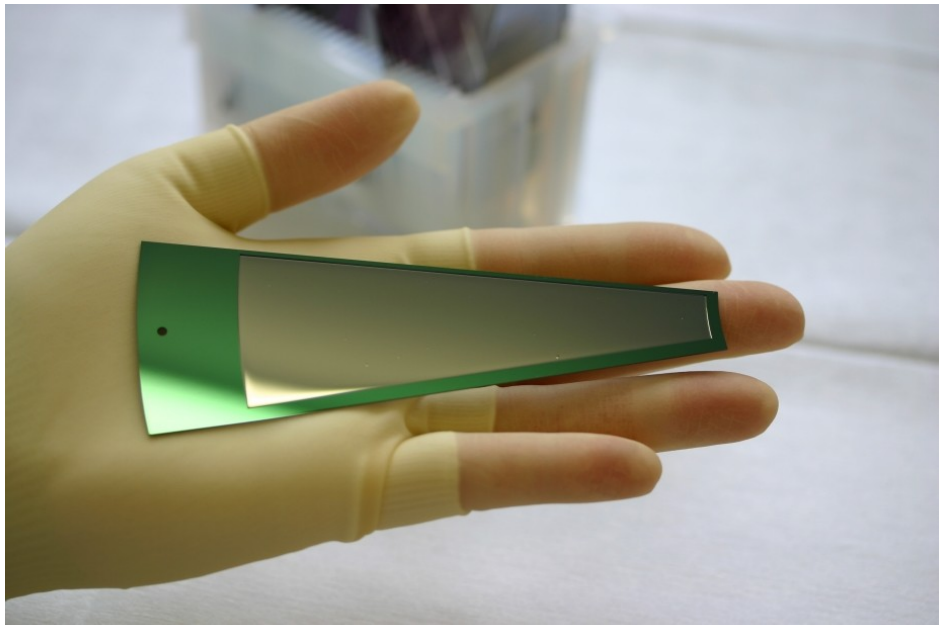
Healthy effort in the DEPFET collaboration for pixel detector R&D for collider applications

with key contributions Bonn/MPI/IFIC
mostly geared towards ILC/ILD
part of the AIDA-2 proposal

Examples:
Mechanical properties of petals
Power-pulsed DEPFET ladders
Micro-cooled DEPFET ladders



Micro-cooled DEPFET mechanical sample



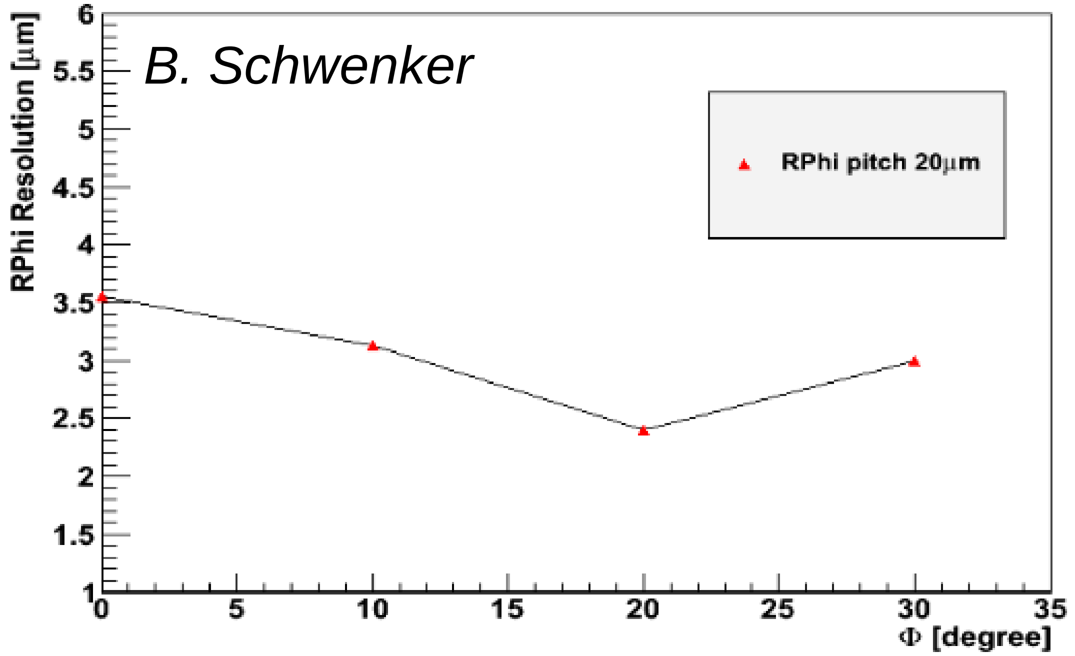
DEPFET mechanical petal prototype

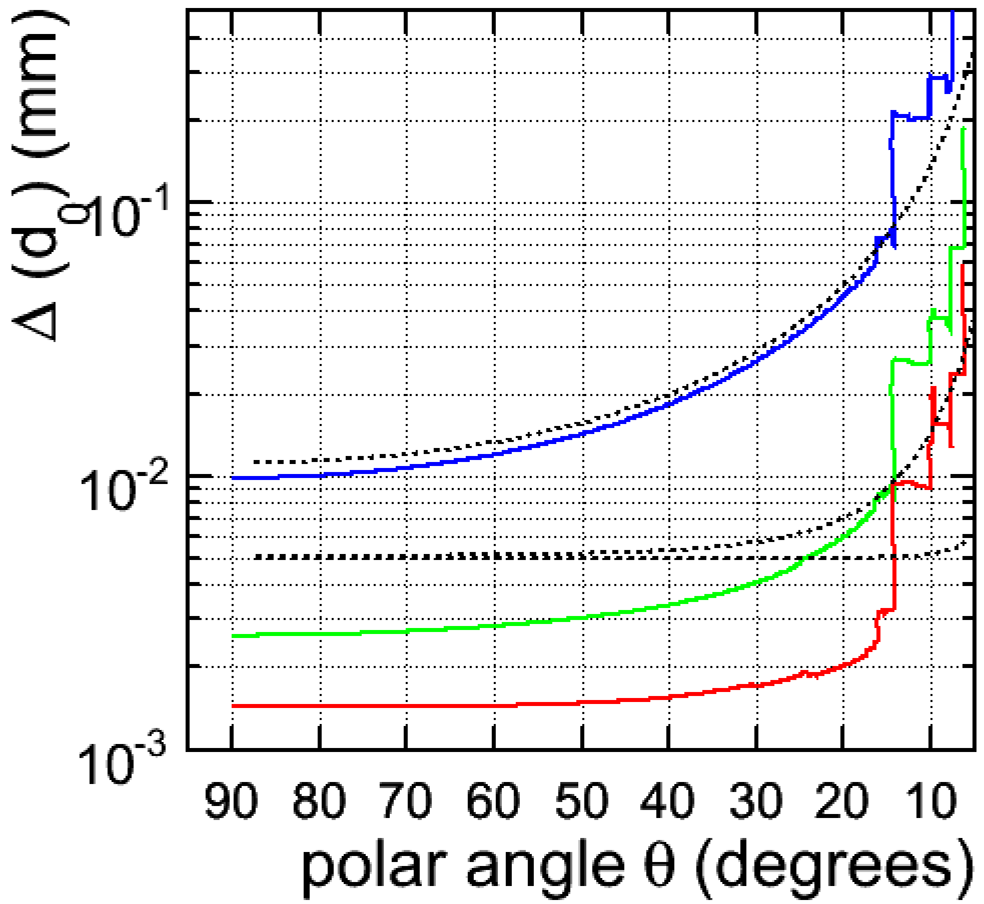
DEPFET
Active Pixel Detector

LC specific work: performance estimates

Detailed digitizer model in ILCSoft validated with years of ILC and Belle II test beams
B. Schwenker, Ph.D. Thesis U. Goettingen, to appear

Predictions for DEPFET spatial resolution in ILD environment: 2.3 - 3.5 µm
(ILD spec. 2.8 µm, but see M. Winter's talk)
IEEE TNS 60,2,2, ECFA review report





Input to optimization

Use detailed response model
(U. Goettingen, done)

Combine with detailed engineering model
(IFIC, under construction, see slide 9)

Return to study of track parameter resolution amd flavour tagging (b/c) performance

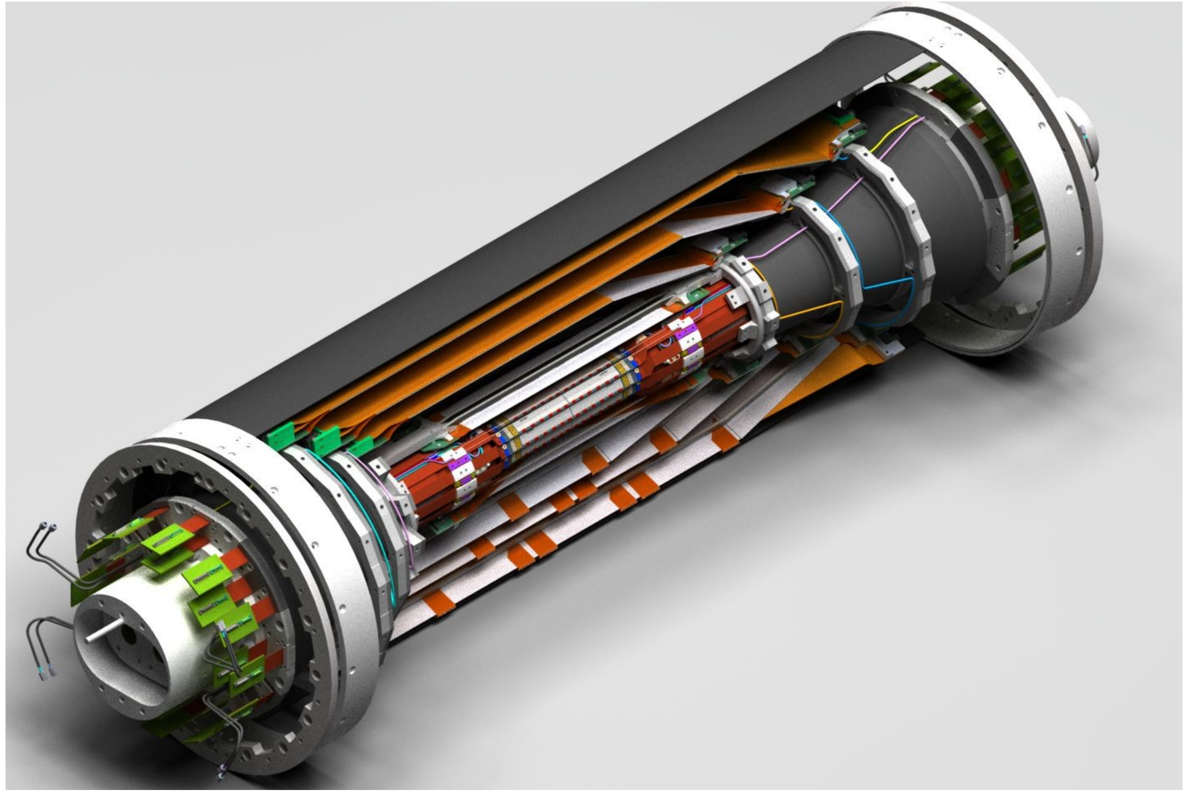
DEPFET
Active Pixel Detector

Summary

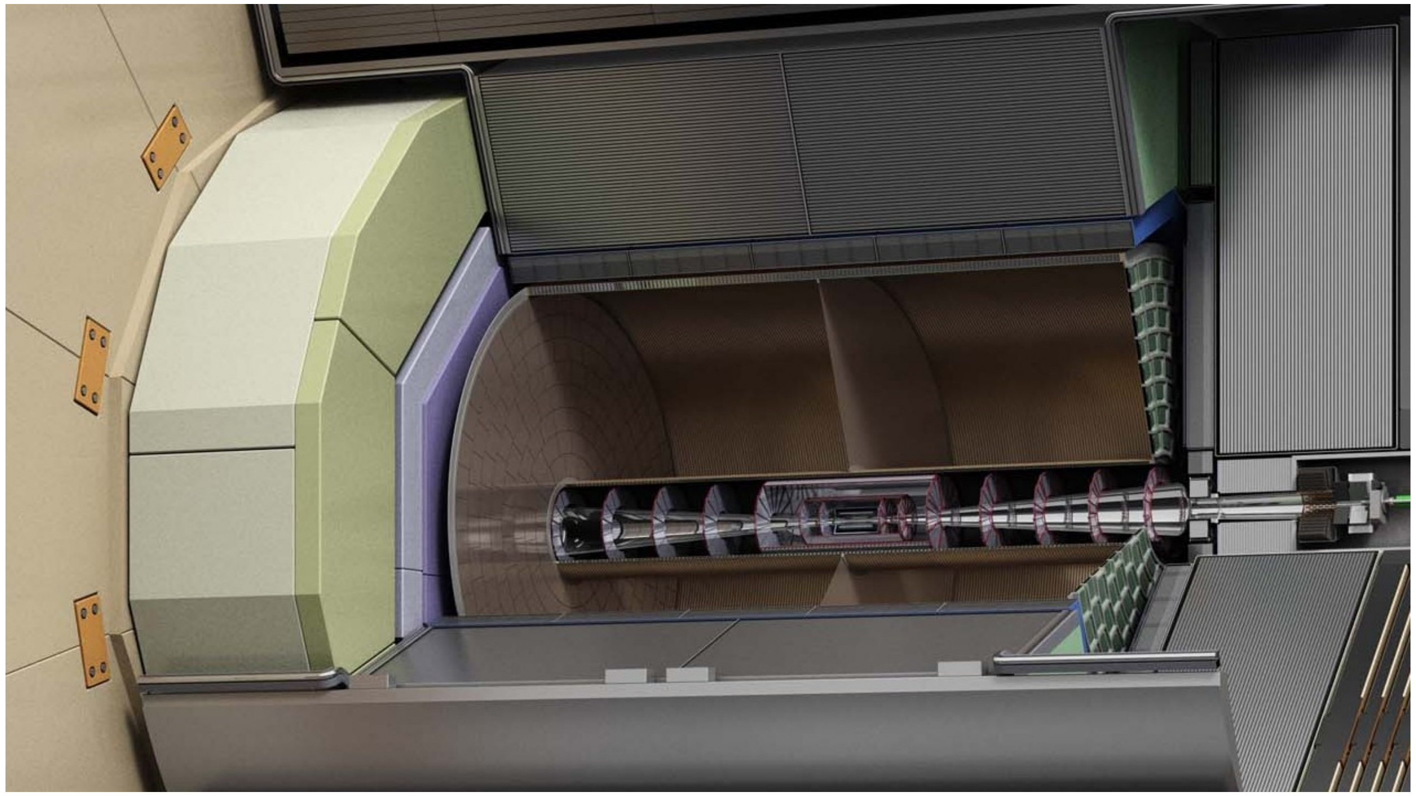
DEPFET candidacy for ILD vertex detector and FTD-pixels strengthening

- demonstrate maturity in Belle II, renaissance of R&D for projects beyond 2016
- work ongoing towards a complete ILC solution
- tools available for tech-specific evaluation of performance

Belle II vs future LC



Belle II vertex detector (2016):
innermost two layers based on DEPFET active pixel sensors



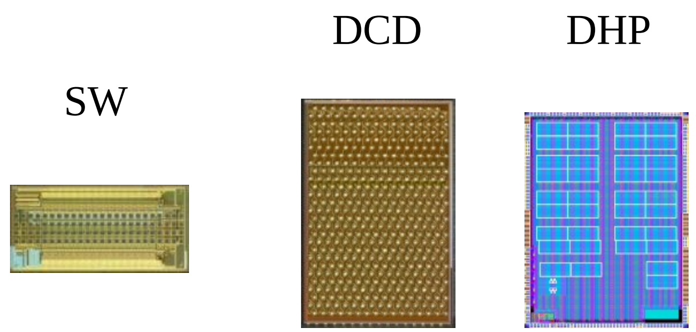
ILD and SiD inner tracking systems (202X):
five- or six-layer barrel vertex detector and several pixelated disks

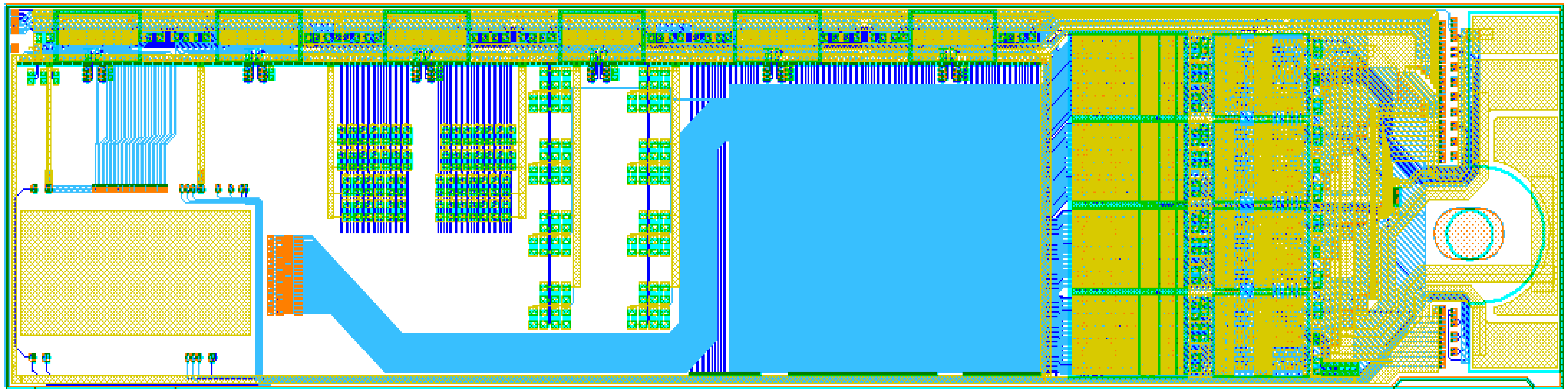
	ILC	*Belle-II*
occupancy	0.13 hits/μm^2/s	0.4 hits/μm^2/s
Radiation	< 100 krad/year, 10^{11} 1 MeV n_{eq}/year	> 1Mrad/year, 2 x 10^{12} 1 MeV n_{eq}/year
Duty cycle	1/200	1
Frame time	25-100 µs (10 ns @ CLIC)	20 µs
Momentum range	All momenta	Low momentum (< 1 GeV)
Acceptance	6°-174°	17°-150°
Resolution	Excellent 3-5 µm (pixel size = 20 x 20 μm^2)	Moderate (pixel size = 50 x 75 μm^2)
Material budget	0.15 % X_0/layer	0.21 % X_0/layer

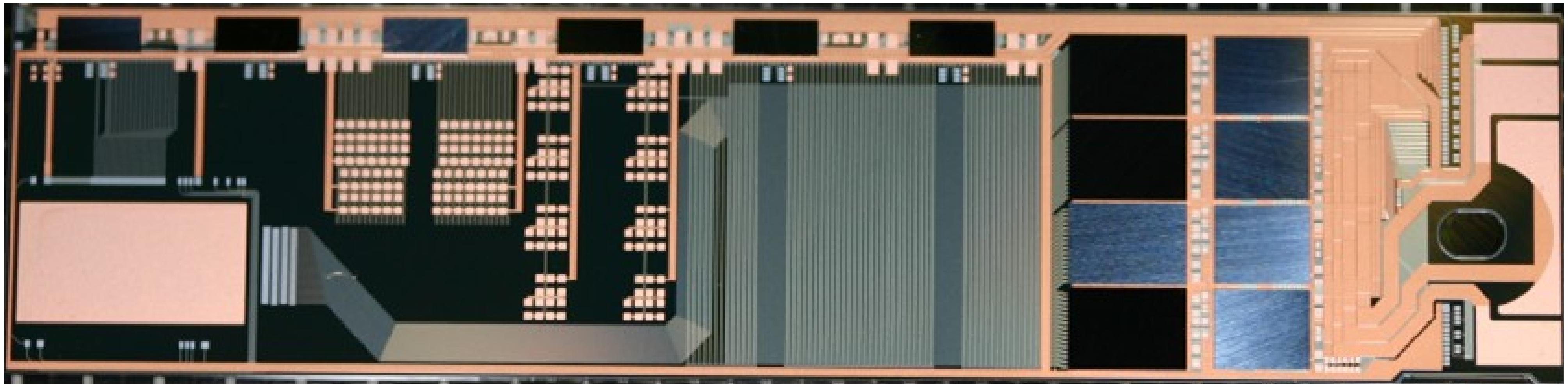
Electric MultiChip Module (E-MCM)

Electrical Multi Chip Module:

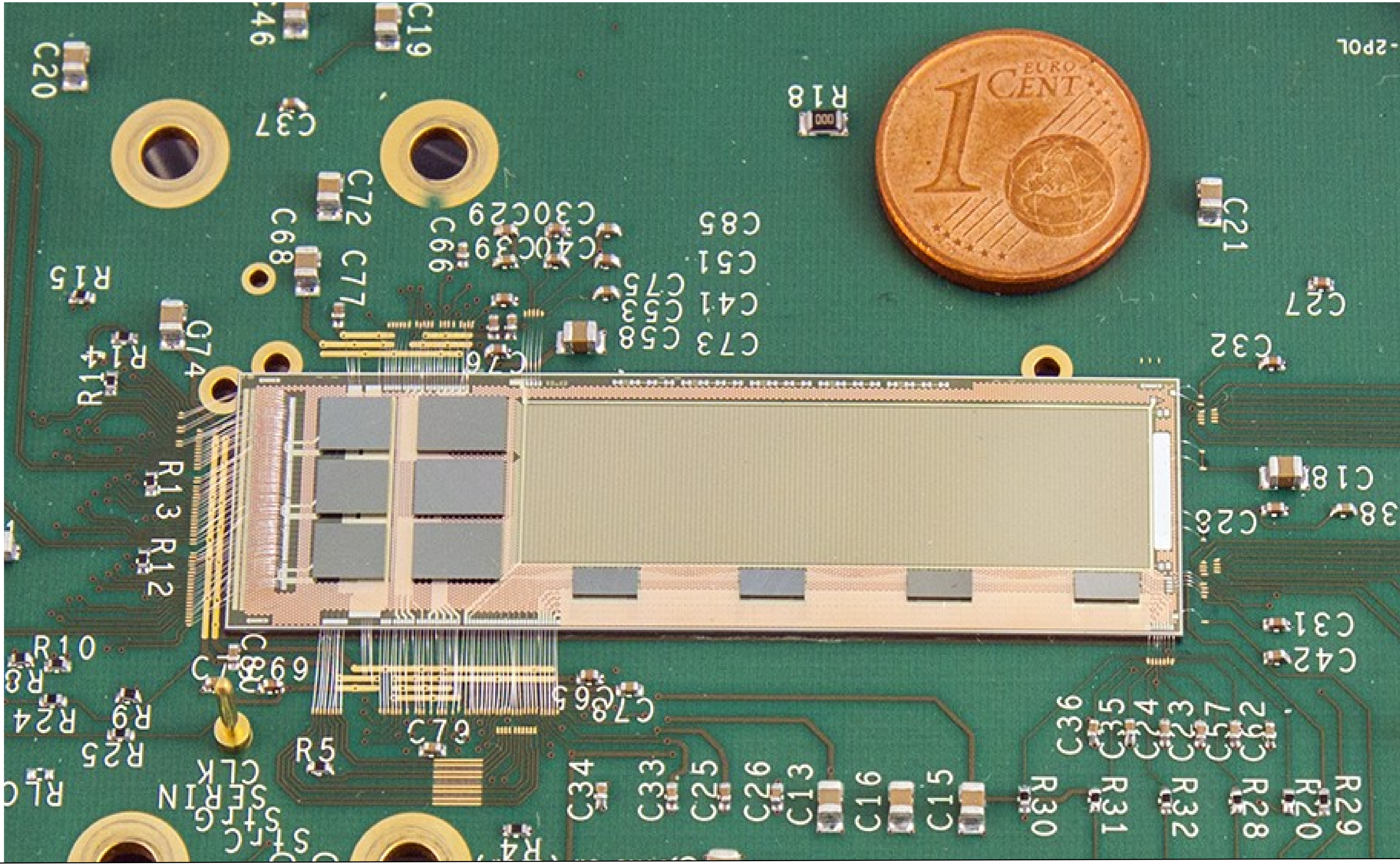
→ **Everything but the DEPFET (implantation)**
→ **Complete on-silicon circuitry for ASIC power and data**
→ **Modules produced, tested, ASICs flip chipped and Kapton attached**





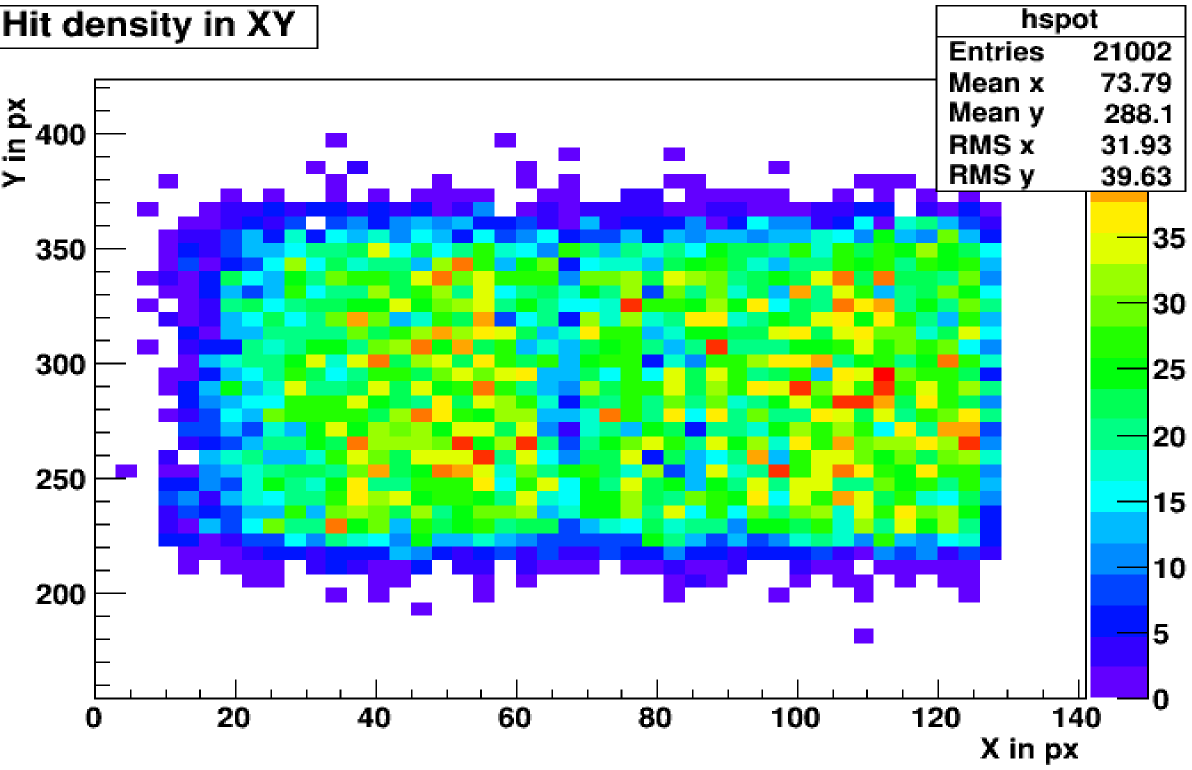


Thin Multichip Module



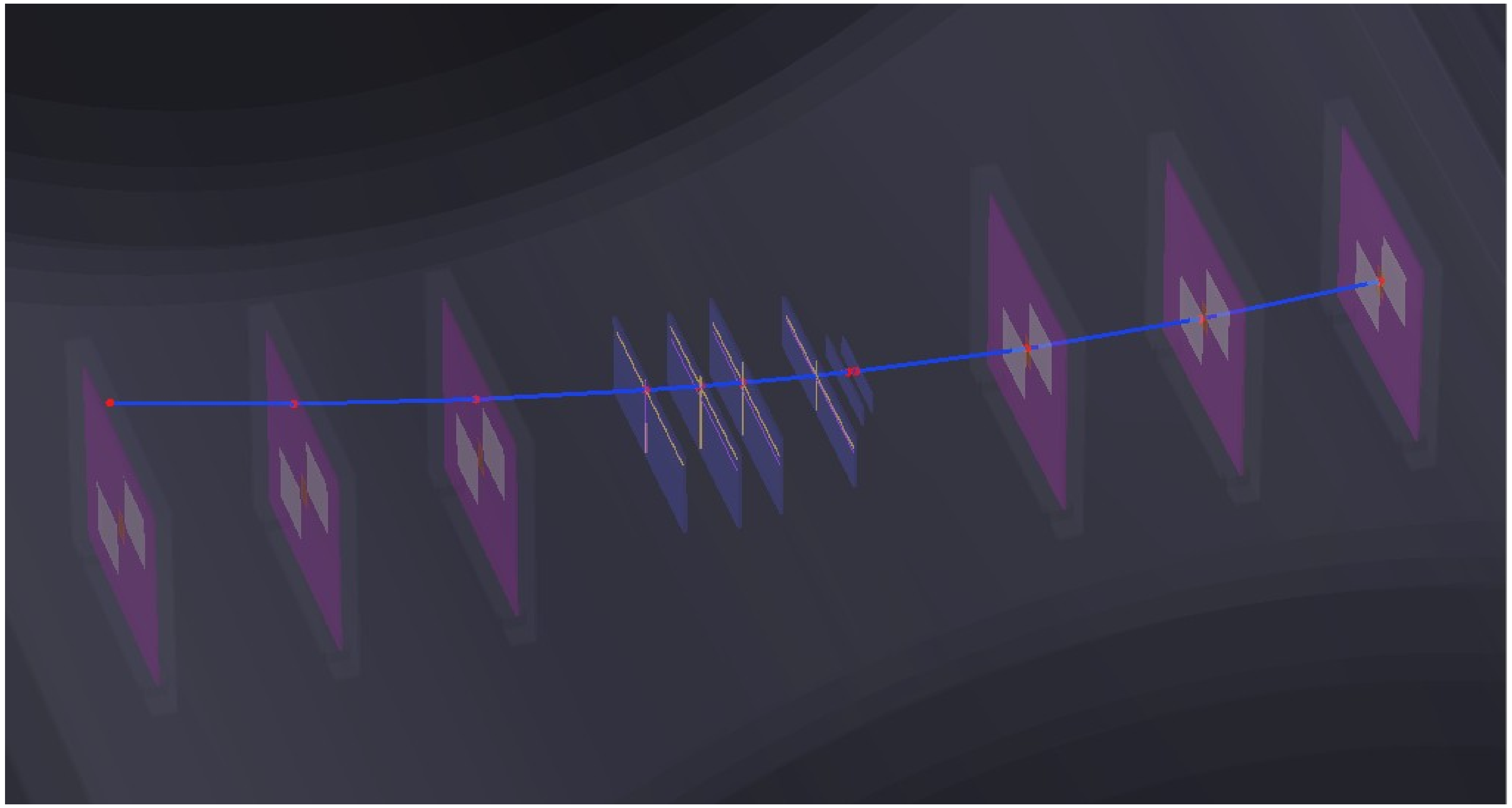
First large (512x192 pixels), thin (50 µm), DEPFET multi-chip ladder was operated in an electron beam at DESY in January

Preliminary TB results



Hit map during TB operation, beam spot 11x6 mm^2

Track fit through 6 MIMOSA beam telescope, 4 μ-strip layers and 1 DEPFET ladders (setup in 1 Tesla field of PCMAG)



DEPFET LC prospects

TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 6, NO. 1, SEPTEMBER 2010 1

DEPFET active pixel detectors for a future linear e^+e^- collider

The DEPFET collaboration
(www.depfet.org)
O. Alonso, R. Casanova, A. Dieguez, J. Dingfelder, T. Hemperek, T. Kishishita, T. Kleinohl, M. Koch, H. Krüger, M. Lemarenko, F. Lütticke, C. Marinas, M. Schnell, N. Wermes, A. Campbell, T. Ferber, C. Kleinwort, C. Niebuhr, Y. Soloviev, M. Steder, R. Volkenborn, S. Yaschenko, P. Fischer, C. Kreidl, I. Peric, J. Knopf, M. Ritzert, E. Curras, A. Lopez-Virto, D. Moya, I. Vila, M. Boronat, D. Esperante, J. Fuster, I. Garcia Garcia, C. Lacasta, A. Oyanguren, P. Ruiz, G. Timon, M. Vos*, T. Gessler, W. Kühn, S. Lange, D. Münchow, B. Spruck, A. Frey, C. Geisler, B. Schwenker, F. Wilk, T. Barvich, M. Heck, S. Heindl, O. Lutz, Th. Müller, C. Pulvermacher, H.J. Simonis, T. Weiler, T. Krausser, O. Lipsky, S. Rummel, J. Schieck, T. Schlüter, K. Ackermann, L. Andricek, V. Chekelian, V. Chobanova, J. Dalseno, C. Kiesling, C. Koffmane, L. Li Gioi, A. Moll, H. G. Moser, F. Müller, E. Nedelkovska, J. Ninkovic, S. Petrovics, K. Prothmann, R. Richter, A. Ritter, M. Ritter, F. Simon, P. Vanhoefer, A. Wassatsch, Z. Dolezal, Z. Drasal, P. Kodys, P. Kvasnicka, J. Scheirich

supporting paper for ILC TDR/DBD
in IEEE TNS 60, 2, 2 (2013)

ILC newsline
December 2012

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LC NEWSLINE
THE NEWSLETTER OF THE LINEAR COLLIDER COMMUNITY

CURRENT ISSUE
30 MAY 2013

The ECFA LC2013 workshop
Setting the course for European particle physics
Hiking like an electron
Impressions from Hamburg
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CALENDAR

AROUND THE WORLD

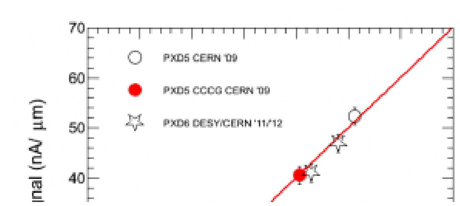
DEPFET active pixel detectors for the linear collider

Marcel Vos reports on behalf of the collaboration

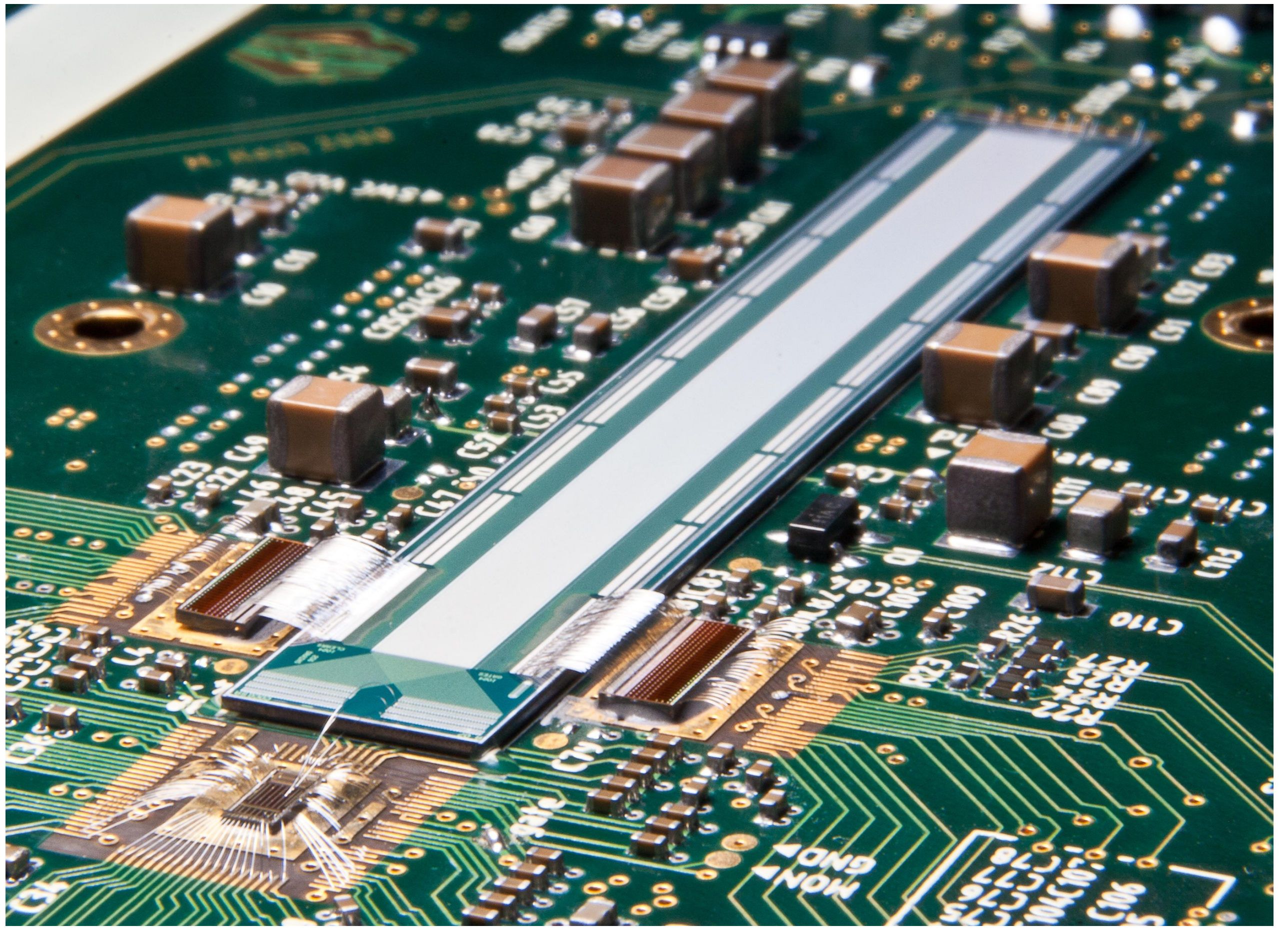
Share |

24 January 2013

Solid-state devices for charged particle tracking proved their value in high energy physics in the most internal layers of the experiments of the Large Electron Positron Collider LEP at CERN, where they provided precise information on the production vertex of charged particles. These silicon micro-strip detectors consisted of a thin reverse-biased *pn*-junction segmented in narrow strips, each of which was read-out by an amplifier and analog-to-digital converter on a read-out ASIC. After a rapid evolution fueled

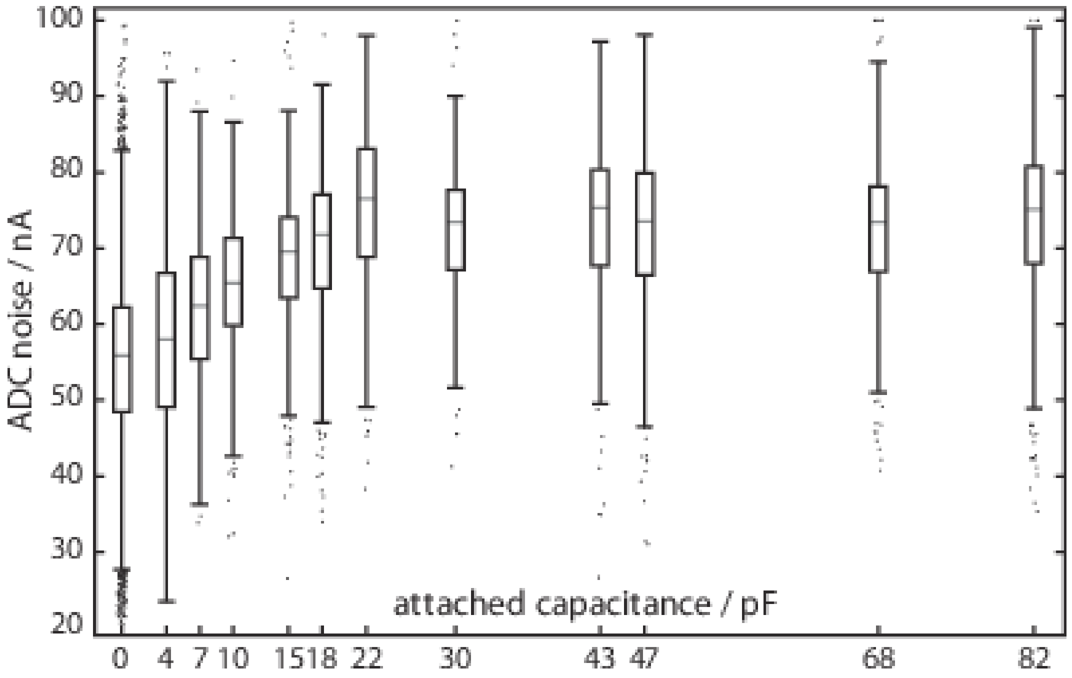


ASIC performance

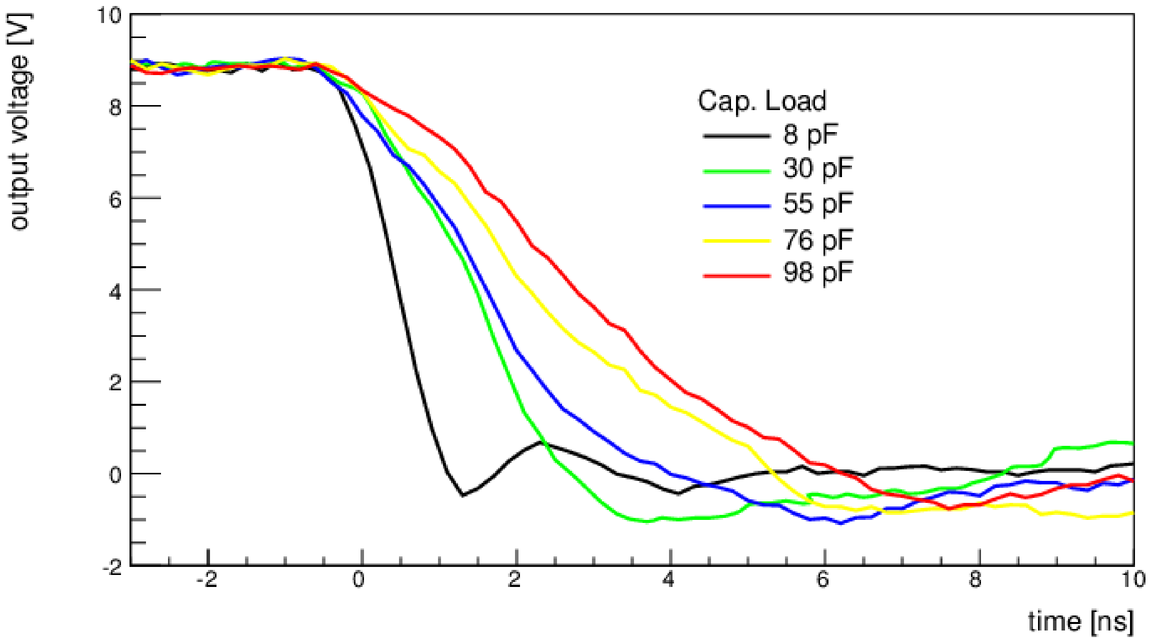


DCDB (read-out ASIC) and Switcher (steering chip) have been produced in a design that is quite close to what we would build for ILC.

Can now base LC prospects on measurements

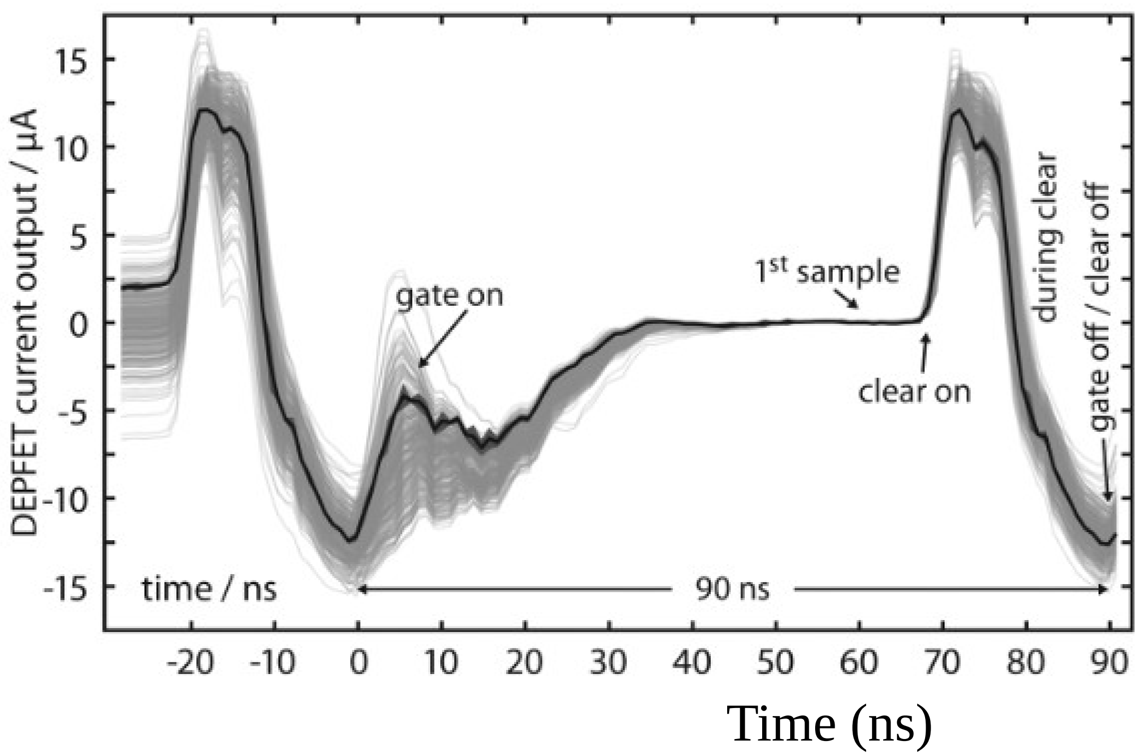


Noise of the FE chip (DCD) versus capacitative load

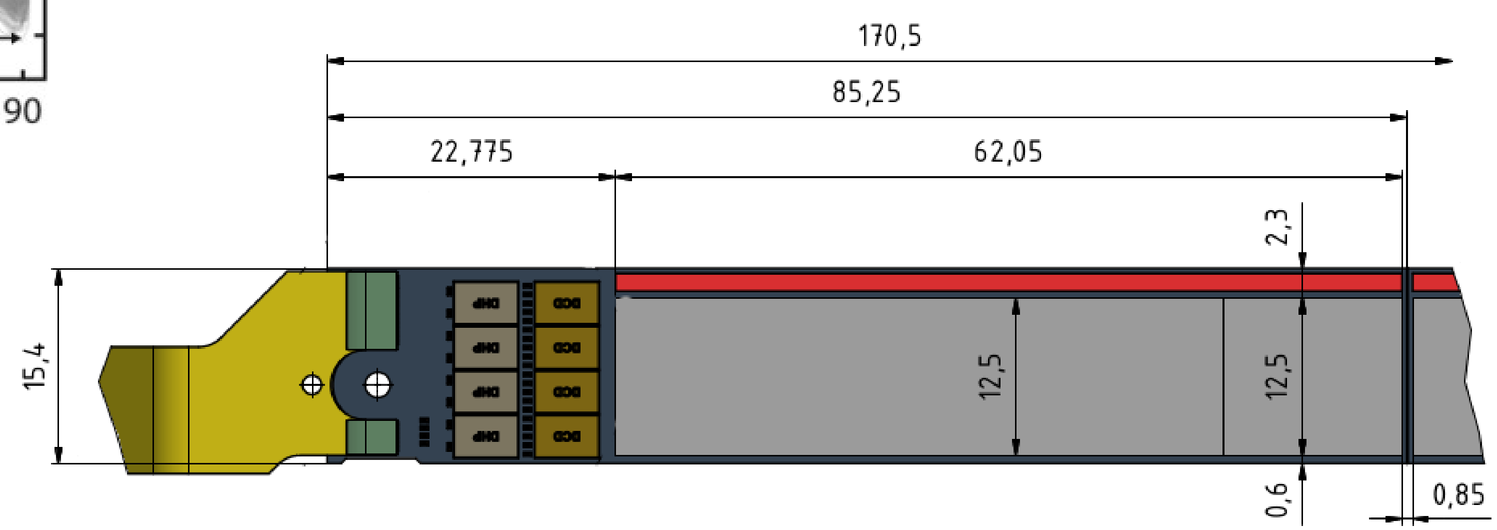


Clear pulse from Switcher

DEPFET @ LC - barrel



Read-out speed: current state-of-the-art allows for a row rate of 1/100 ns. Room for improvement.



VXD0 → 12.5cm long barrel layer with read-out ASICs on both ends.

Pixel size:

Center (|z|<1) → 25 x 25 µm^2

1 <|z|< 2 cm → 25 x 50 µm^2

|z| > 2 cm → 25 x 100 µm^2

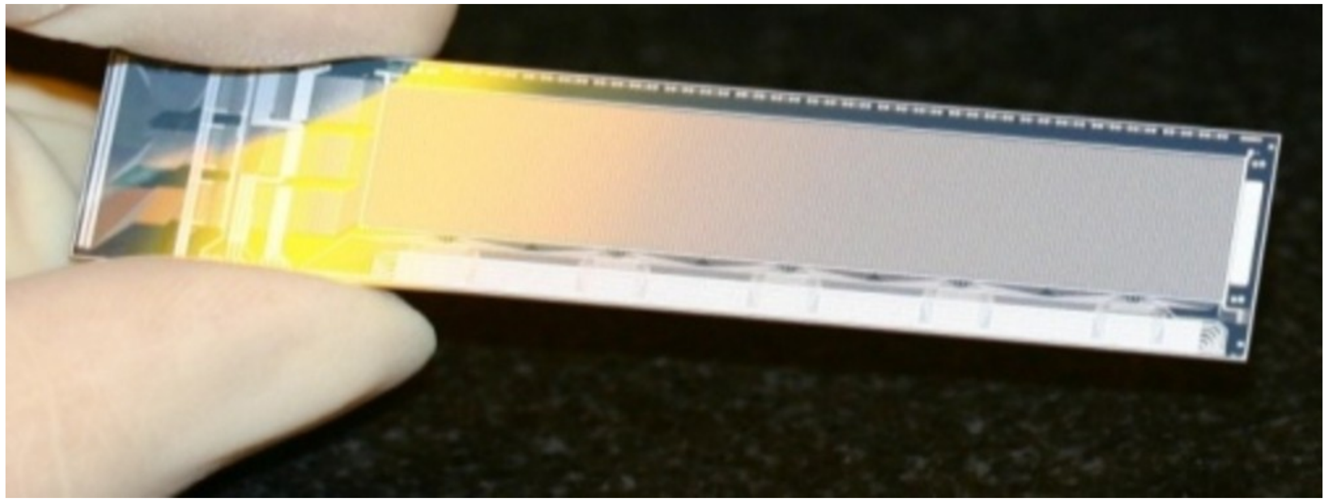
Column depth: *1025 pixels/half-ladder*

Multiplexing: *2 (4) rows sampled in //*

Row rate: *1/80 ns*

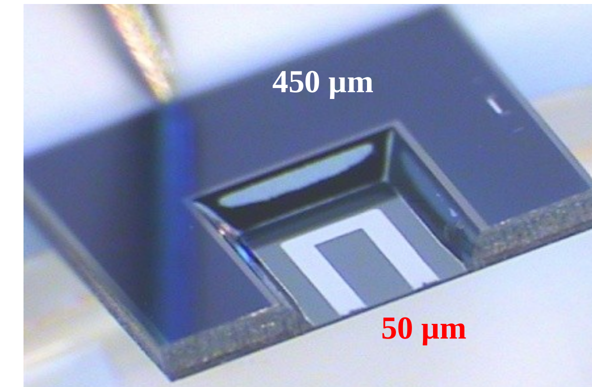
Frame time: *40 µs (20 µs)*

Material budget

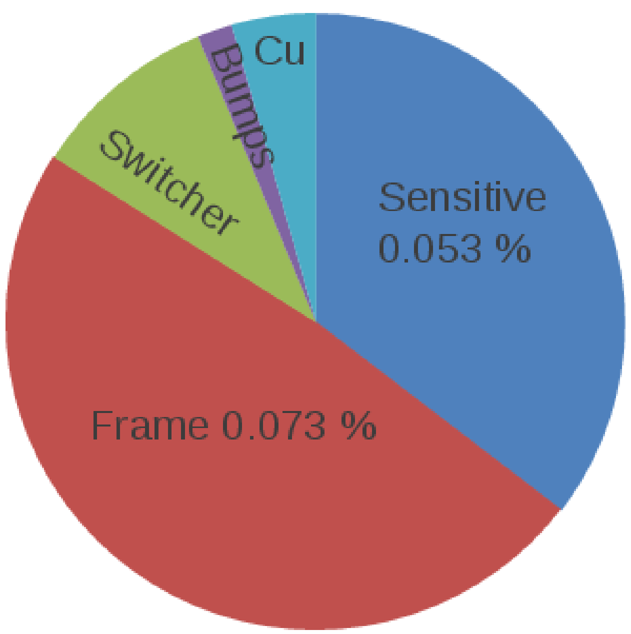


Integrate!

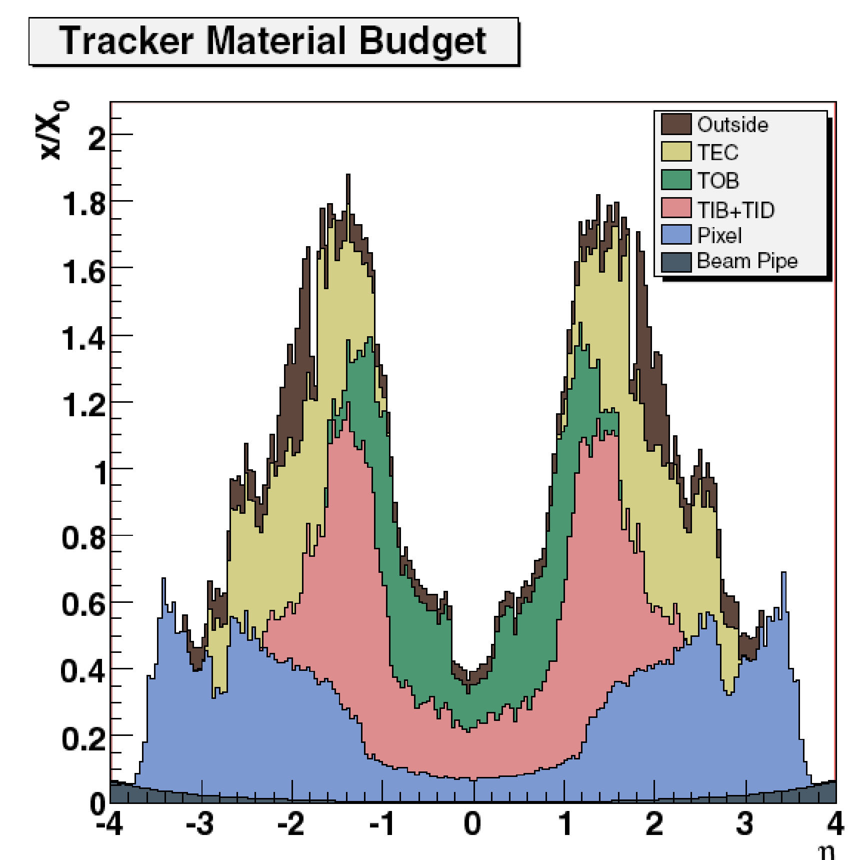
Amplification stage in sensor
Support structure in sensor
Signal and power lines on sensor
Electronics on sensors



Material budget close to LC goal!!!



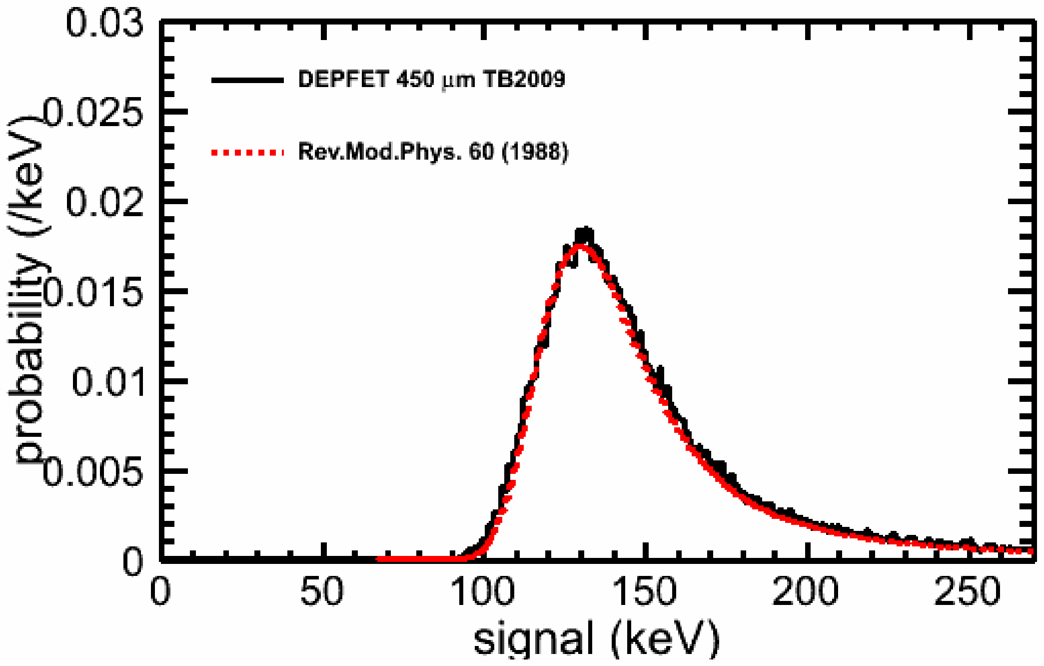
Sensitive	0.053 % X_0
Frame	0.073 % X_0
Switcher	0.015 % X_0
Cu layer	0.007 % X_0
Bumps	0.003 % X_0
Total ladder	0.15 % X_0



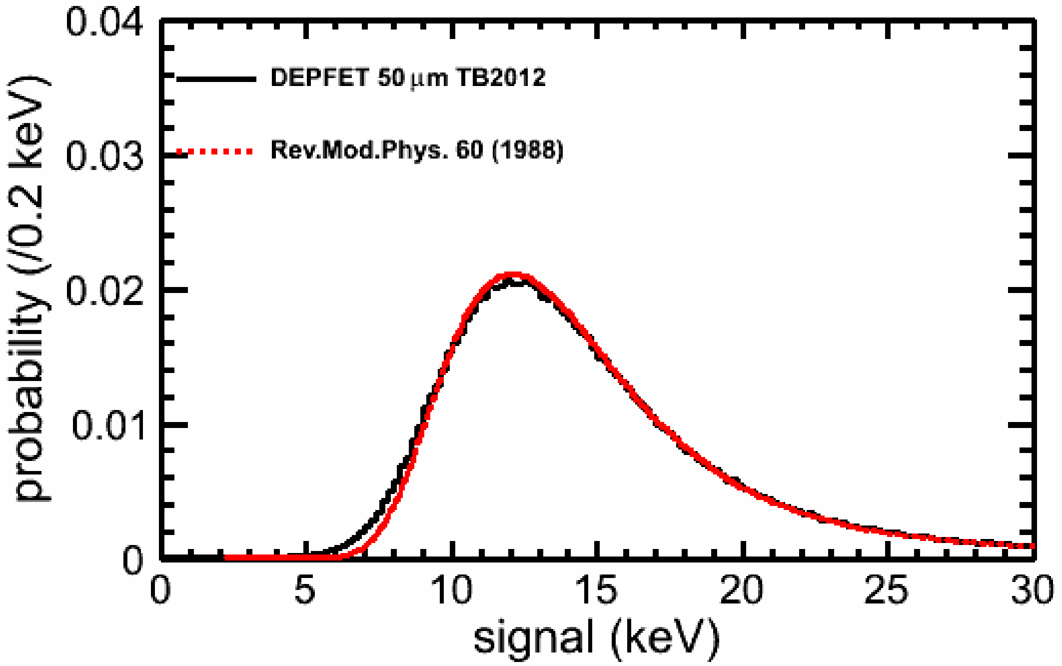
Big leap wrt to LHC...

Admittedly not a fair comparison

Test beam measurements



450 μm thick prototype
with 20x20 μm2 pixels
Slow (CURO) read-out
S/N ratio = 130-200



50 μm thick prototype
With 50x75 μm2 pitch
Close to final (DCDB) read-out
S/N ratio = 20-40

Excellent agreement with straggling model by H. Bichsel up to several times the Most Probable Signal
Width of distribution due to “Landau” fluctuations correctly predicted

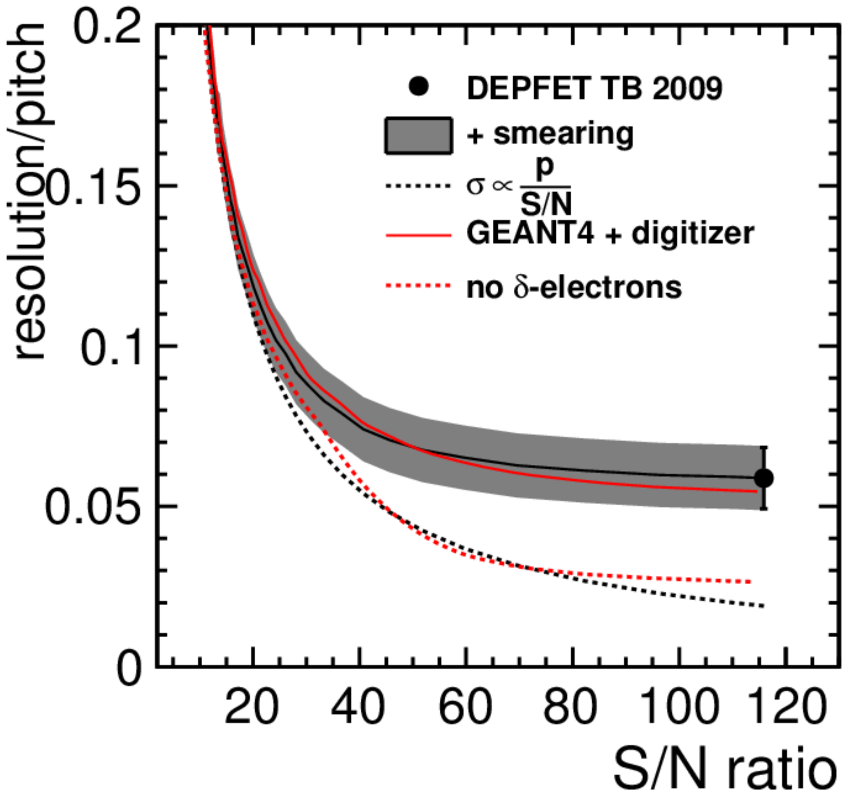
Spatial resolution – the limit

Thick DEPFET sensors have registered a resolution (for 120 GeV pions) of approximately **1 μm**

Questions: *Is that what we would expect?*
What should we do to do better still?

Theory: $\sigma \propto \frac{p}{S/N}$ *(constant depends on charge sharing details)*

Empirical answer: sensor with S/N > 100, smear signal to mimic worse S/N



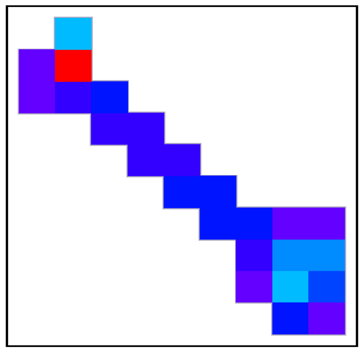
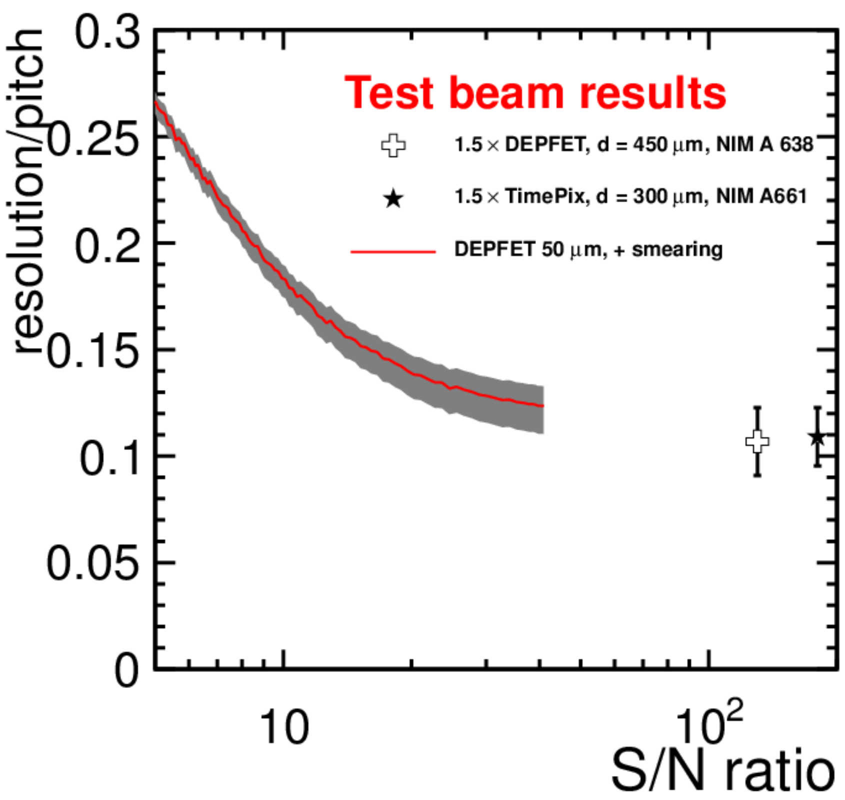


Image of a δ electron captured in a DEPFET beam test



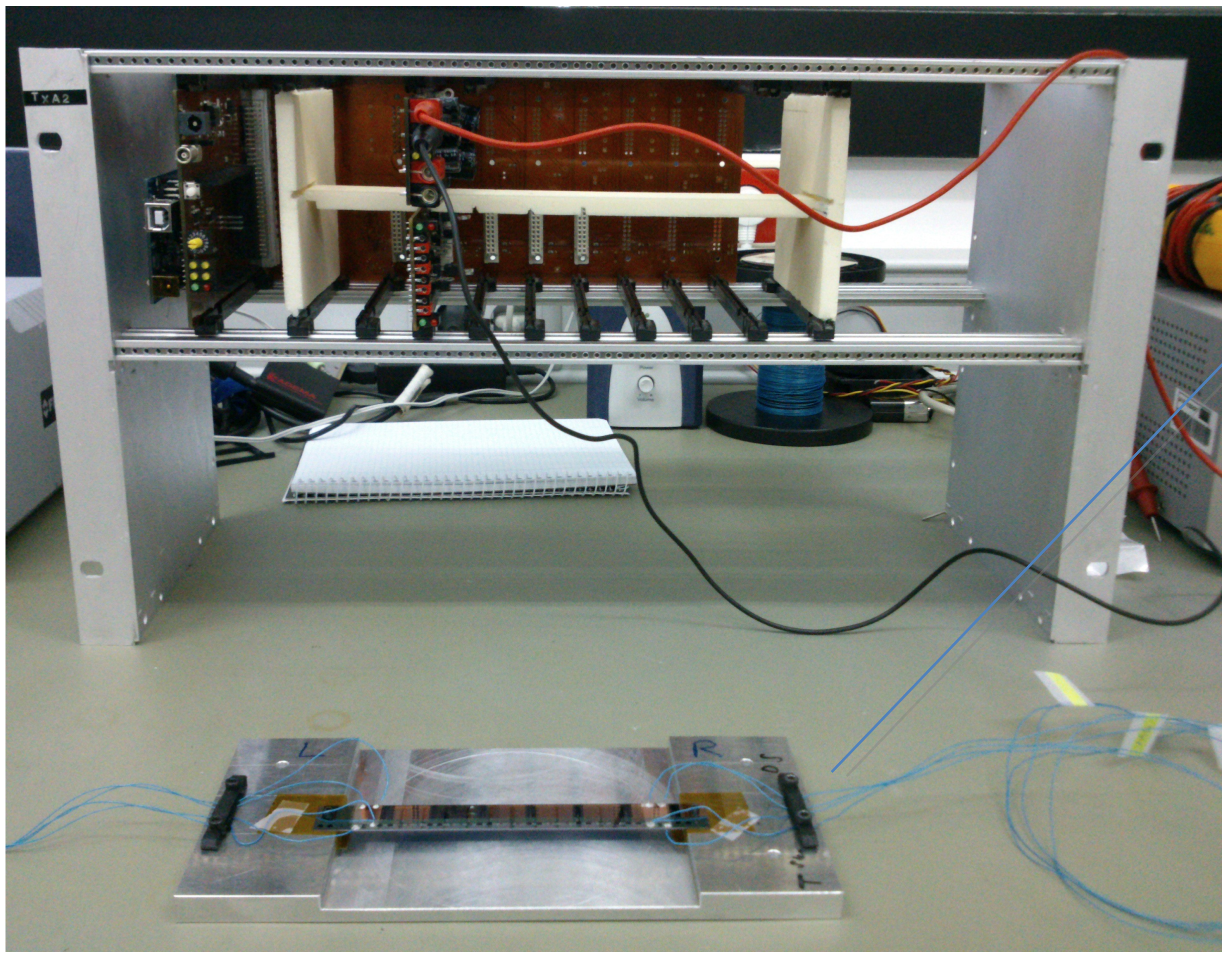
Incidence angle such that projection = pixel size
Landau fluctuations start to play a role
Asymptotic resolution depends on thickness
σ/p ~ 0.12 for d=50 μm

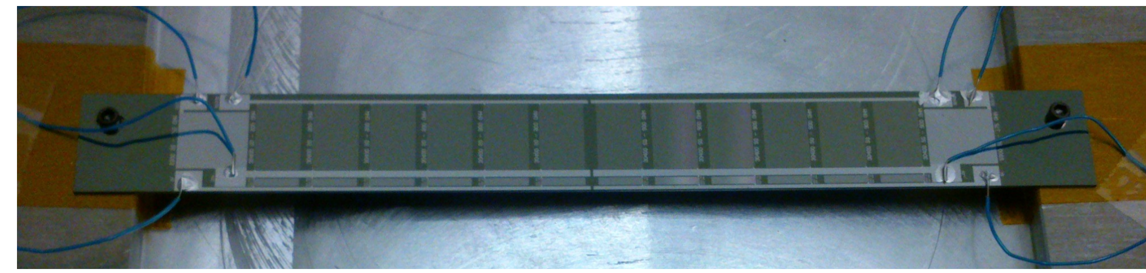
Perp. Incidence: the spatial resolution "saturates" at σ/p ~ 0.07 (approx. 1 μm for state-of-the-art devices). Further progress is checked by δ-electrons

arXiv:1404.3545

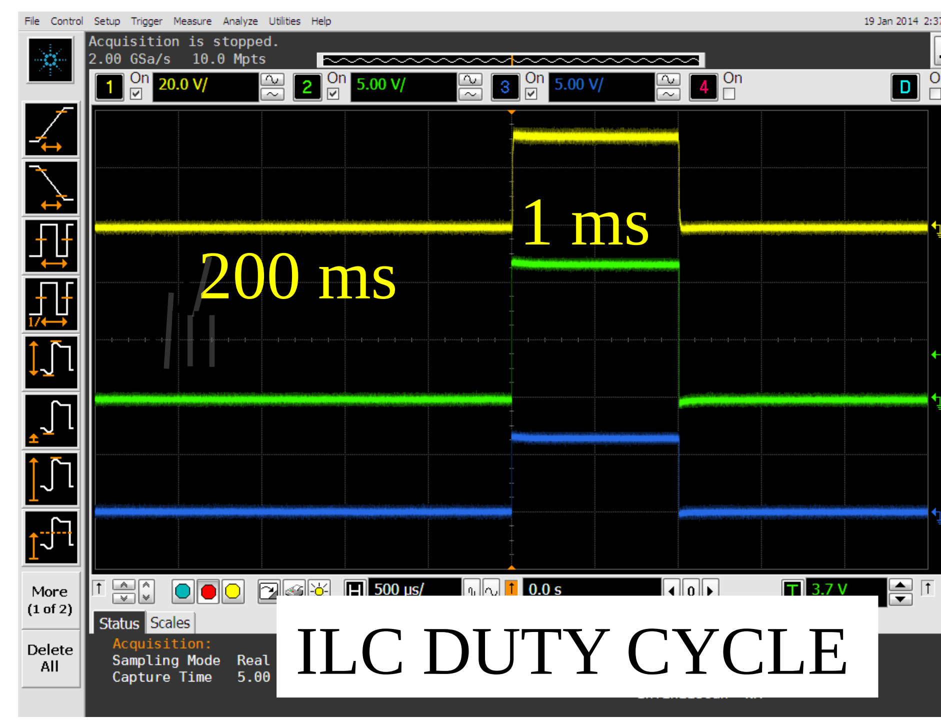
Power pulsing & thin Si ladders

- **Pulsing power system developed at IFIC**



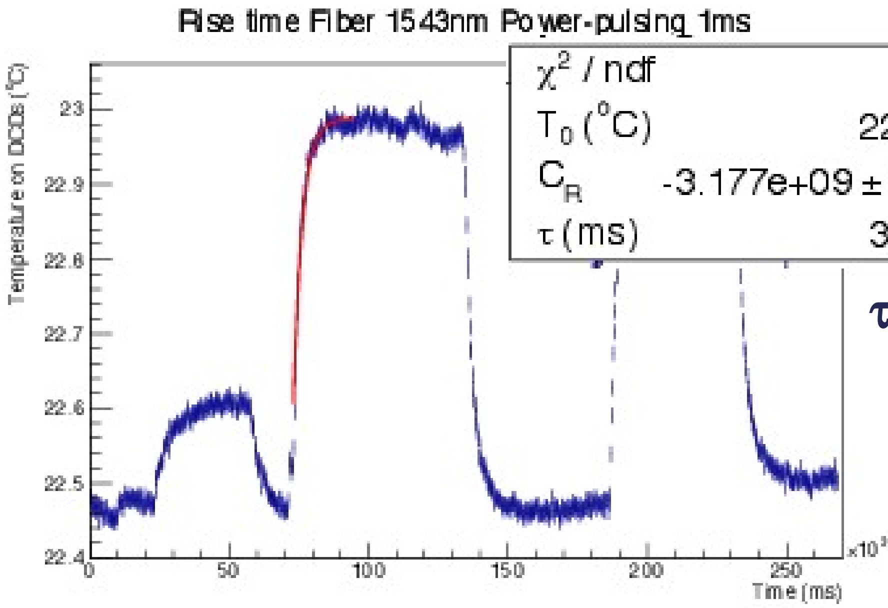


Mechanical DEPFET ladder sample

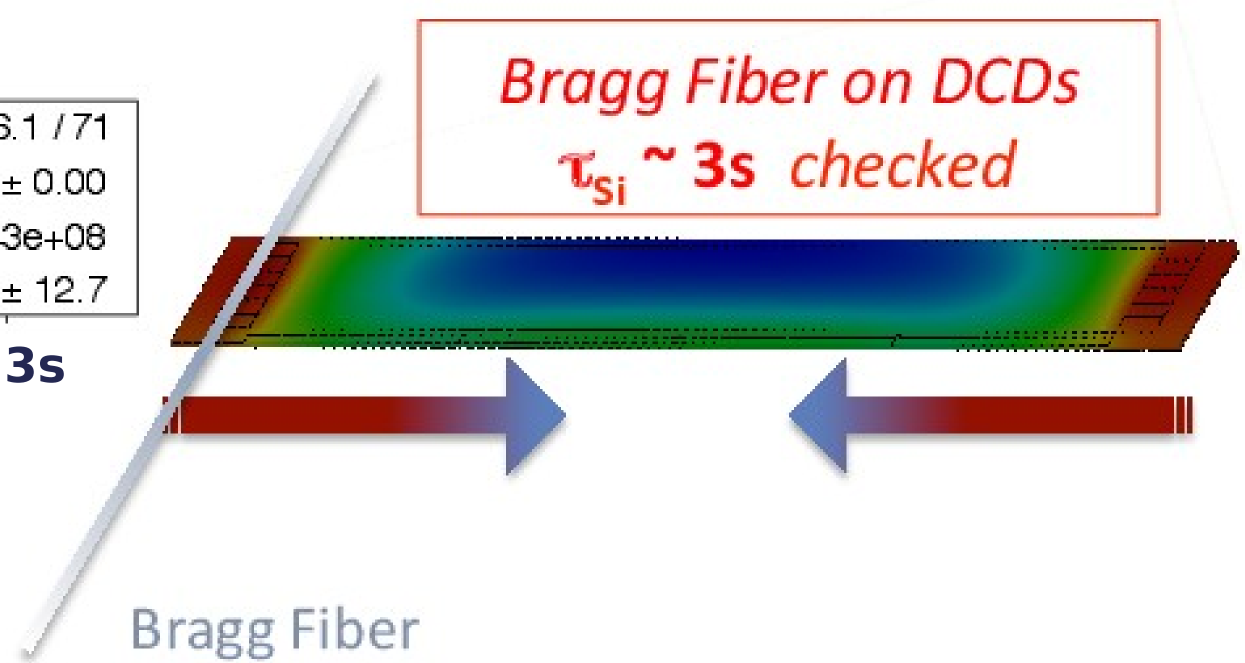


- Study of the thermo-mechanical properties of thin sensors with a pulsed power supply

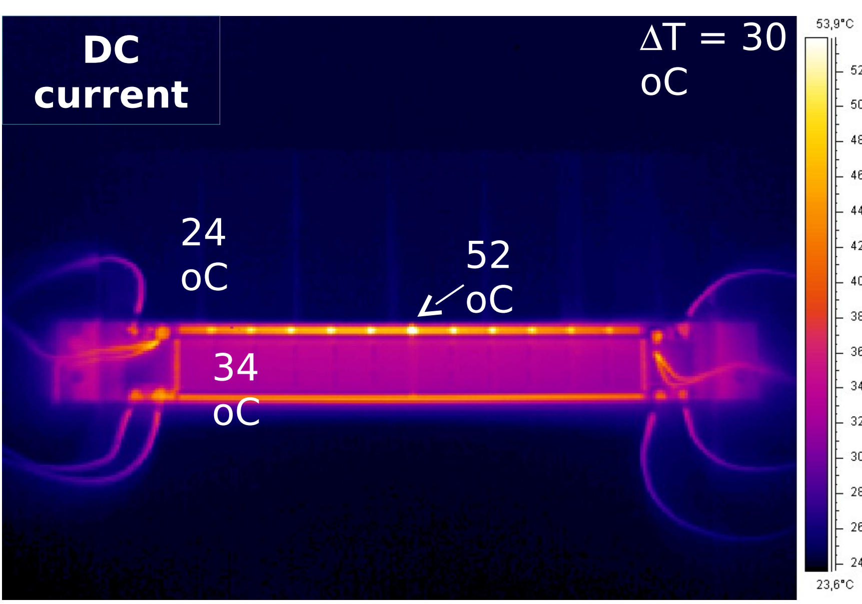
Thermal measurements

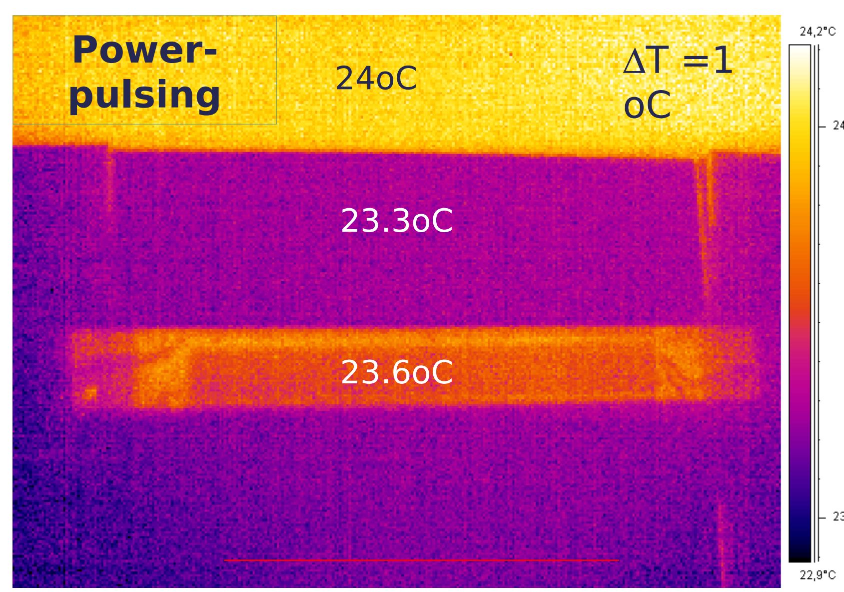


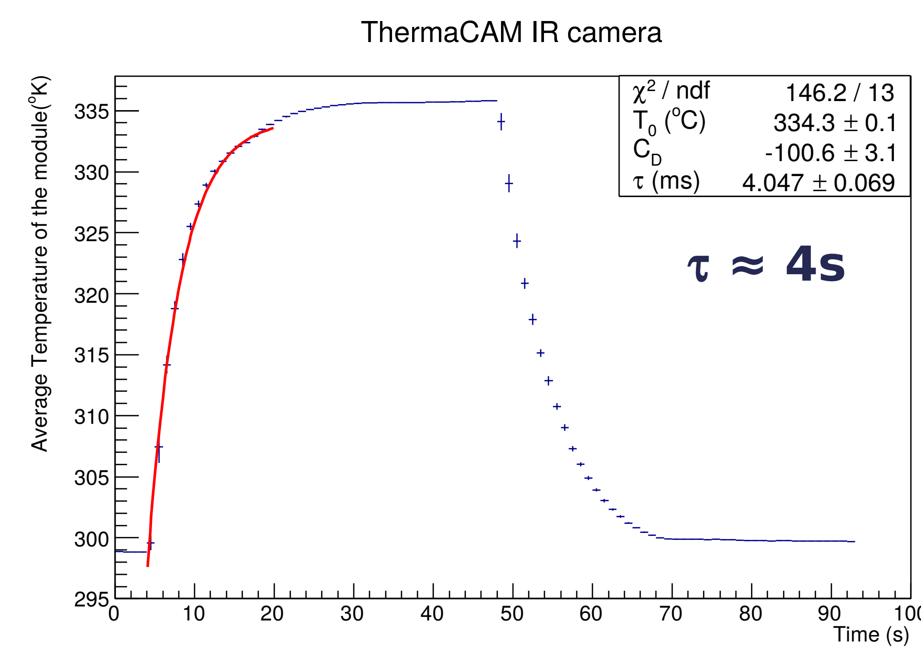
$\tau \approx 3s$



Switch power supply on and off abruptly and measure time it takes for Silicon temperature to settle





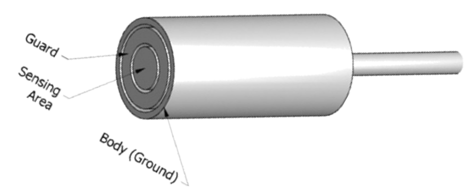


ThermaCAM SC500 (FLIR systems) Frecuency: 50Hz

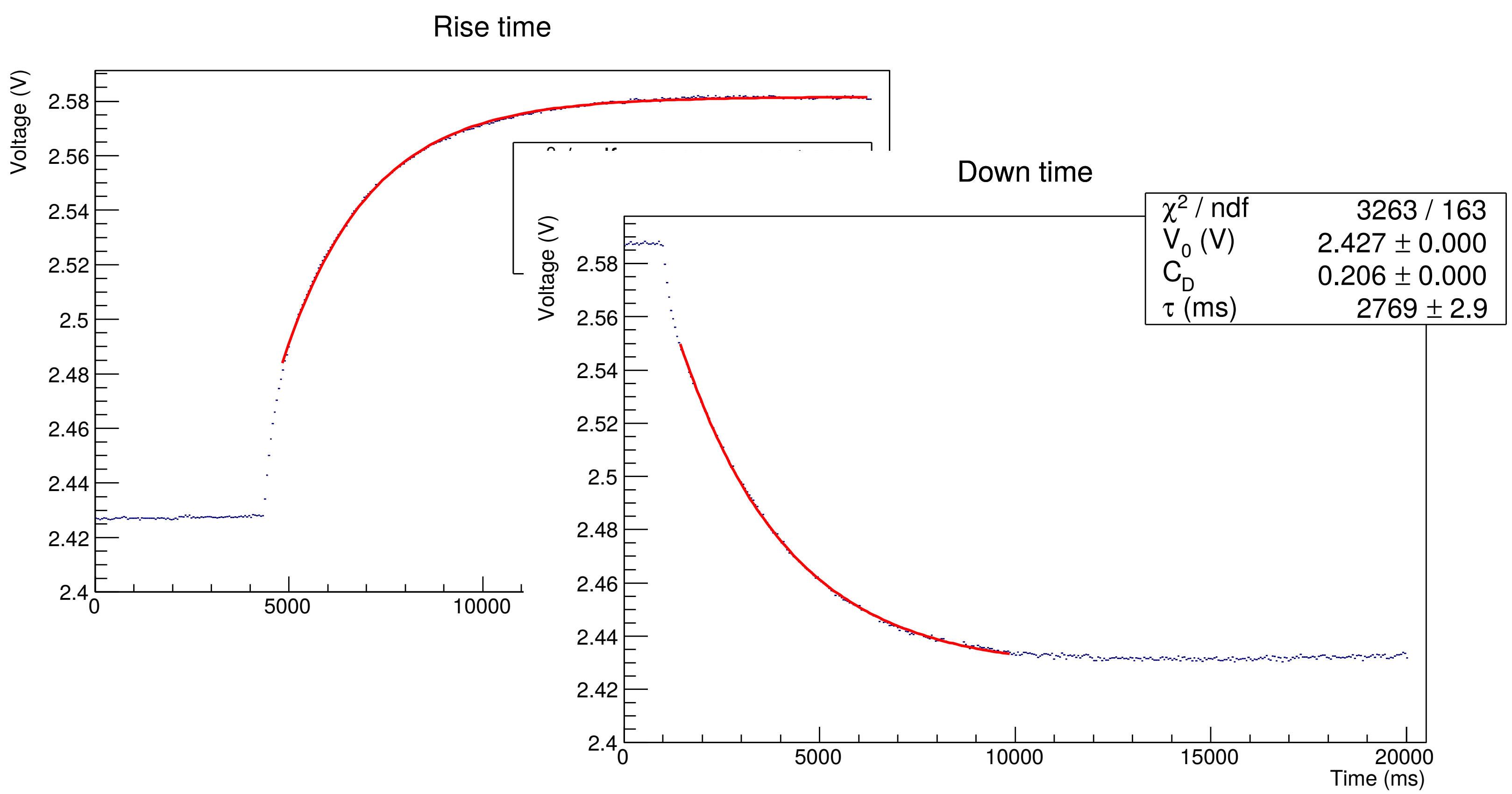
Mechanical measurements

Capacitive sensor
(Micro-Epsilon Capa NCDT 6100)

- Sensitivity: 0.15µm



DC current

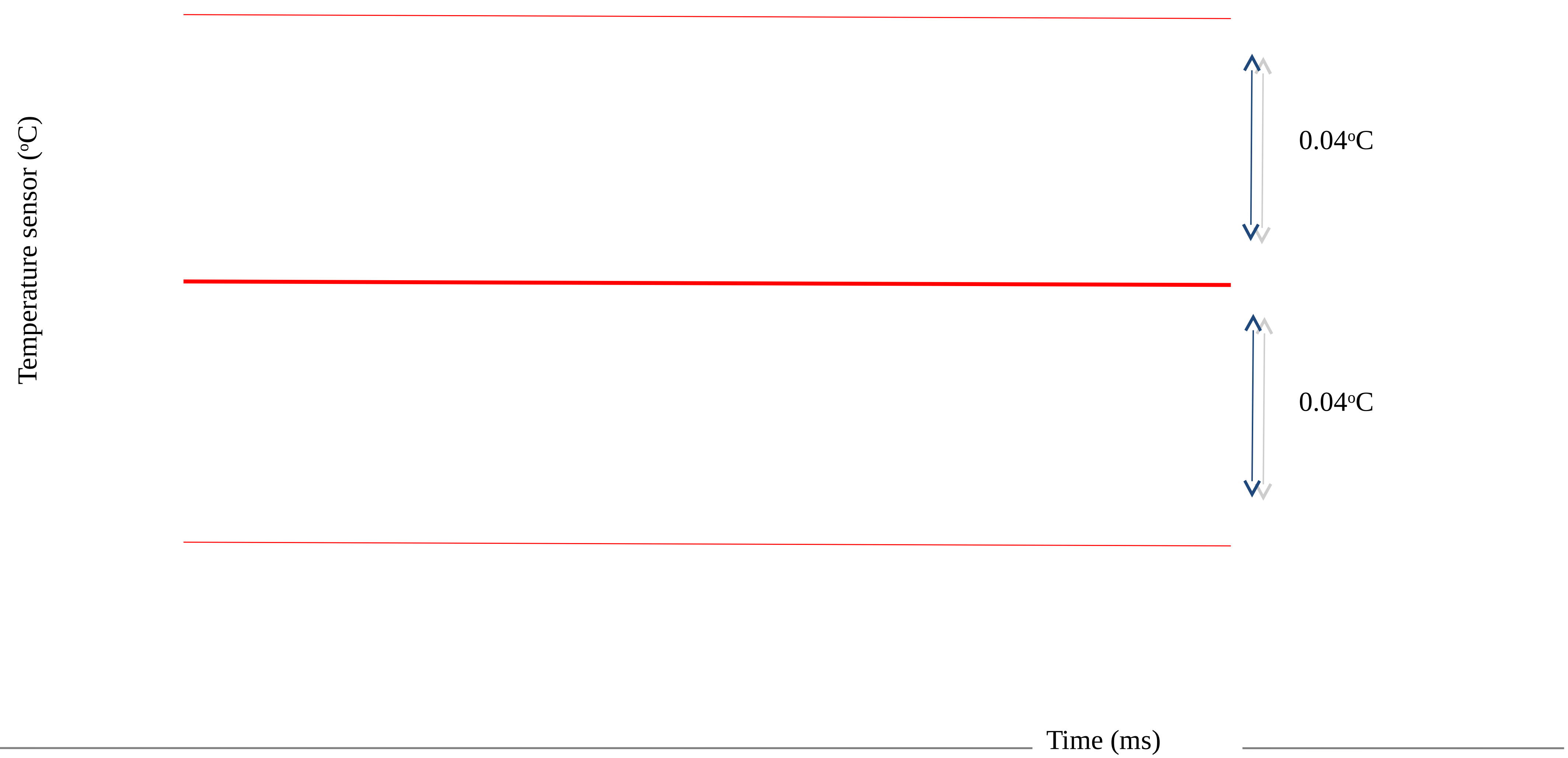


Mechanical measurements follow the temperature measurements with nearly identical time constant

Results on thin ladders with power pulsing

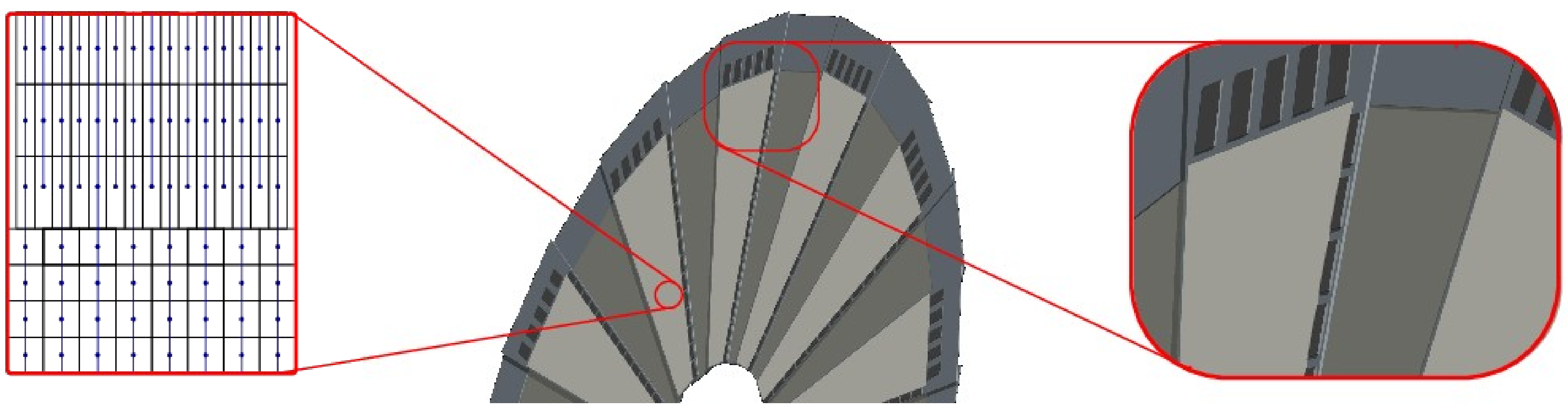
Combination of measurements using thermal camera (60 Hz), optical fibers with Bragg grating (1 kHz) and capacitative probe (1 kHz)

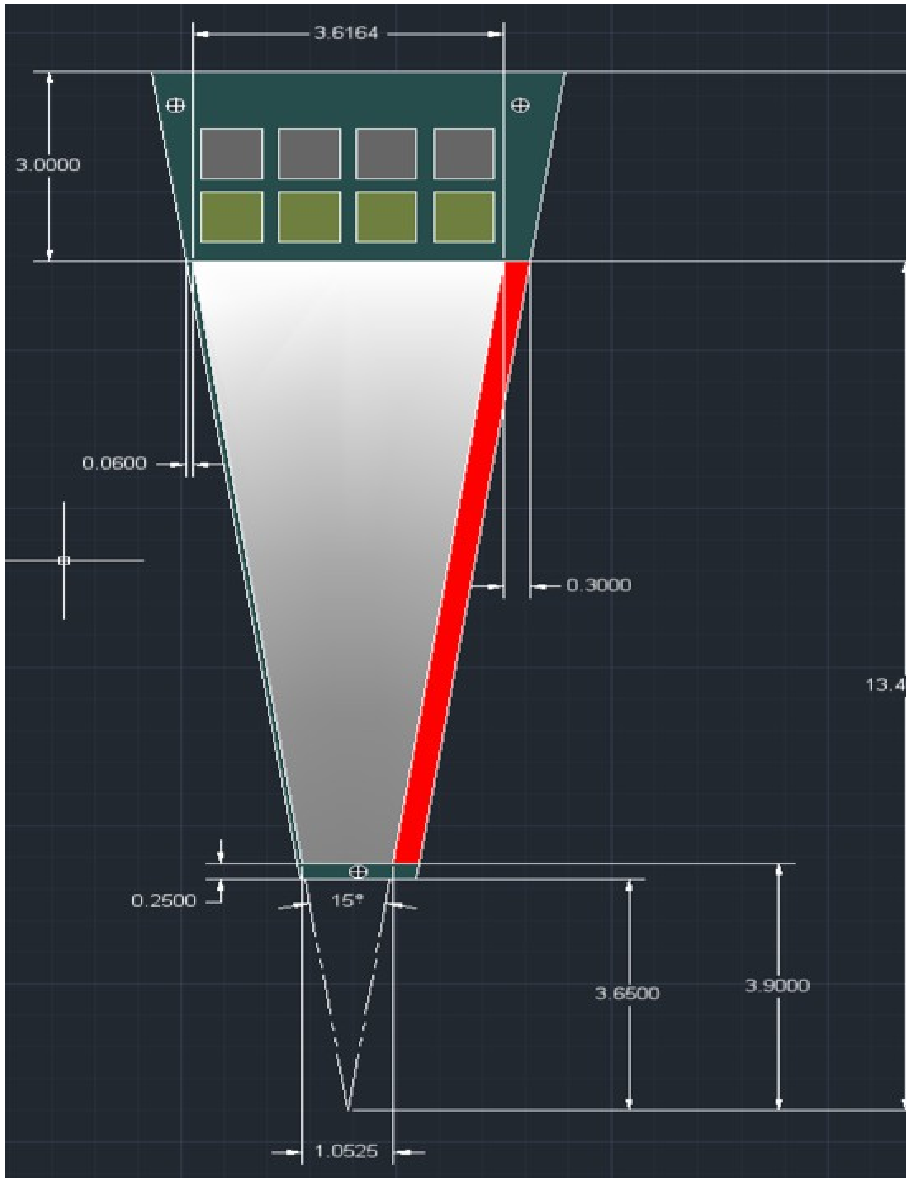
- **NO rapid thermal excursions** observed due to **power pulsing (< 0.1 °C)**
- **Thermal inertia of Silicon** ladder measured; **τ ~ 3 s**
- **Average ladder temperature** rises **< 1 °C** for nominal DEPFET load and 1/200 duty cycle



DEPFET @ LC disks

- LC detector concepts require pixelated disks
  - → vertex detector end-cap in SiD, Forward Tracking Disks in ILD
  - → adapt DEPFET all-Si “ladder” design to “petal” geometry

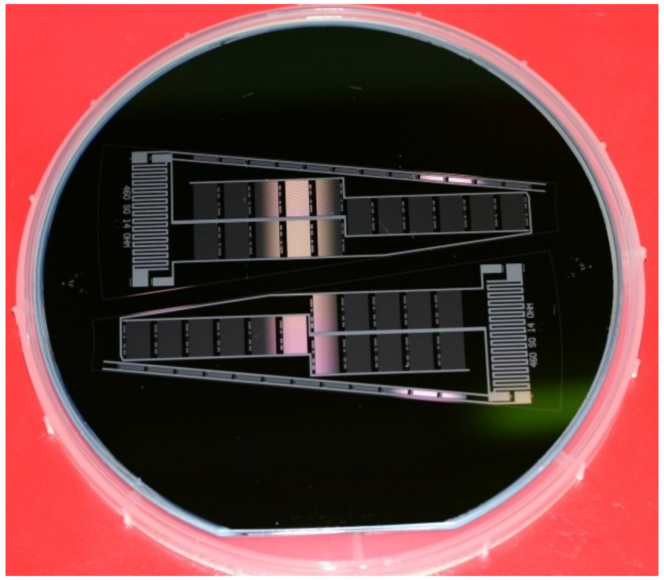


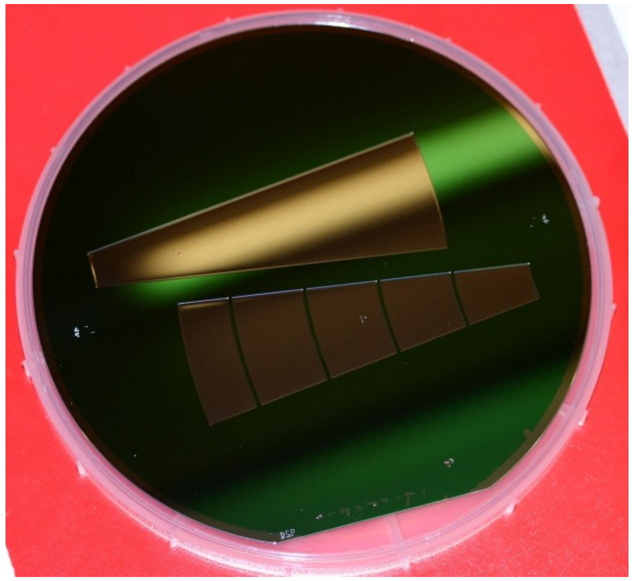


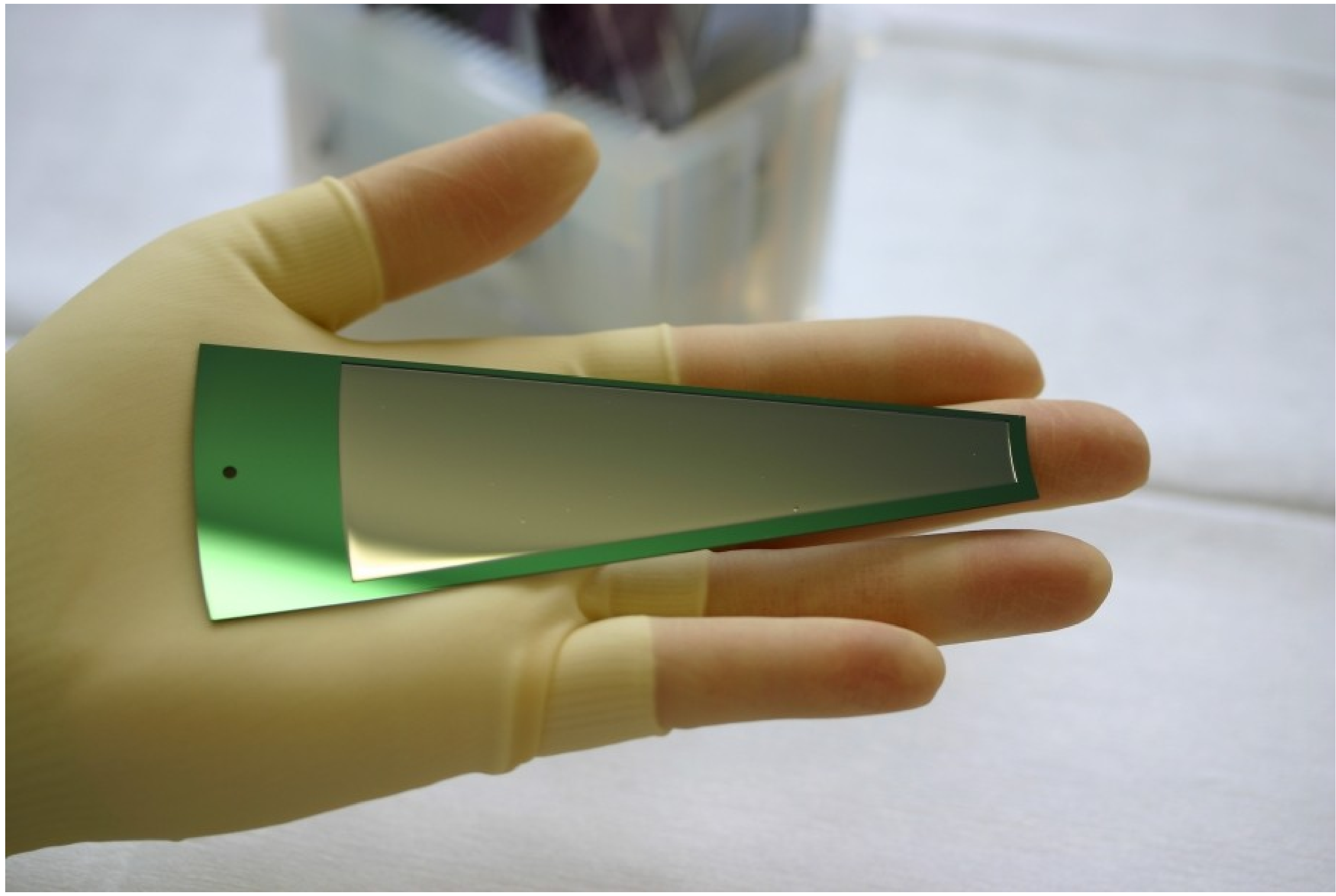
- Woking on fully engineered design + mock-up
- Hoping to learn*:*

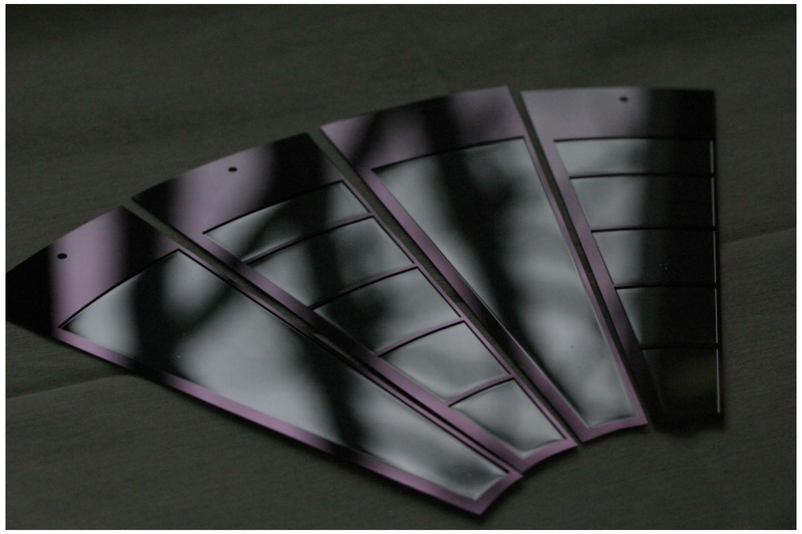
  Sensor: feasibility of layout with variable pitch & length
  Ancillary: length of switcher lines, load on DCD...
  Mechanics: self-supporting frame
  Cooling: air flow through disks
  Physics: assess performance of this design

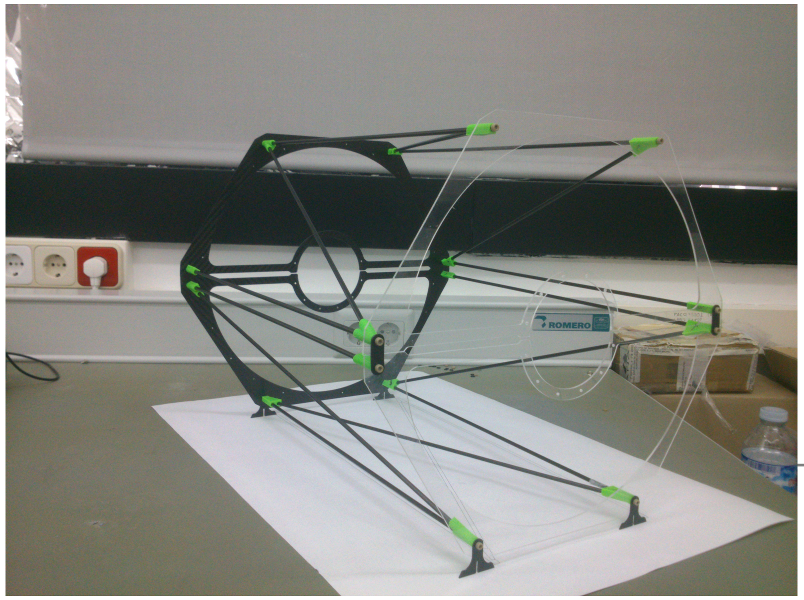
Mechanical petals for FTD mock-up



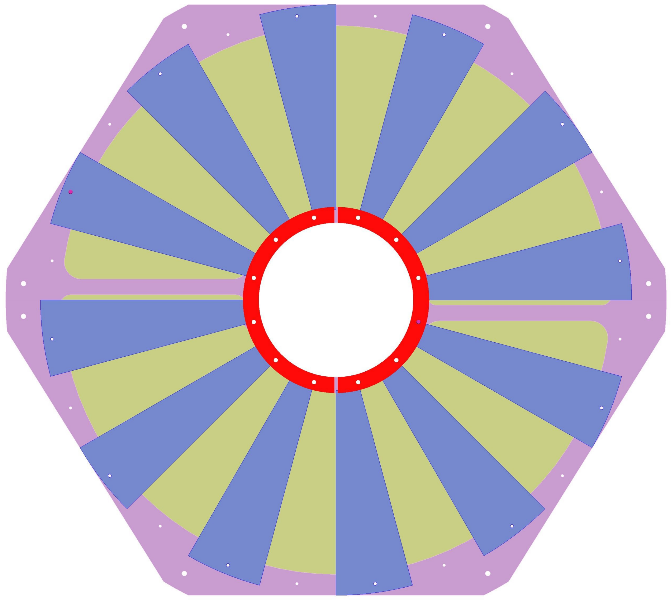








DEPFET mechanical
petals for FTD mock-up.
See “forward tracking”
talk in Thursday session

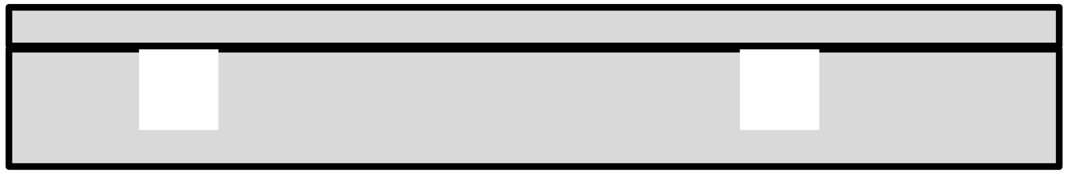


Micro-channel cooling in all-silicon ladders

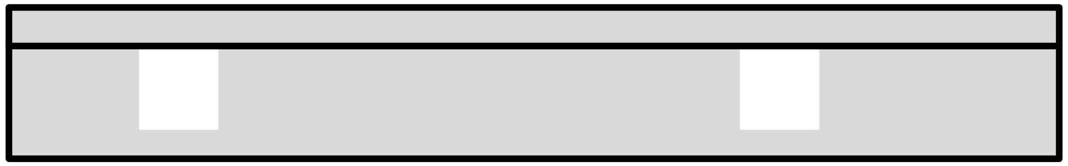
Start with oxidized handle wafer

Define lithographically micro-channels, etch oxide

Etch micro-channels, blind via

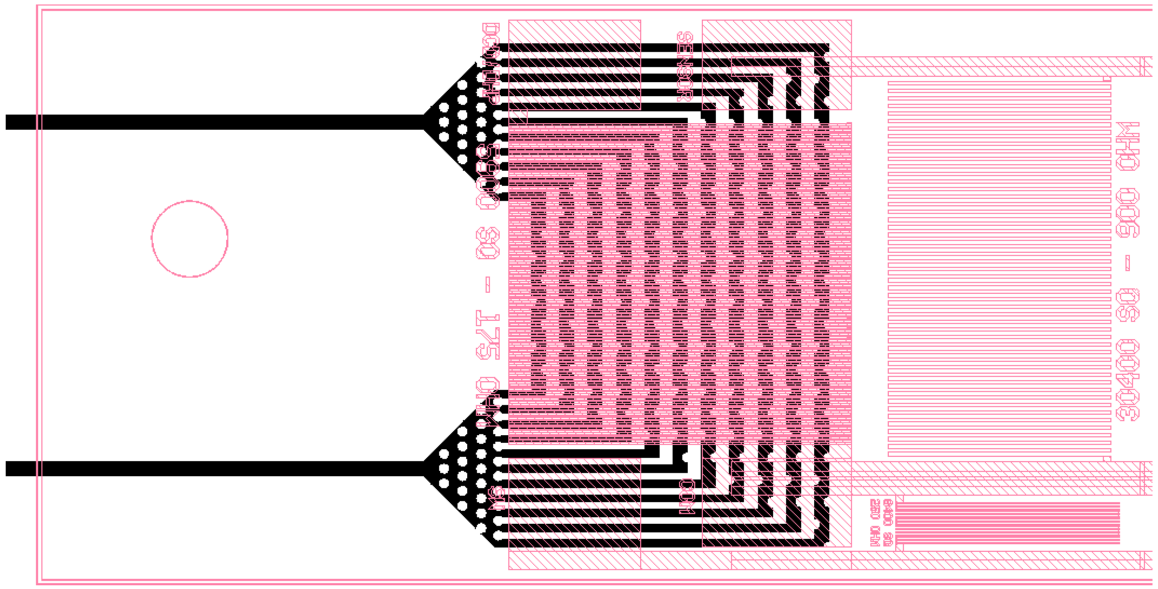


» Bond prepared top wafer as usual
» Finish SOI wafer (“Cavity SOI”)
» top wafer for DEPFETs
» Handle wafer with micro-channels under ASICs

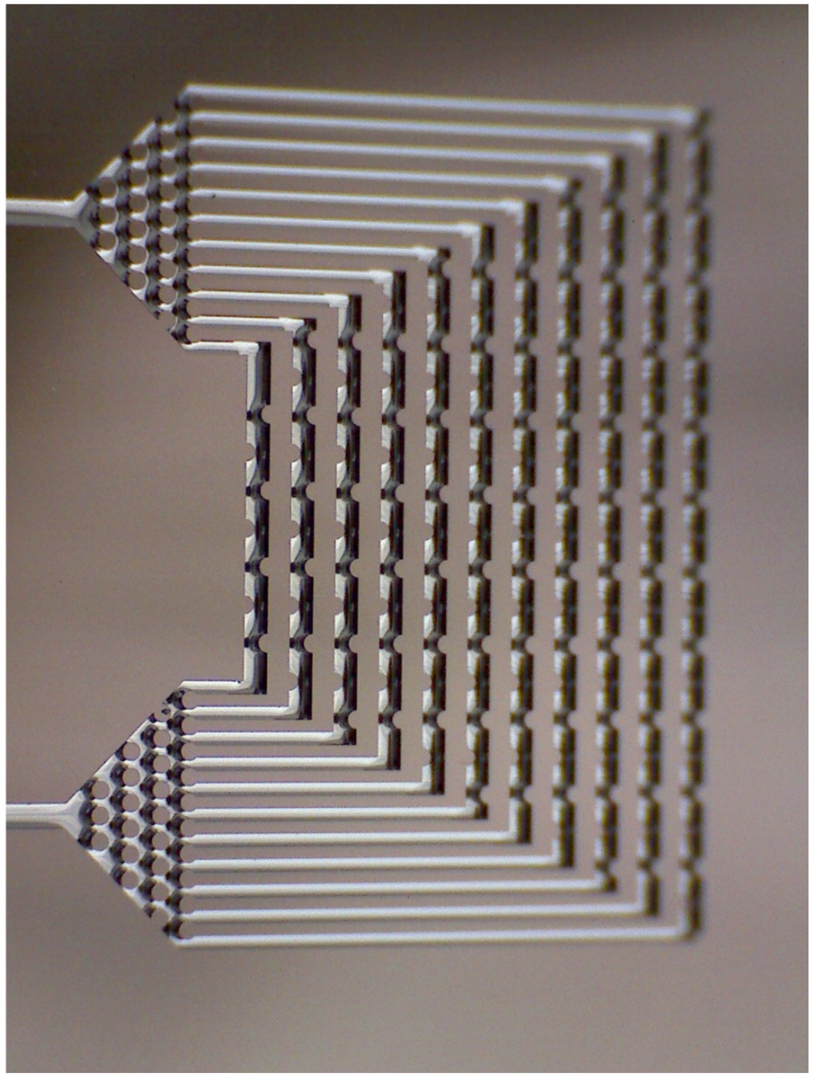


» Handle removed in sensitive area
» Channels exposed after cutting

Micro-channel cooling circuit embedded in Si-sensor

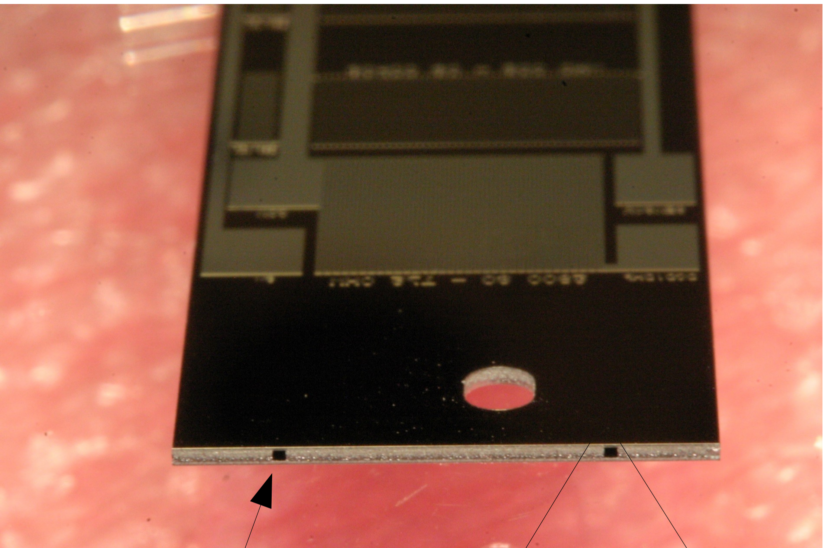


Micro-manifold right under heater circuit that represents the main power dissipation on the ladder (Front End and Digital Data Handling & Processing)



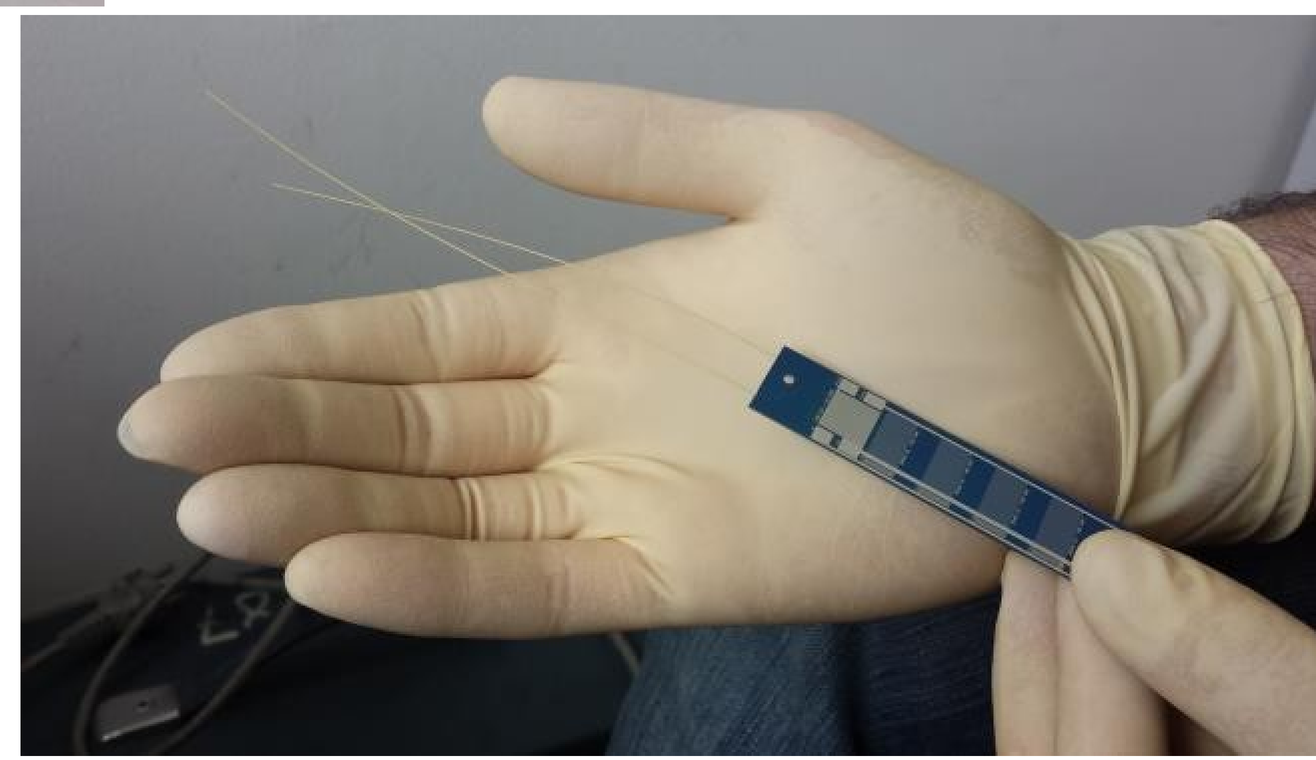
Micro-pattern in handle wafer

First samples with micro-cooling circuit

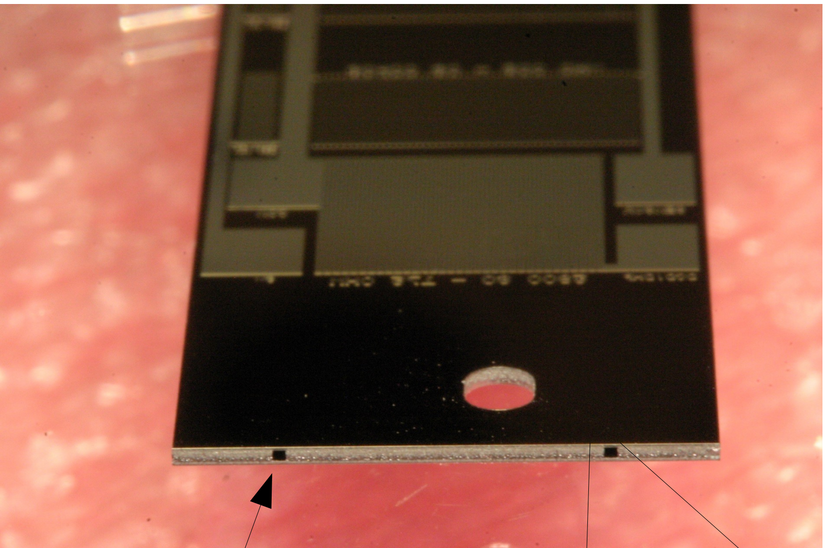


Inlet and outlet
at end-of-ladder

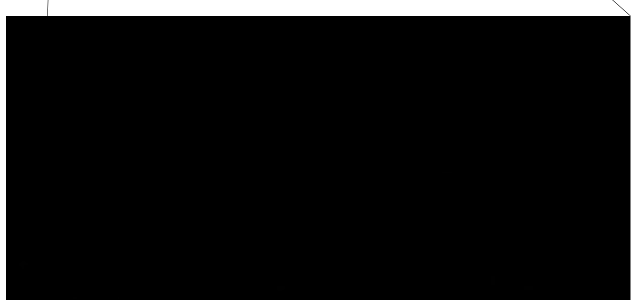
Connect to commercial
360 µm PEEK Tubes

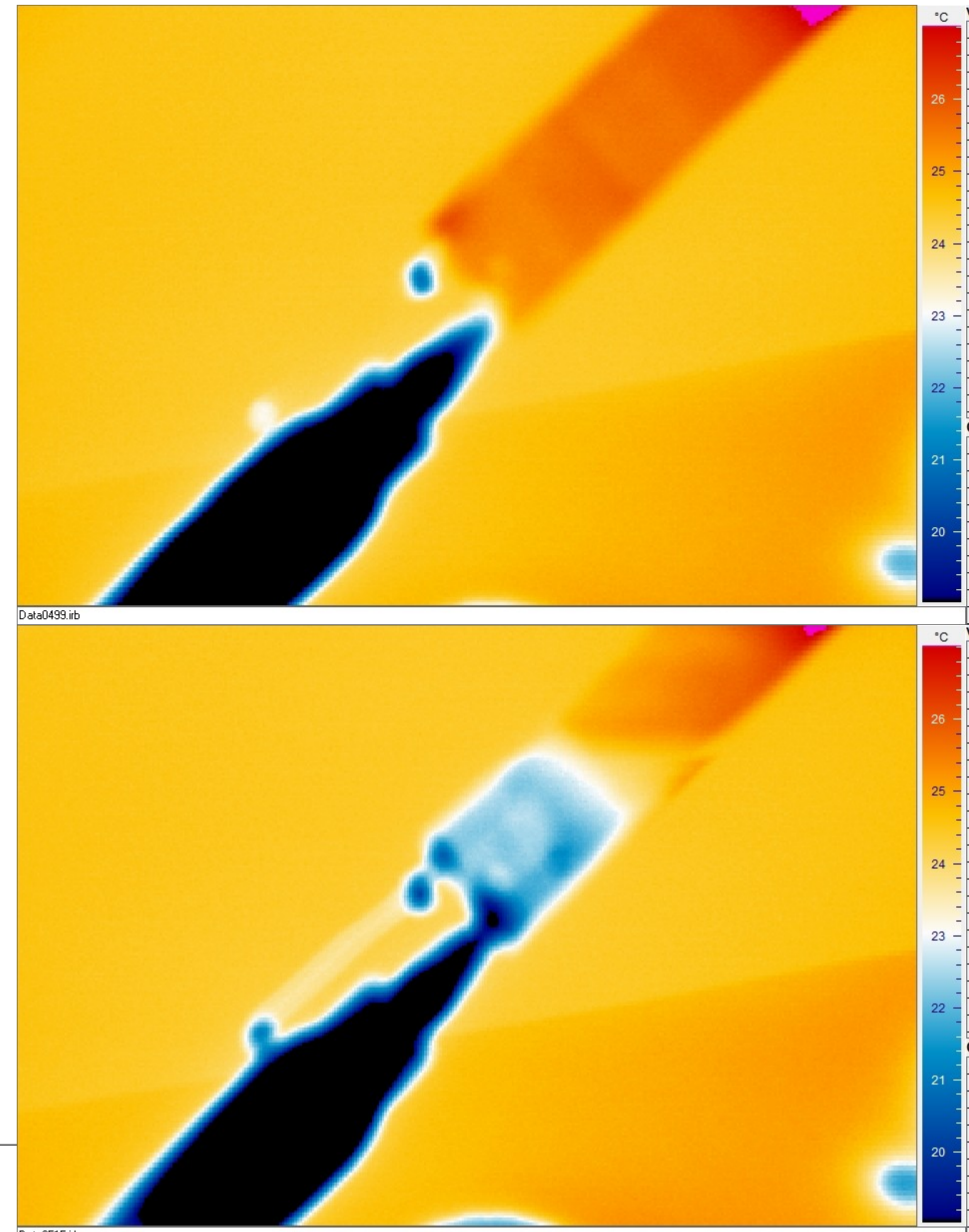


First samples with micro-cooling circuit

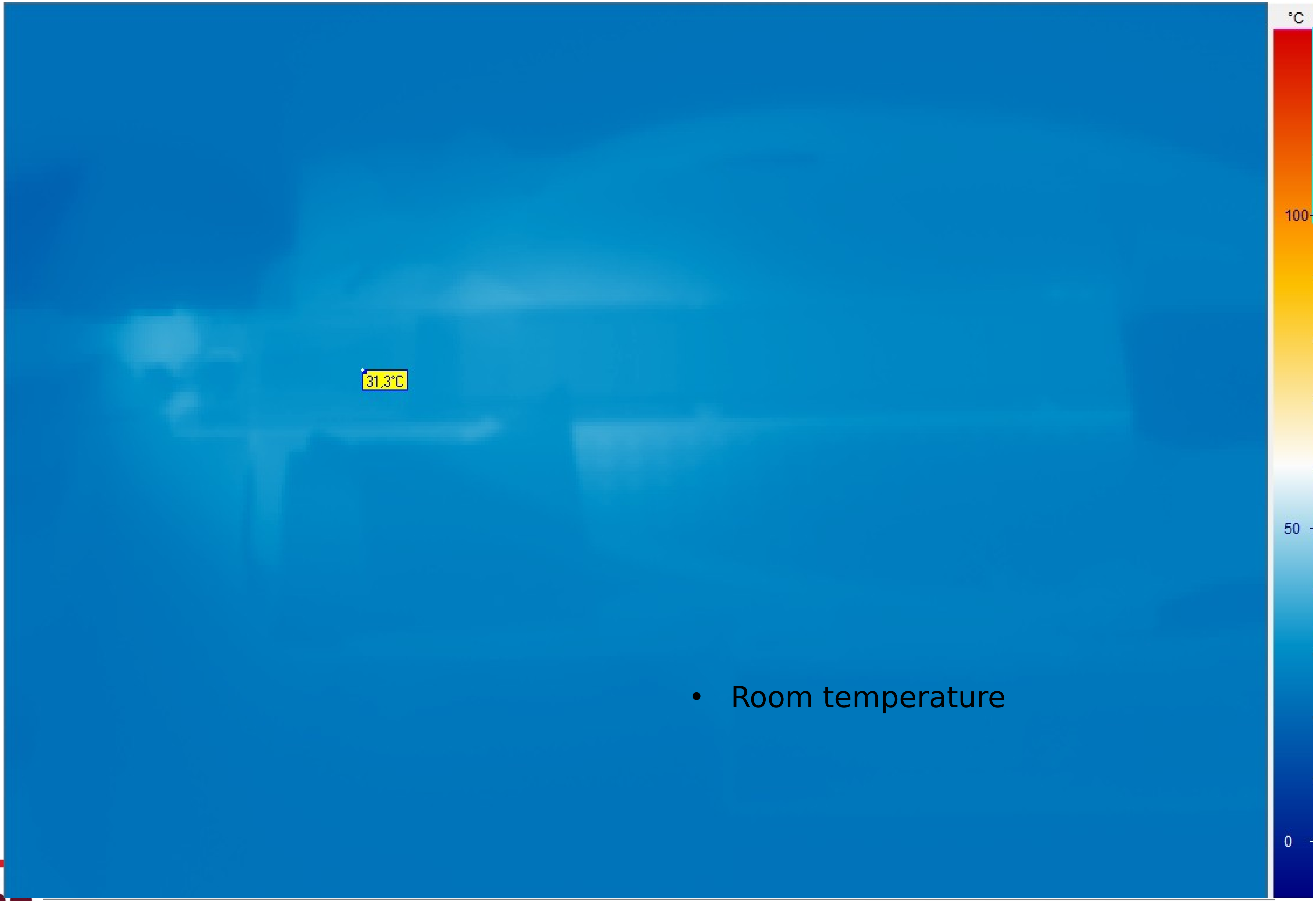


Inlet and outlet
at end-of-ladder

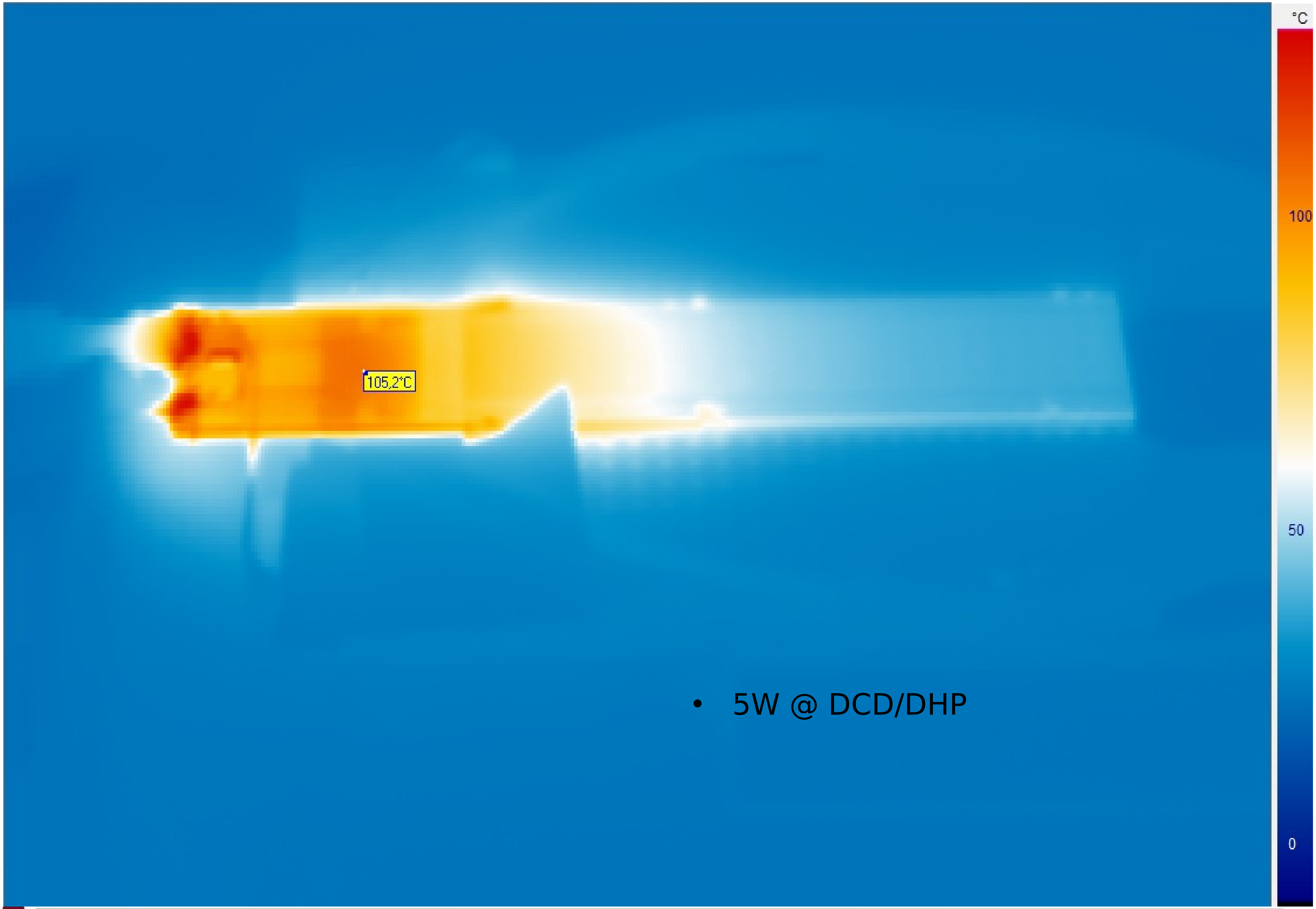




Initial – everything's cold

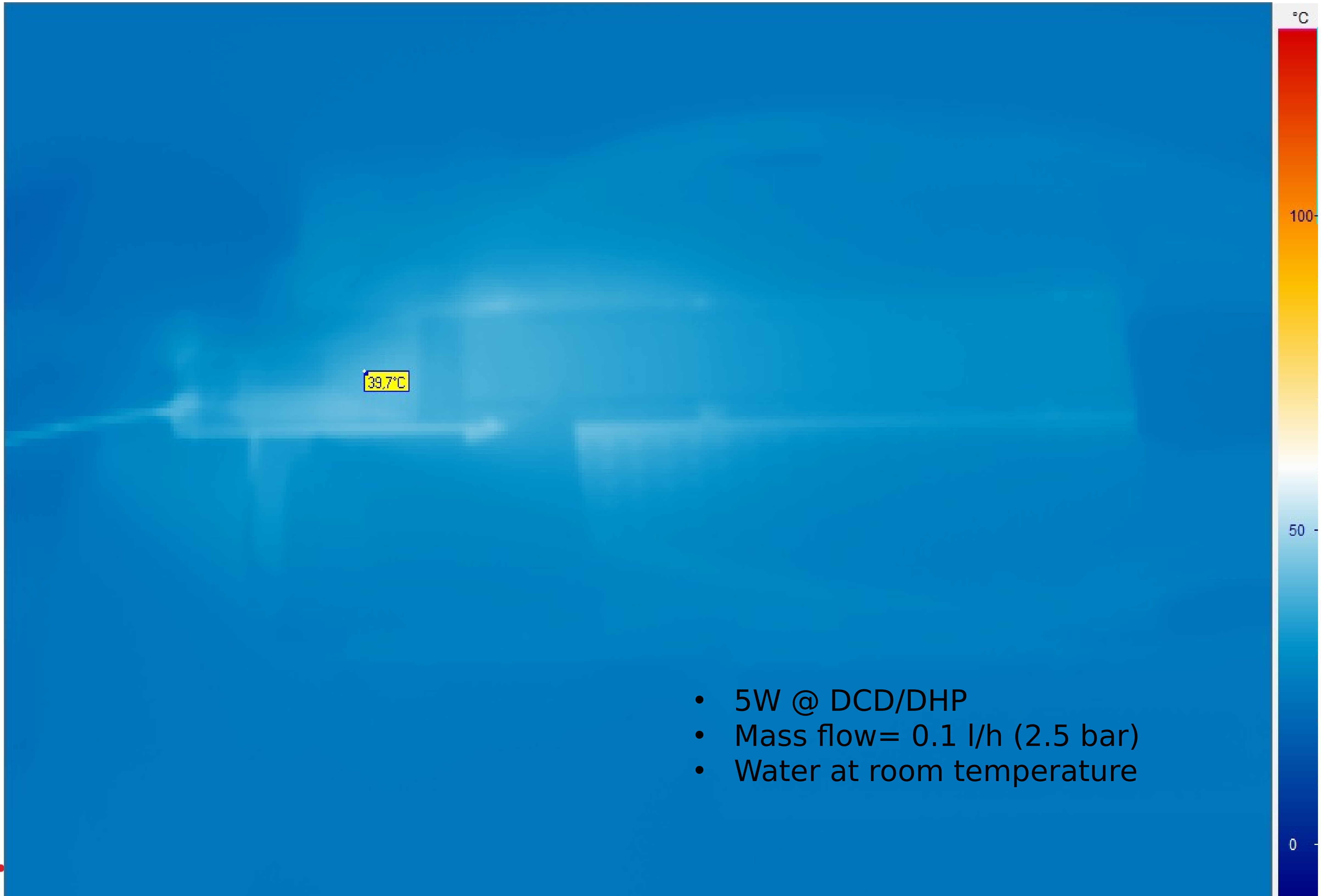


Power on – cooling off!



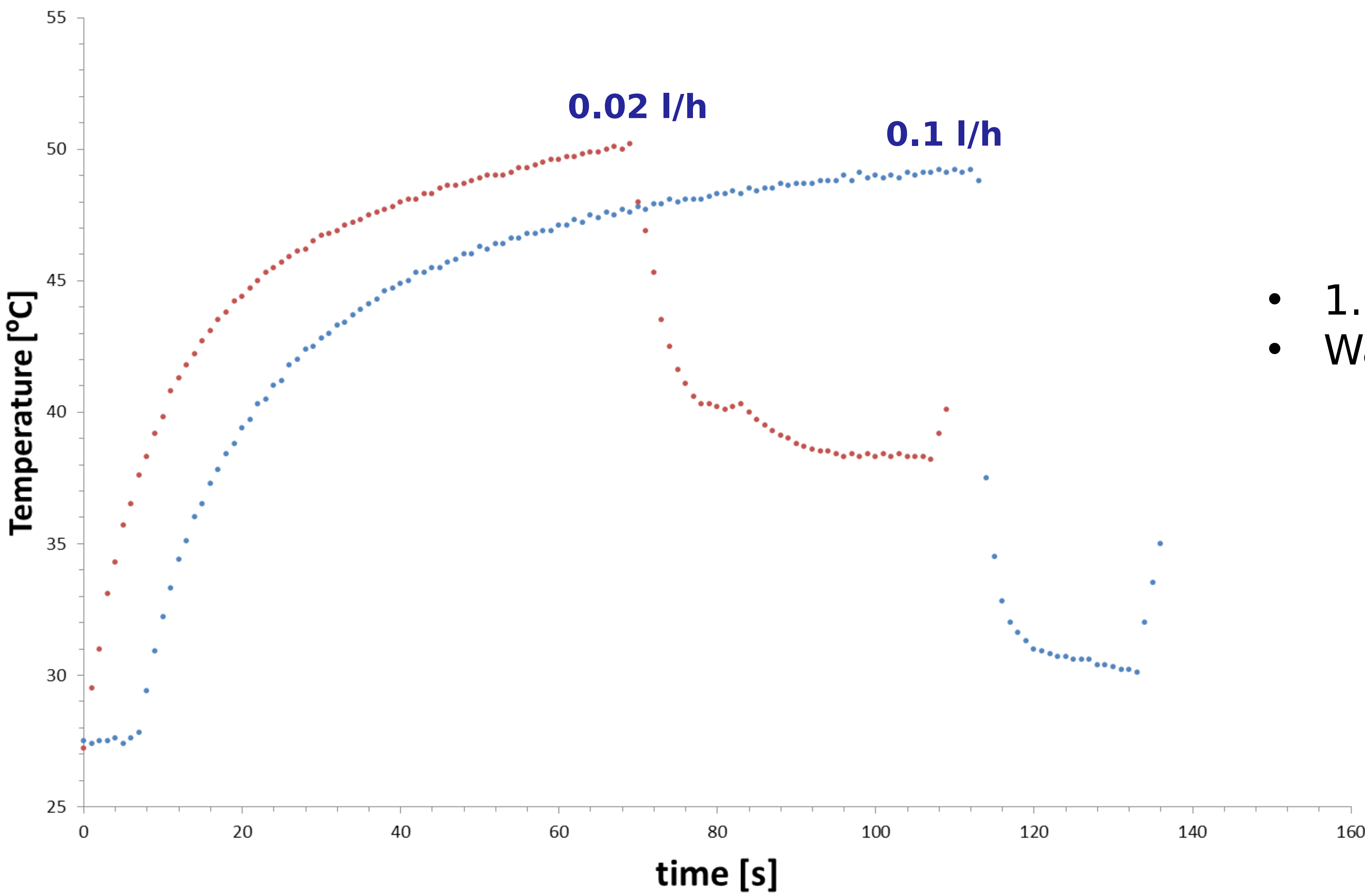
- 5W @ DCD/DHP

Power on – cooling on!



- 5W @ DCD/DHP
- Mass flow= 0.1 l/h (2.5 bar)
- Water at room temperature

Cooling vs. flow



- 1.5 W @ DCD/DHP
- Water at room tempe

DEPFET @ LC: conclusions

DEPFET remains a strong candidate for LC vertex detector

benefit from progress building the Belle II **system**
→ full-scale ladder read-out successfully in TB at DESY (January 2014)
→ complete read-out chain exercised (FE + on-ladder digital processing + off-detector)

DEPFET can meet main LC vertex detector requirements (IEEE TNS paper)
→ 2-4 μm spatial resolution (with small-pixel sensor, 20 x 20 μm^2)
→ read-out speed: 40 μs/frame for ILD layer 1 (with current DCD)
→ ladder material ~ 0.15% X_0, close to LC specification (0.21% X_0 in Belle-II)

Recent progress on ILC-specific R&D:
- power pulsing exercized on thin mechanical DEPFET sample
  (small thermal excursion as expected, no measurable impact on alignment)
- mechanical samples for FTD petals tested
  (more details in forward tracking talk)
- first attempt at micro-channel cooling & FEA simulation
  (liquid circulates and cools, small pressure and flow are sufficient)
- Learnt something about limitations of spatial resolution along the way