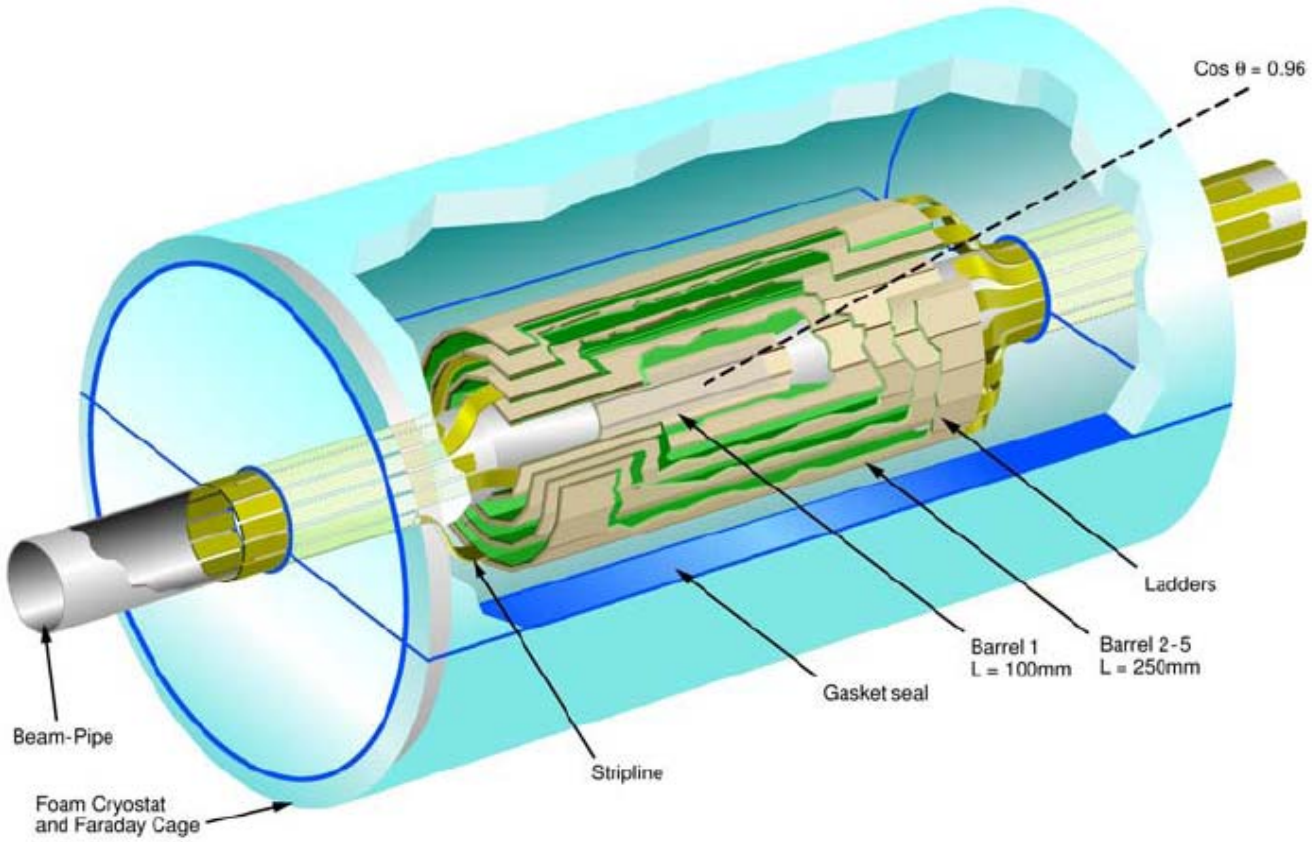
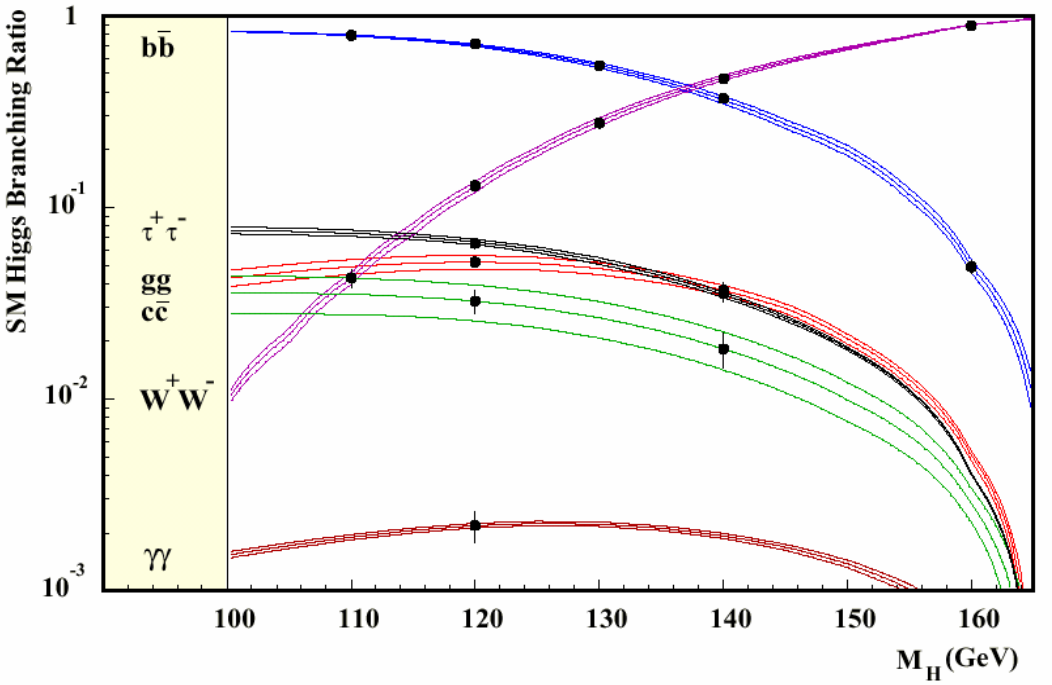
Studies of Sensors for the ILC

- Introduction
- Studies of Column Parallel CCDs
- Design of In-situ Storage Image Sensors
- CMOS sensors
- Thin support structures for silicon sensors
- Other UK plans
- Summary



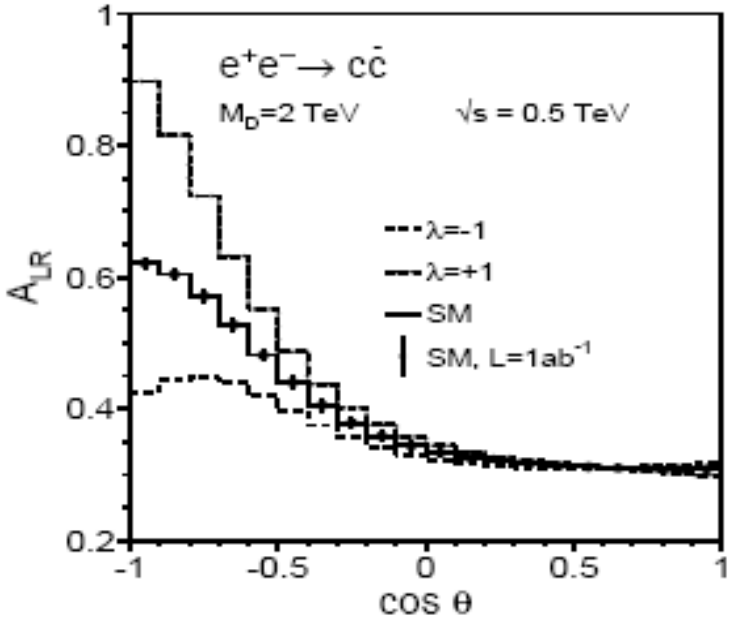
Introduction – physics at the ILC

- The Int e^+e^- LC and its detectors will allow precise measurements of cross sections, masses, branching ratios...
- E.g. Branching ratios of Higgs boson:



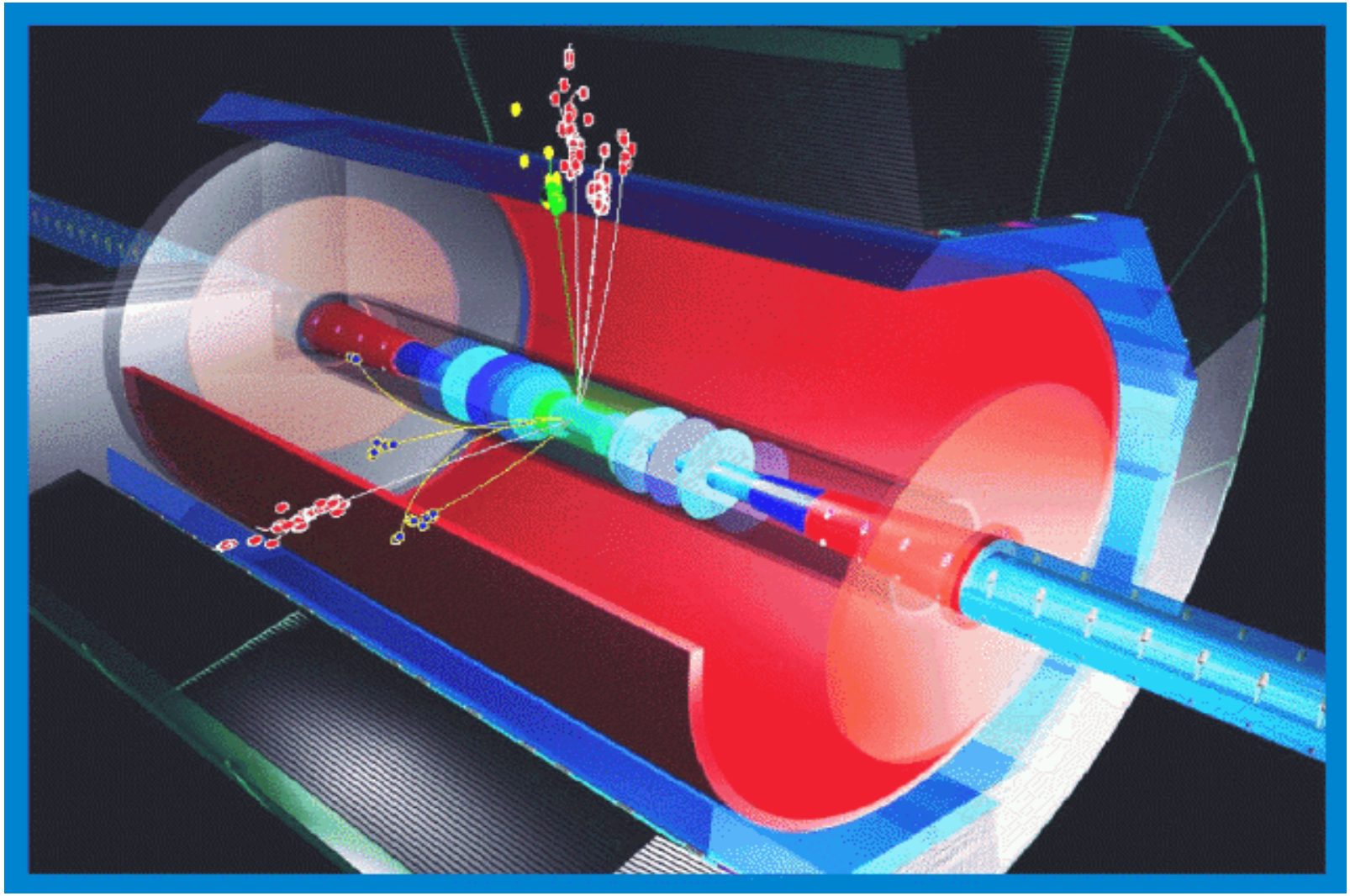
- Requires quark flavour identification.

- Contribute to understanding of mass, dark matter, structure of space-time...
- E.g. effects of large extra dimensions on $A_{LR} = (\sigma_L - \sigma_R)/\sigma_{tot}$ as a function of $\cos\theta$ in process $e^+e^- \to f\bar{f}$.



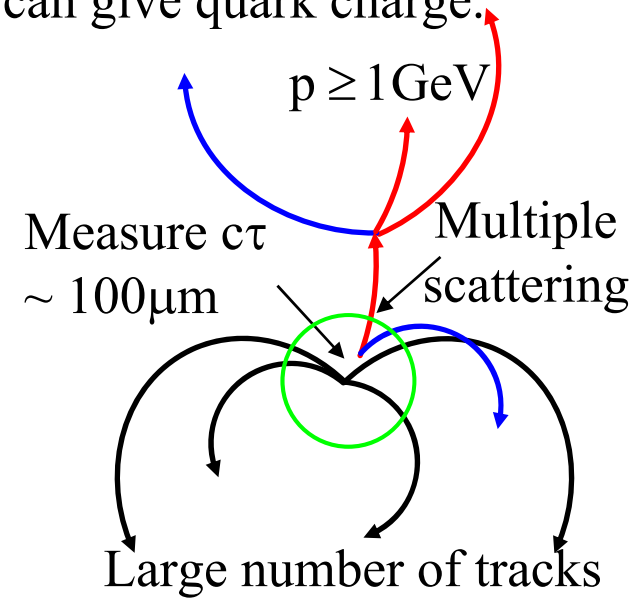
- Requires quark charge identification.

Schematic of ILC detector



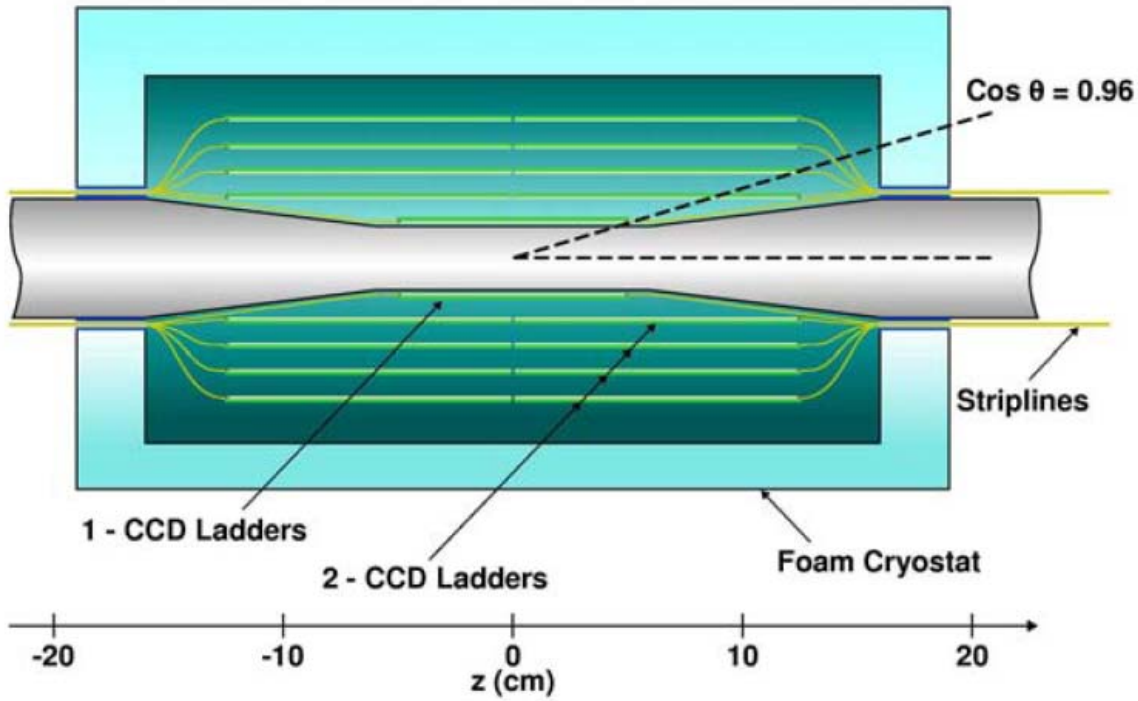
Requirements on the ILC vertex detector

- Identify quark flavour by measuring distance hadrons fly before decay.
- Net charge of particles from vertices can give quark charge.



- Point precision < 5 μm needed.
- Two track resolution < 40 μm.
- Pixels ~ 20 x 20 μm^2 suffice.

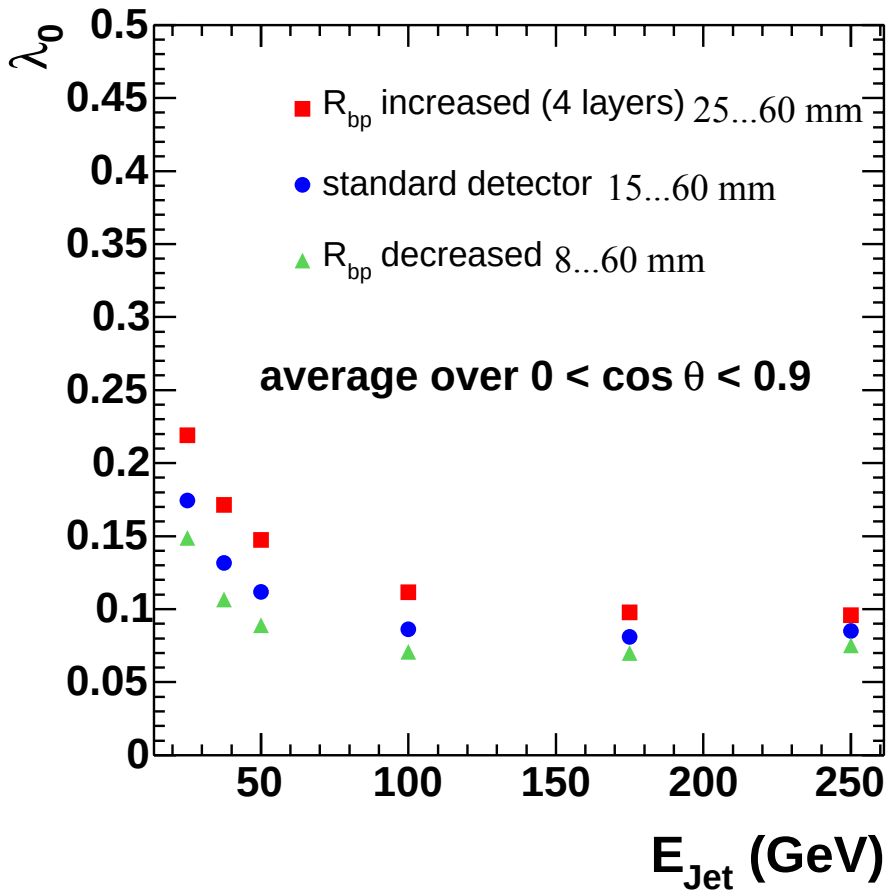
- Layer thickness < 0.1% X_0.
- First measurement at r ~ 1.5 cm.
- Need ~ 5 layers to allow pattern recognition.
- Leads to vertex detector design:



Quark charge identification performance

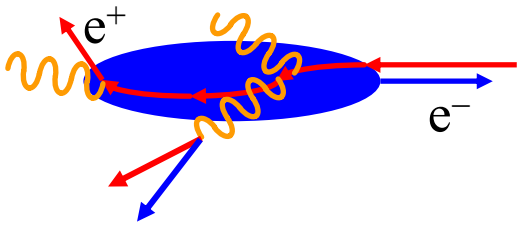
- Quantify performance in terms of λ_0, probability of reconstructing neutral B hadron as charged.
- Investigate effects of changing detector inner radius.
- Larger BP radius implies thicker BP:
  - R_{BP} = 14 mm, t = 0.4 mm.
  - R_{BP} = 25 mm, t = 1.0 mm.
- Significant loss of performance with increasing R_{BP}.
- Can express in terms of effective luminosity loss.
- For E_{Jet} = 25 GeV and R_{BP} = 25 mm, must inc. lumi. by factor ~1.7 w.r.t R_{BP} = 15 mm to get same error.

- λ_0 for different detector configurations:

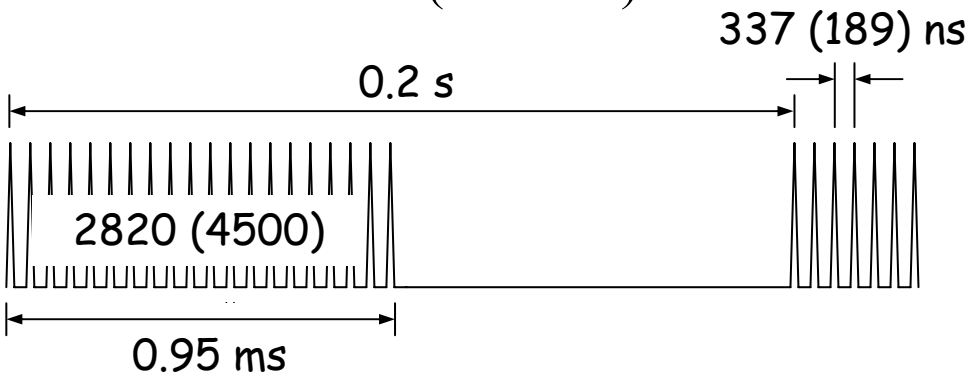


Constraints on the vertex detector due to the ILC

- Beamstrahlung...



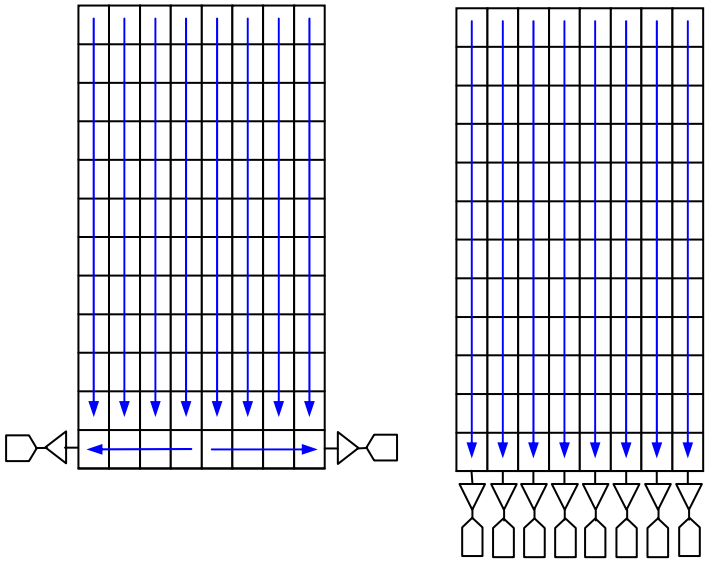
- ...results in production of ~ 5 hits/cm^2 each bunch crossing in inner layer (B = 4T, $\sqrt{s}$ = 500 GeV).
- Time structure of beam at $\sqrt{s}$ ~ 500 Gev (~ 1 TeV):



- Readout pixels 20 times in bunch train at $\sqrt{s}$ = 500 Gev, i.e. ~ every 50 μs, if want occupancy ~ 0.3%.
- Radiation dose ~ 20 krad p.a.
- Neutron background from interactions of e^+ and e^- in beam dumps ~ 10^9 1 MeV n/cm^2 p.a.
- Electromagnetic interference generated by e^+ and e^- beams.
- Beam induced pick-up disabled the electronics of the SLD vertex detector for ~ 1 μs after each bunch crossing.

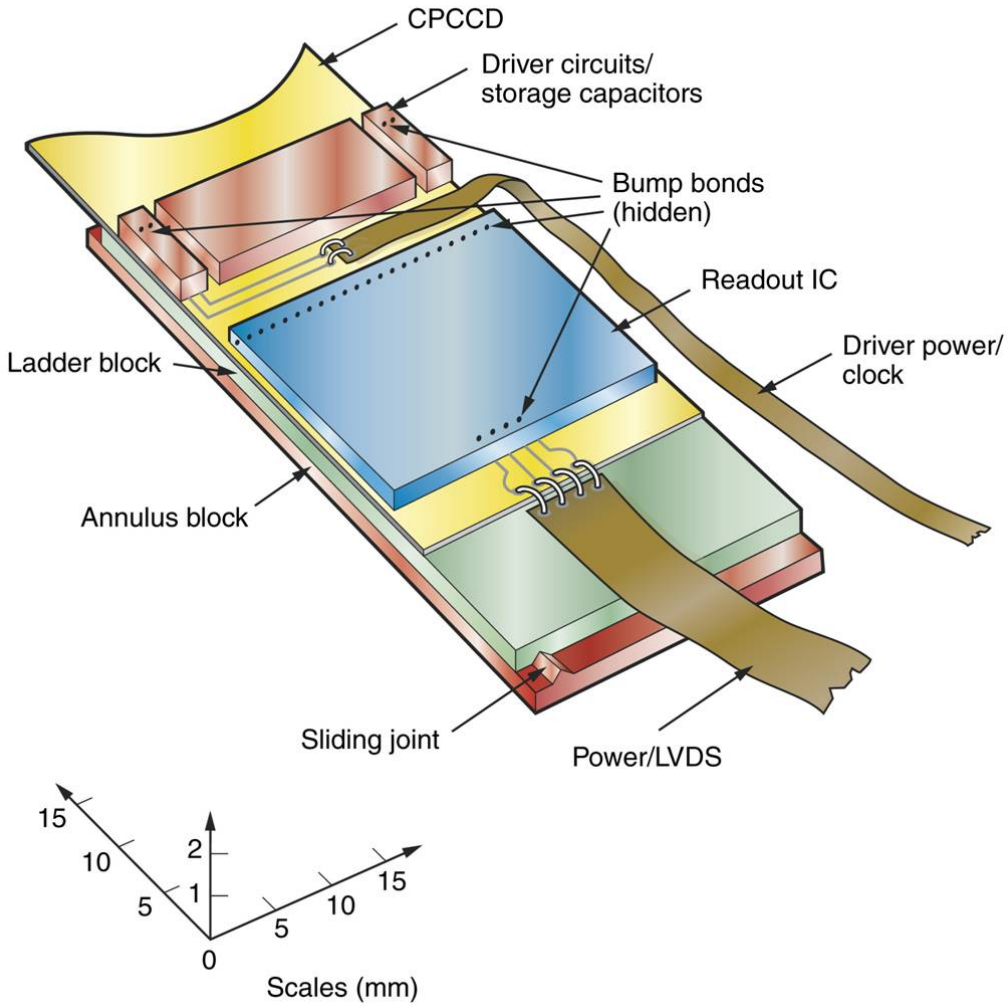
Column Parallel CCDs

- Achieve necessary readout speed with CCDs using column parallel architecture:



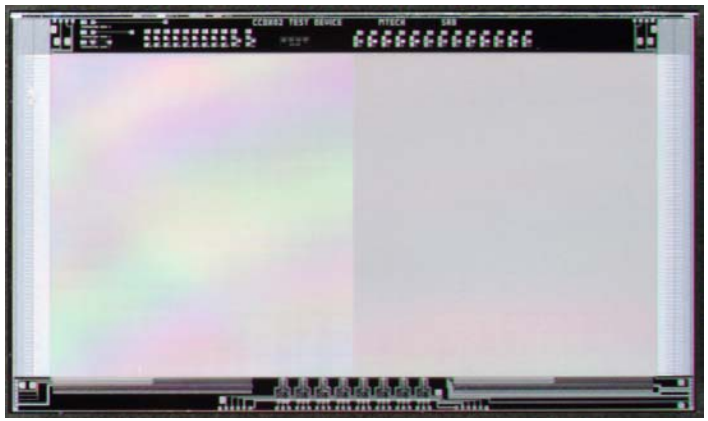
- Must drive image register at 50 MHz to readout in 50 μs.

- Conceptual "ladder" design:



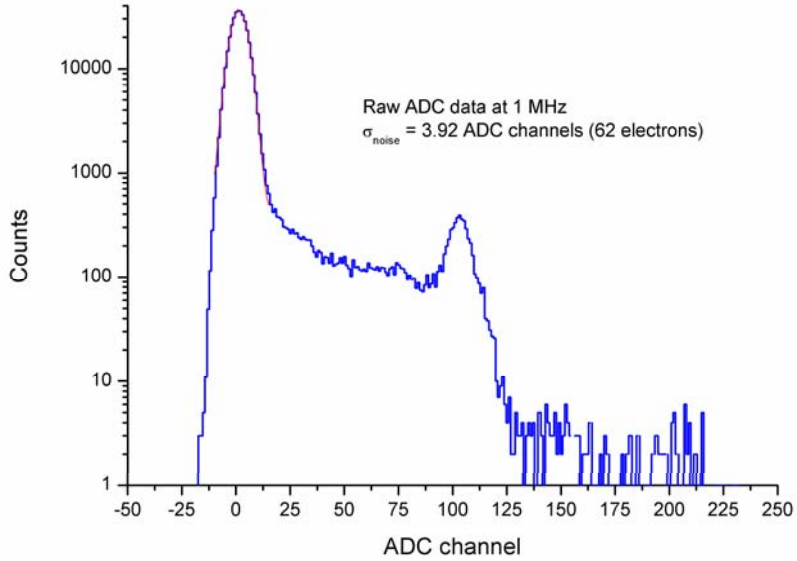
CPC1

- First of these, CPC1, manufactured by e2v.



- Two phase, 400 (V) × 750 (H) pixels of size 20 × 20 μm^2.
- Metal strapping of clock gates.
- Two-stage and one-stage source follower and direct (charge) outputs.

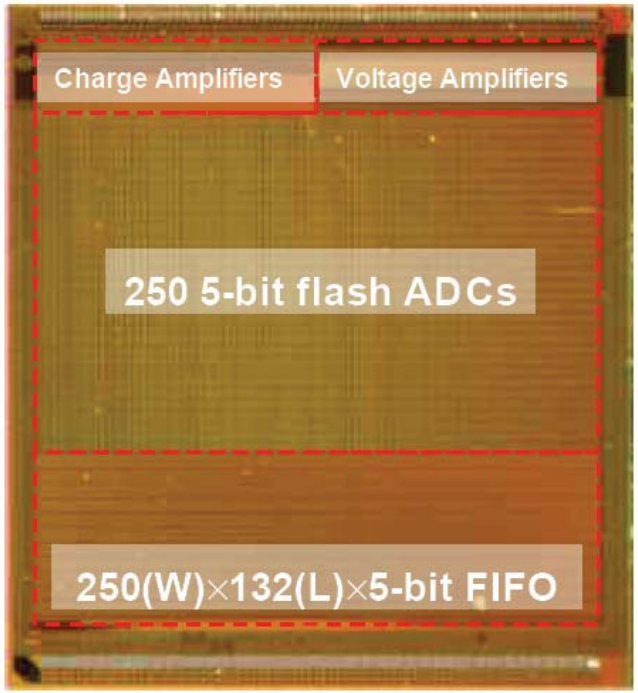
- Standalone CPC1 tests:
- Noise ~ 100 e$^-$ (60 e$^-$ after filter).
- Minimum clock potential ~1.9 V.



- Max clock frequency above 25 MHz (design 1 MHz).

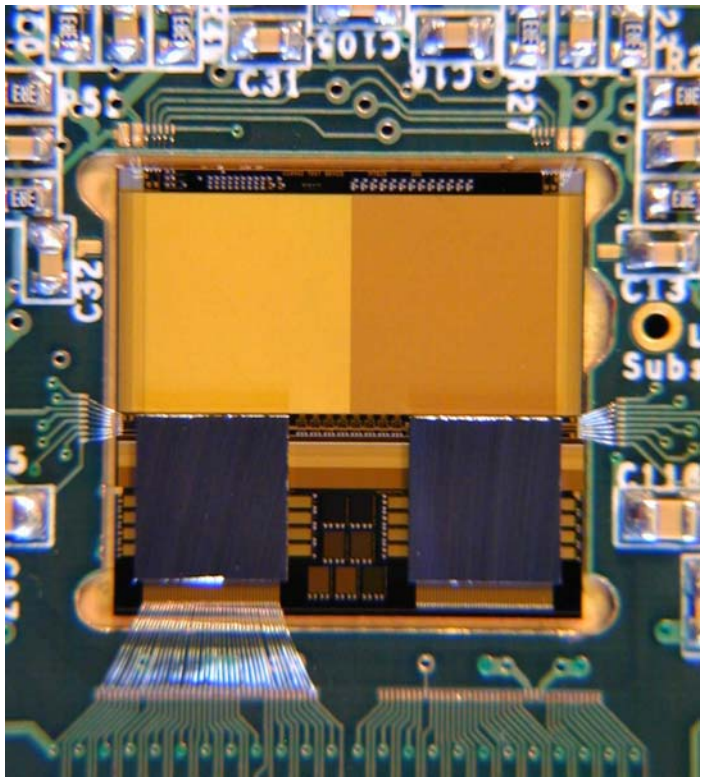
CPC1 bump-bonded to CPR1 readout chip

- Marry with CMOS CPCCD readout ASIC, CPR1 (RAL):



- IBM 0.25 μm process.
- 20 μm pitch, designed for 50 MHz.

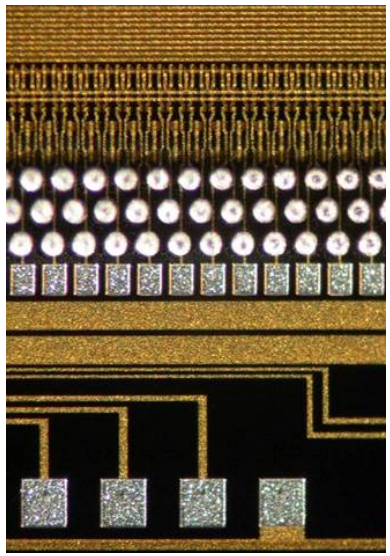
- Bump bonding performed by VTT:



- First time e2v CCDs bump bonded.

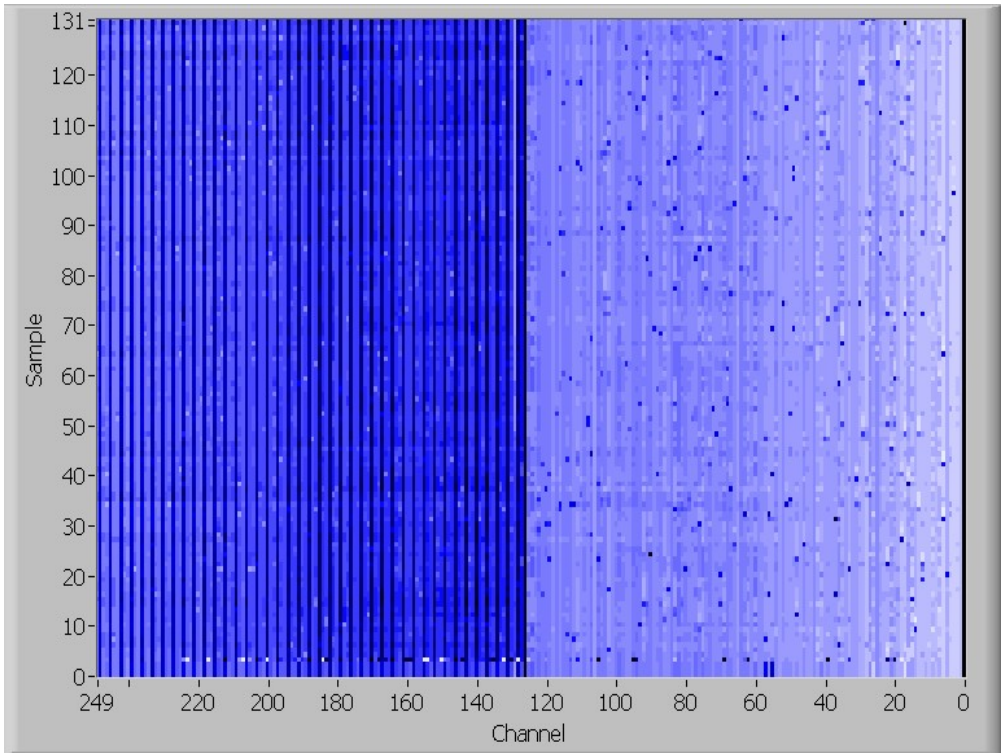
CPC1 bump bonded to CPR1 readout chip

- Bump bonds are good, as visible under microscope...



- ...but yield of functioning assemblies only 30%.

- 6.9 keV X-ray hits, 1 MHz column parallel readout:



Inv. charge o/ps
(+ ive signals)
noise ≈100 e-

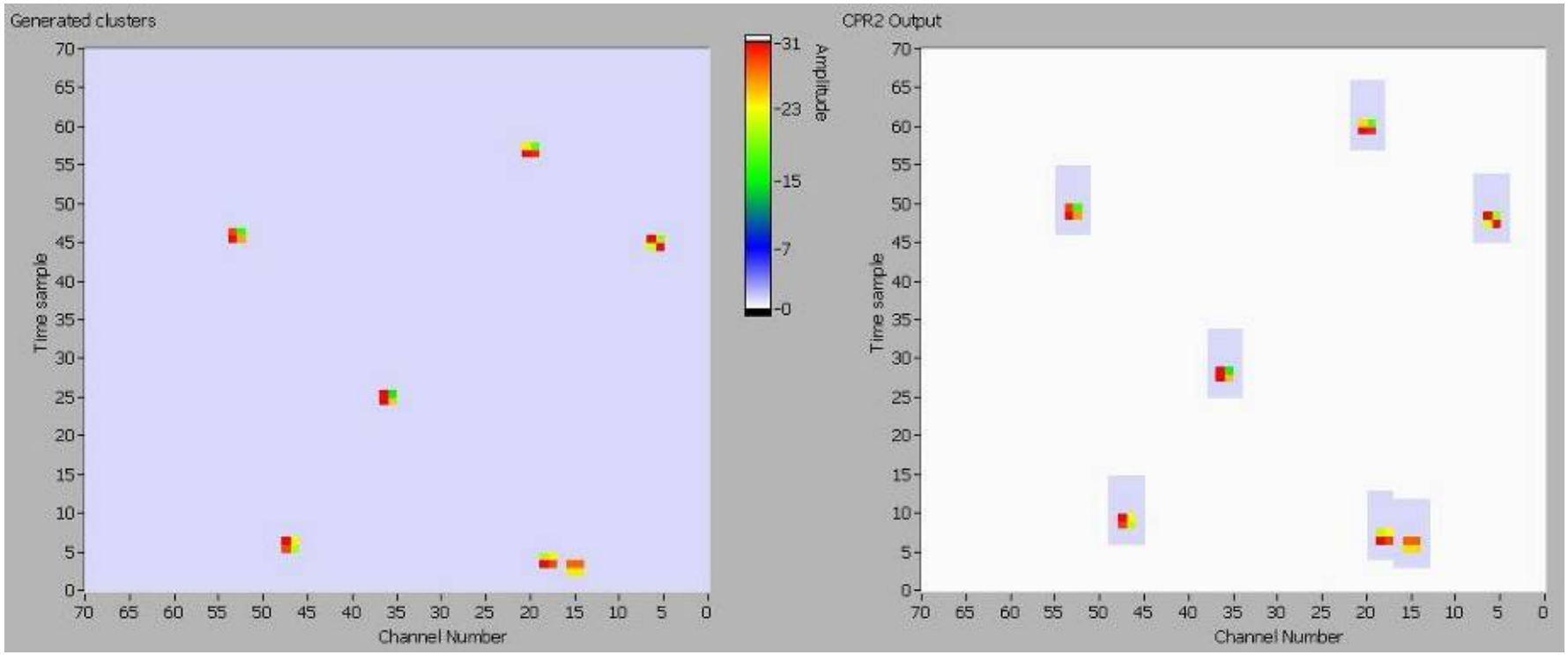
Non-inv. volt. o/ps
(- ive signals)
noise ≈ 60 e-

Next generation CPCCD readout chip, CPR2

- CPR2 designed for CPC2 by the Microelectronics Group at RAL.
- All problems identified with CPR1 rectified.
- Many additional features to improve testing.
- Size: 6×9.5 mm^{2}.
- IBM 0.25 µm CMOS process.
- First tests now completed.

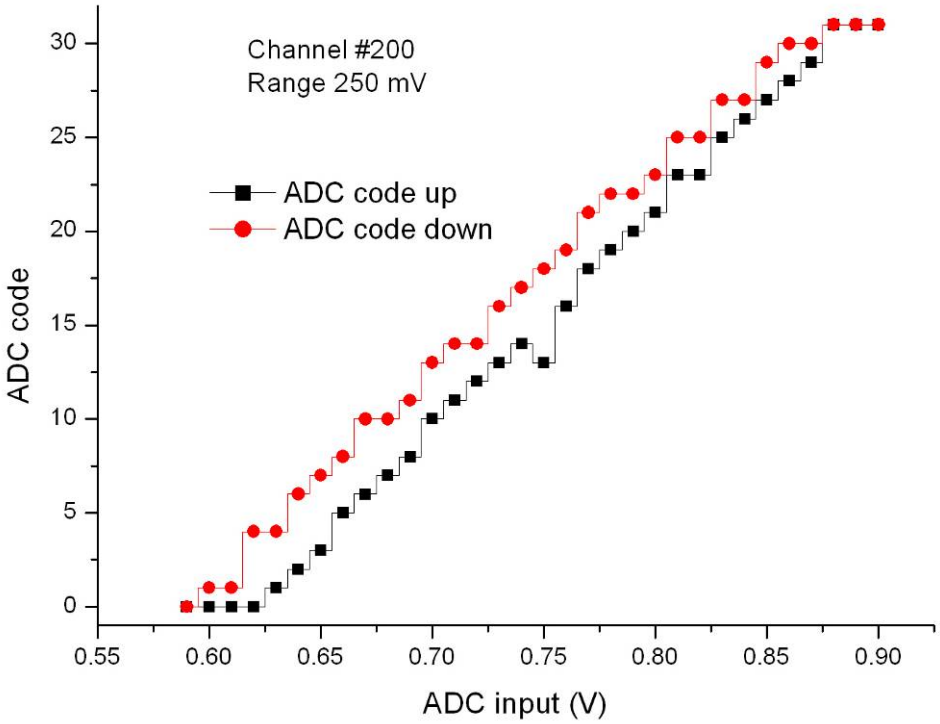
Next generation readout chip – CPR2

- Test clusters in:
- Sparsified data out:



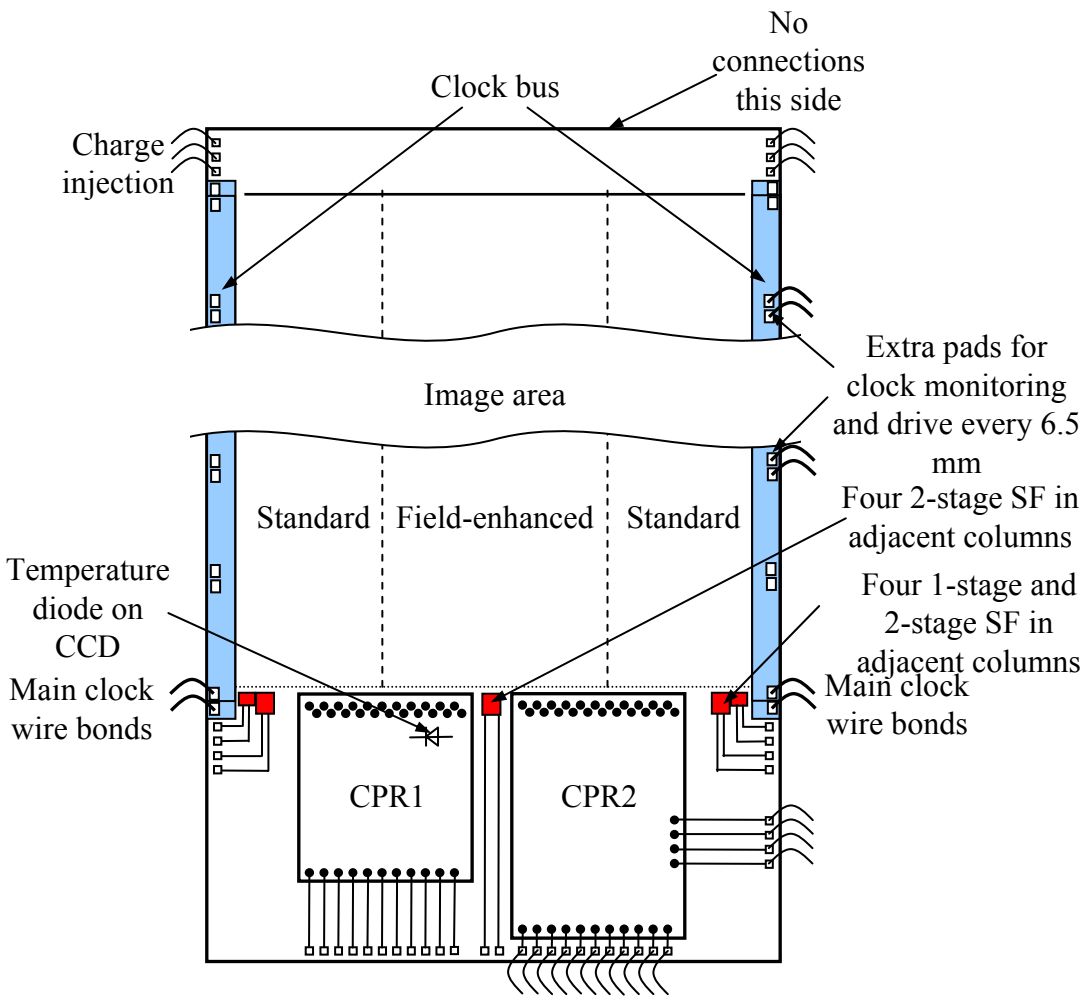
Next generation readout chip – CPR2

- Test analogue-to-digital conversion:



- Hysteresis in the ADC transfer curve:
  - Charge coupling between digital and analogue circuitry in the ADC comparators.
  - Should be much less than 1 x LSB.
- At least two ways to solve it for next chip, CPR2a:
  - Reduce transistor size (less gate charge).
  - Separate analogue and digital signals using switch.
- CPR2a design largely complete, start work on CPCCD drive: major challenge remaining for this sensor.

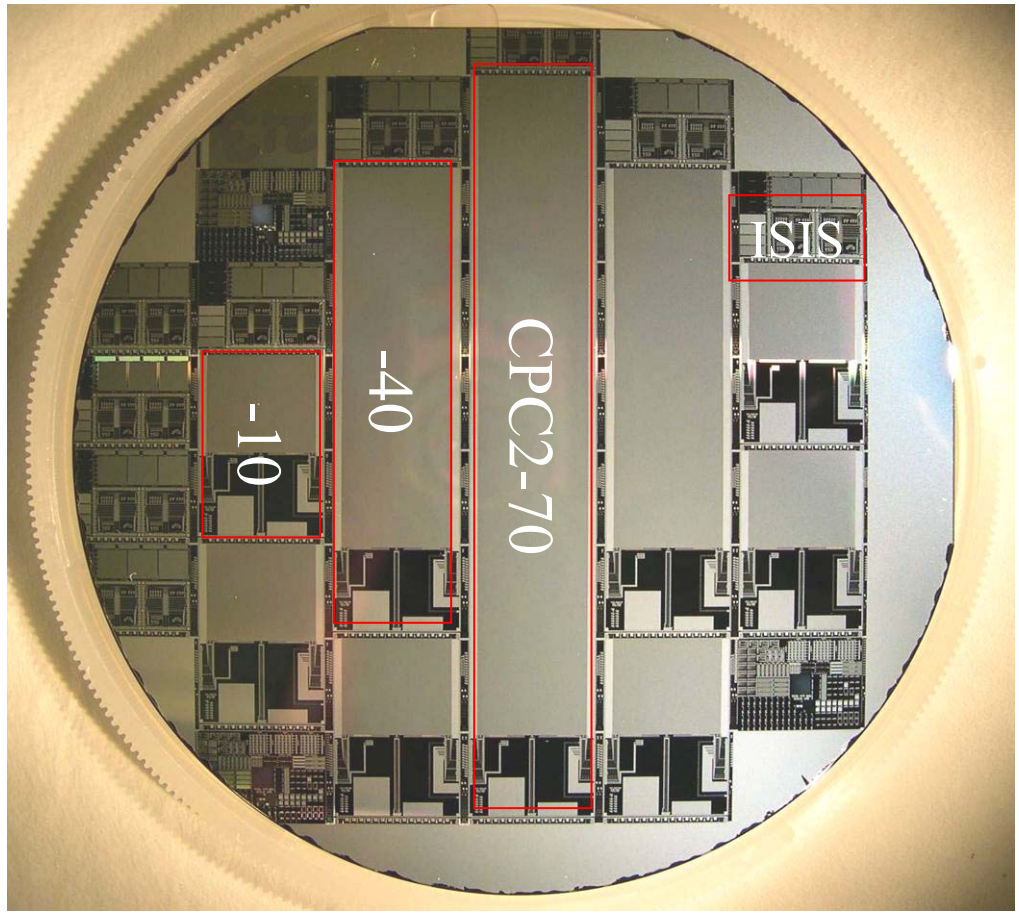
Next generation CPCCD – CPC2



- Compatible with CPR1 and CPR2
- Two charge transport sections.
- Choice of epitaxial layers giving different depletion depths: 100 Ω cm (25 μm thick) and 1.5 kΩ cm (50 μm thick)
- Design allows few MHz operation for CPC2-70.
- Hope to achieve 50 MHz with small CPC2s.

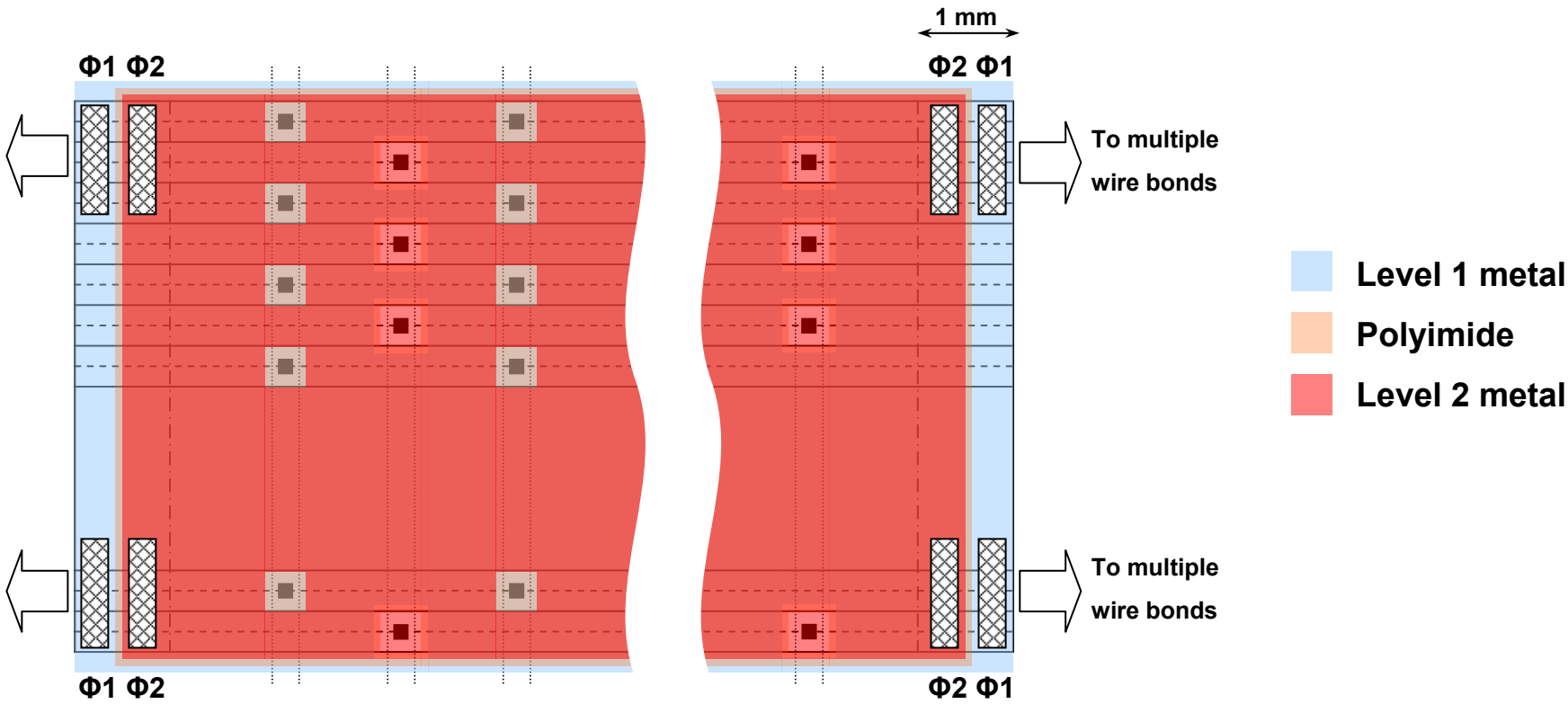
CPC2

- Three chip sizes on CPC2 wafer:
  - CPC2-70: 92 × 15 mm^2 image area.
  - CPC2-40: 53 × 15 mm^2.
  - CPC2-10: 13 × 15 mm^2.



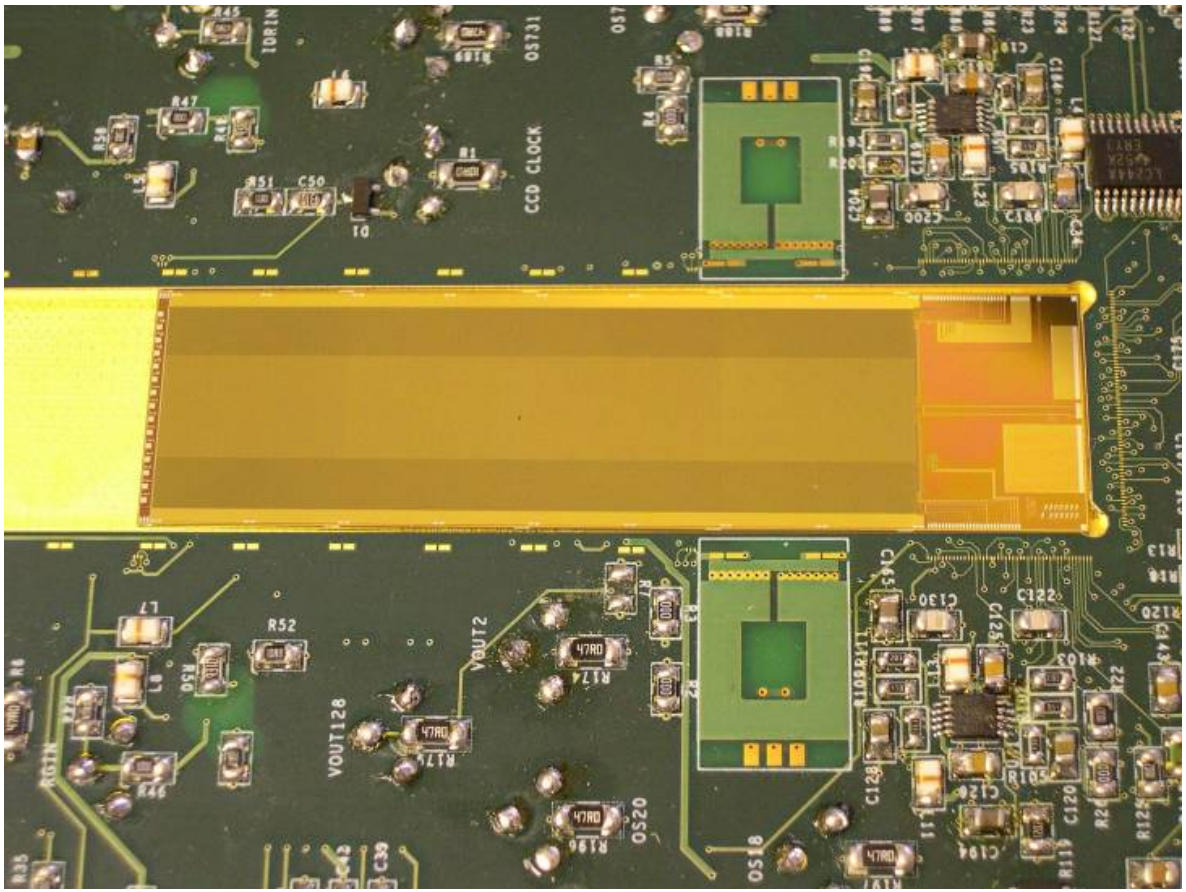
CPC2 clock distribution

- Novel idea for high-speed clock propagation, “busline-free” CCD:



CPC2

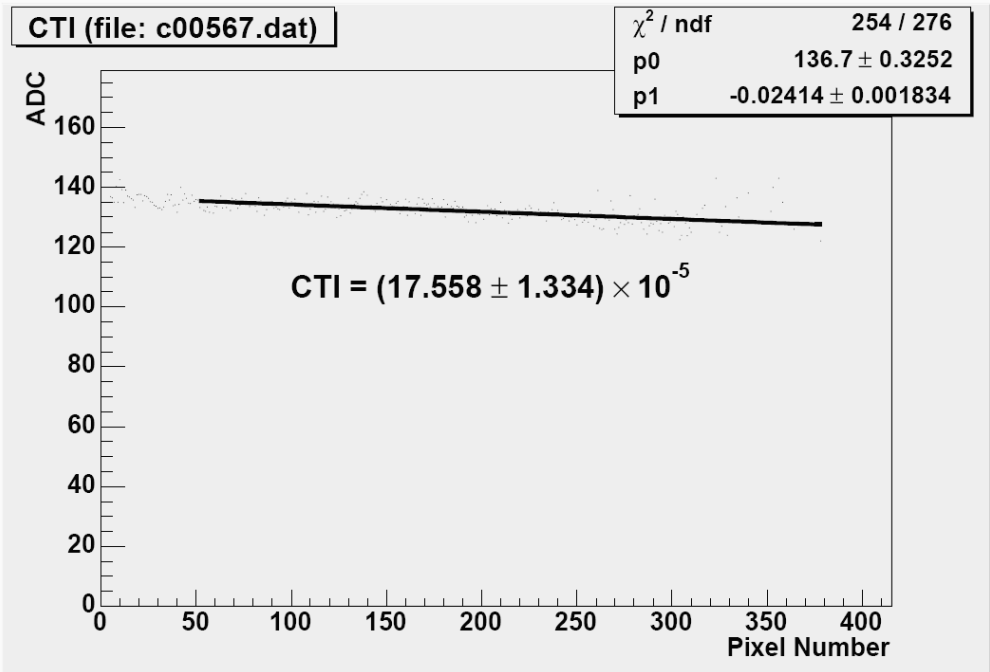
- CPC2-40 on motherboard awaiting testing:



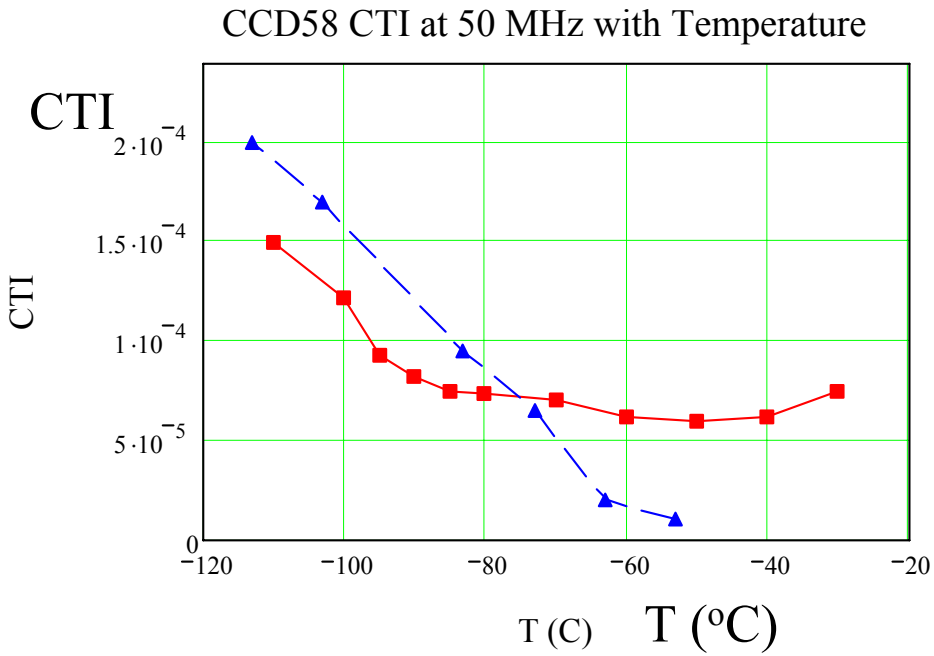
- (See Konstantin Stefanov's talk at Vertex05 for more details)

CCD radiation hardness tests

- Study CTI in CCD58 before and after irradiation (^{90}Sr 30 krad).
- Measure decrease in charge from ^{55}Fe X-rays as func. of number of pixels through which charge transferred.



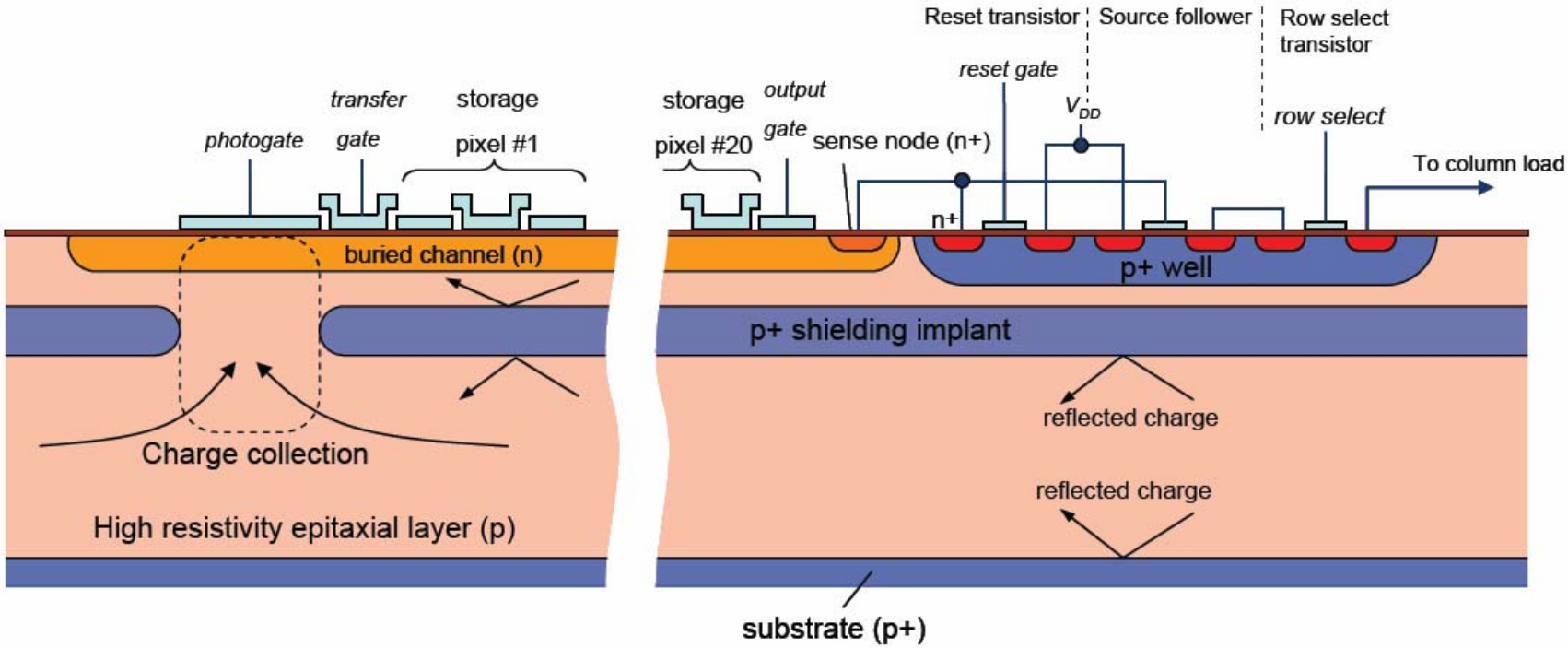
- Compare data with simulations performed using ISE-TCAD.



- Extend to CPCCD in 2006.

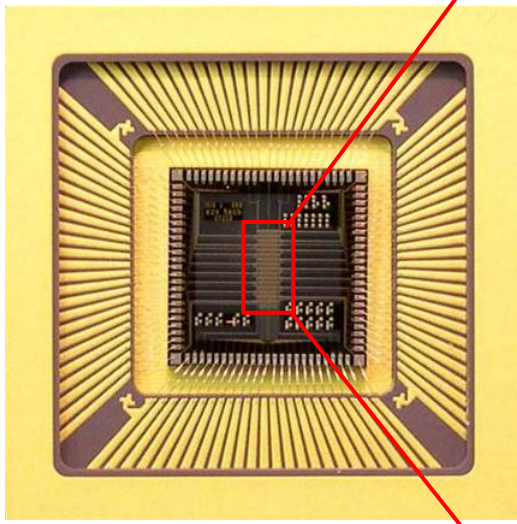
Principle of the ISIS

- CPCCD, charge-to-voltage conversion during bunch train, susceptible to pick-up?
- In-situ Storage Image Sensor (ISIS) eliminates this problem.
- Charge is collected under photogate, transferred to storage CCD 20 times during the 1 ms bunch train, then converted to voltage and read out in 200 ms quiet period after bunch train: column parallel readout at 1 MHz sufficient.



First ISIS tests

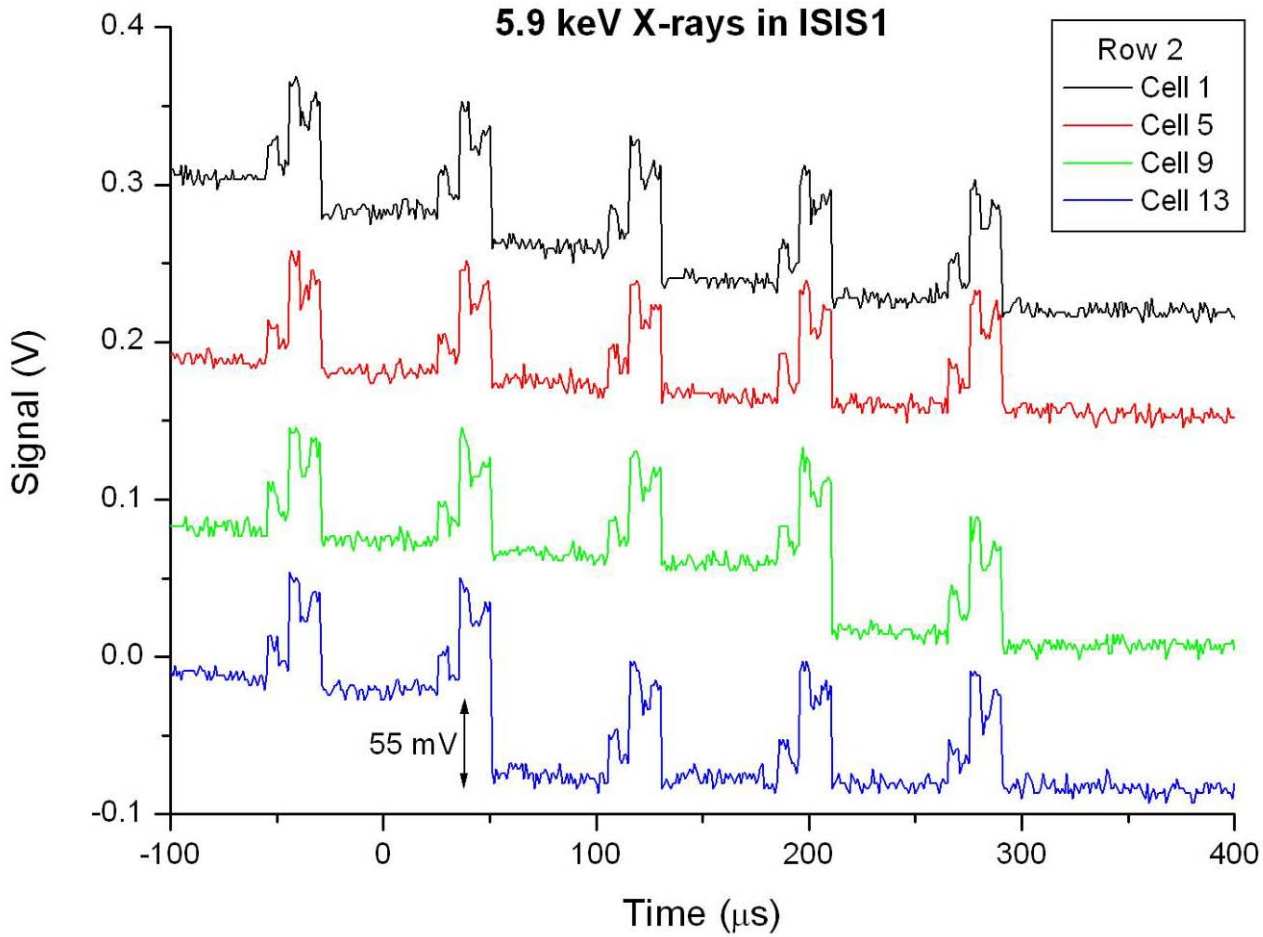
- "Proof of principle" device designed by e2V technologies.
- Array of 16 ×16 pixels with CCD storage register (5 cells) in each pixel.
- ISIS1 in 100-pin PGA carrier →



- Pixel pitch 40 × 160 μm^2, no edge logic (pure CCD process).
- Size ≈ 6.5 × 6.5 mm^2.

First X-ray signals from ISIS1

- Observe “steps” with correct amplitude: 3 μV/e⁻ × 1620 e⁻ × gain (10) = 49 mV.

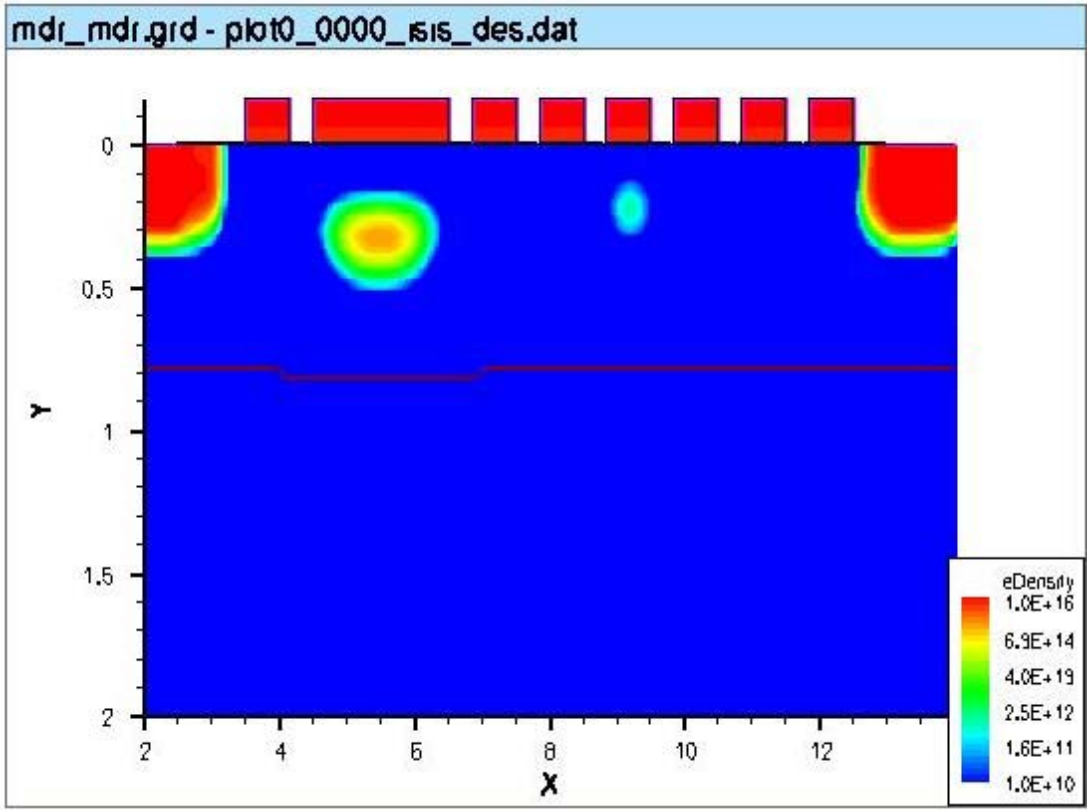


Future ISIS developments

- Next generation of ISIS will be CMOS based.
- Targeting 0.25 μm (or 0.18 μm) process.
- Possible to use 6.5 nm SiO_2 for both CCD and transistor gate dielectric?
- Maximum voltage 3.3 V.
- Non-overlapping poly-Si gates (0.35 μm gap using 0.25 μm design rules).
- ISE-TCAD used to investigate achievable charge transfer efficiency, including simulation of implantation procedure.

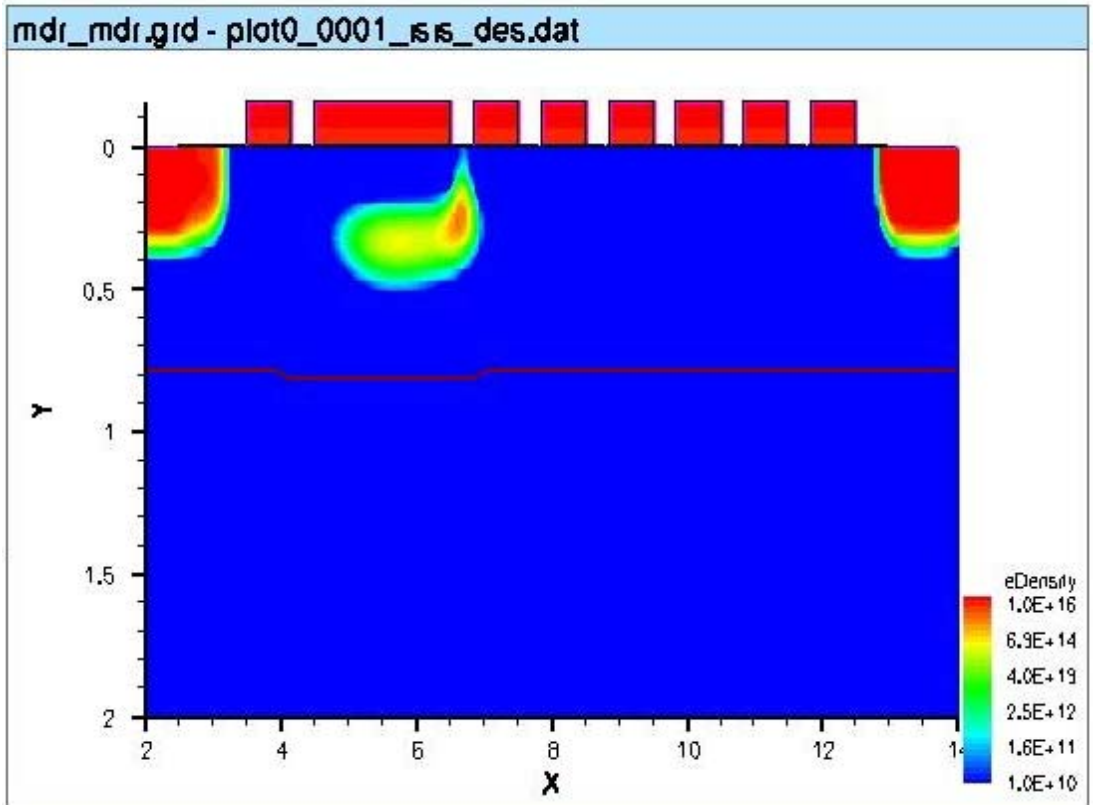
ISIS and the CMOS process

- Good charge transfer efficiency achieved in simulations.
  - Charge under photogate:



ISIS and the CMOS process

- Good charge transfer efficiency achieved in simulations.
  - Charge transferring to first storage gate:



ISIS and the CMOS process

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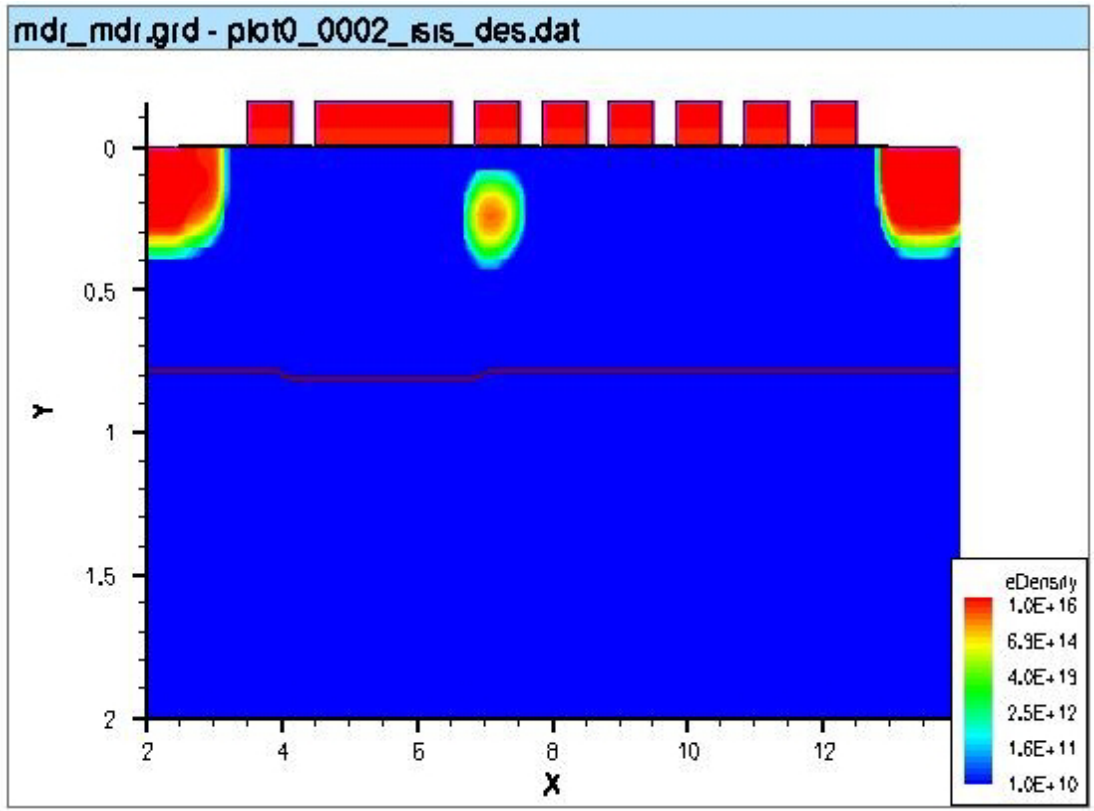
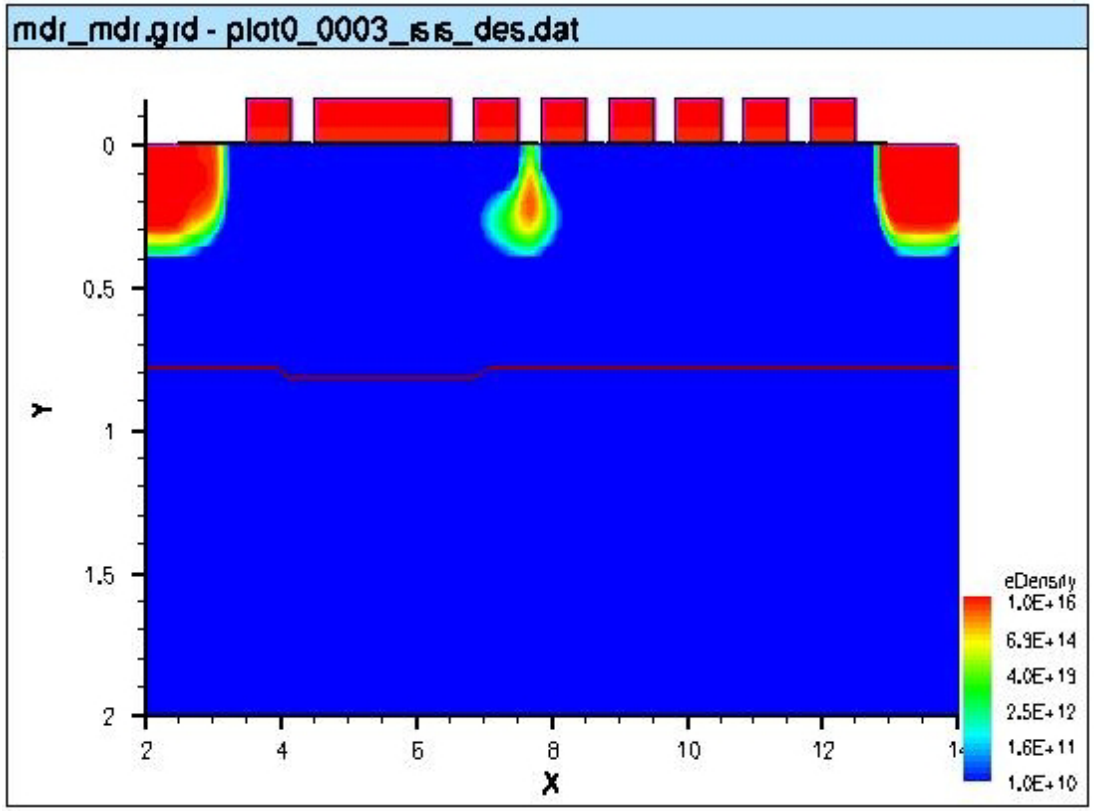


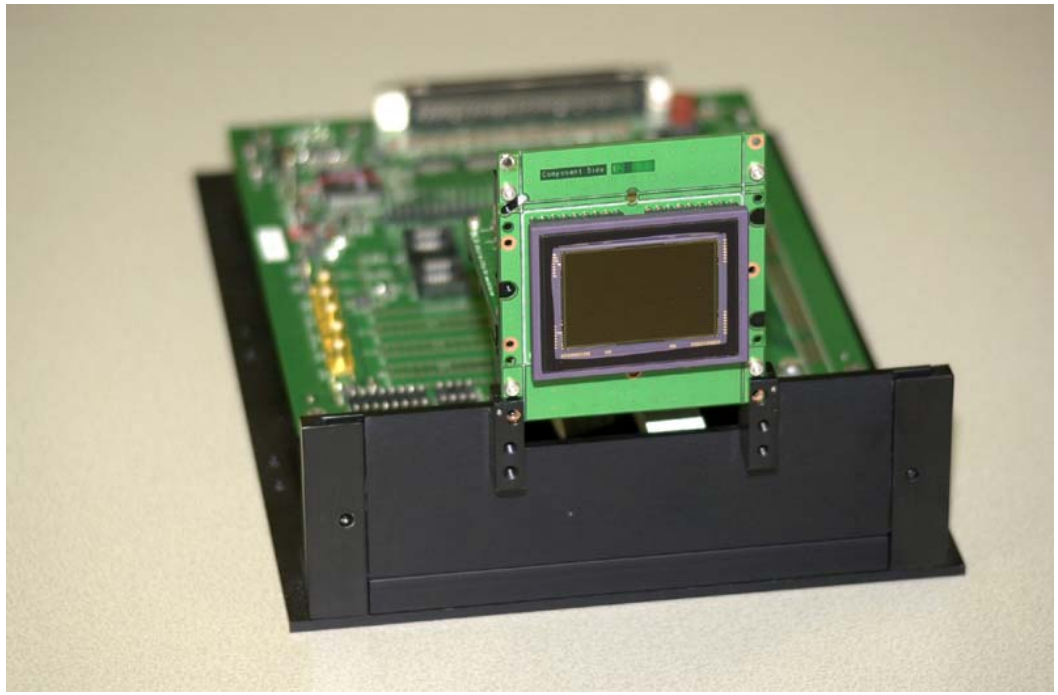
ISIS and the CMOS process

- Good charge transfer efficiency achieved in simulations.
  - Charge transferring to second storage gate:

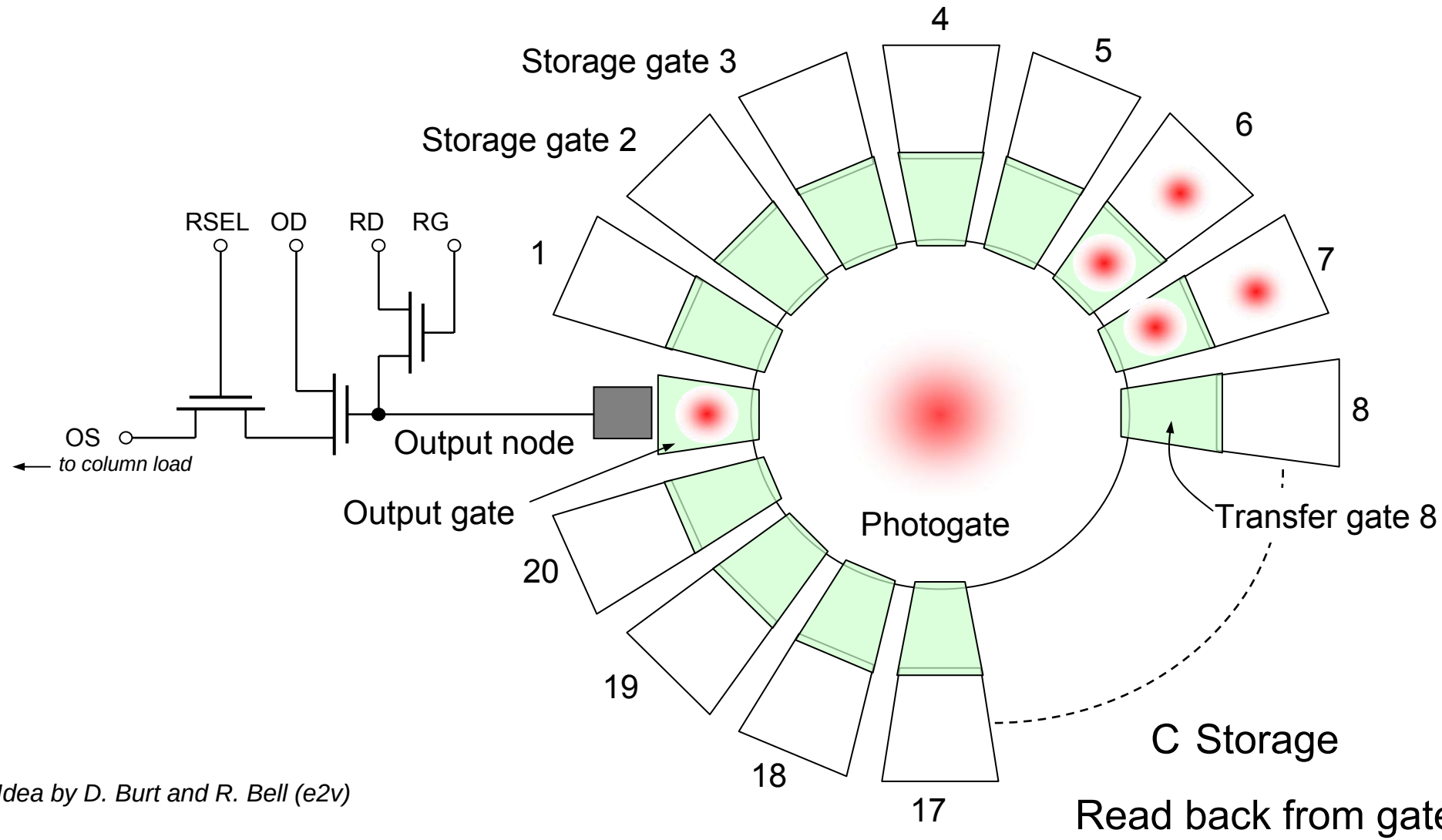


Radiation hardness of device with non-overlapping gates

- DALSA manufacture CCDs with non-overlapping gates.
- Have provided five CCDs which will allow studies of effects of electromagnetic radiation on these devices.
- Tests now starting at Rutherford.



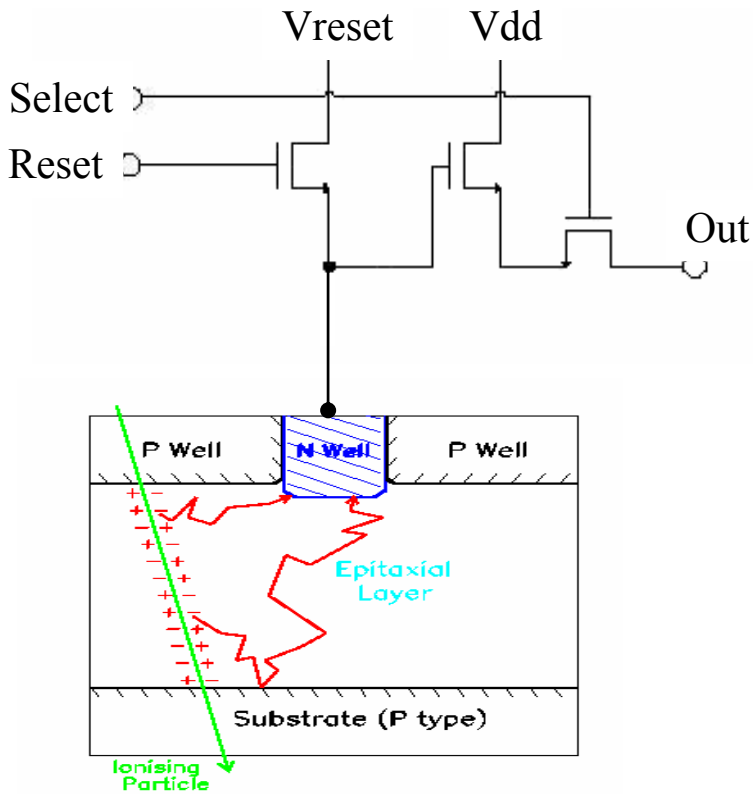
Alternative concept, the revolver



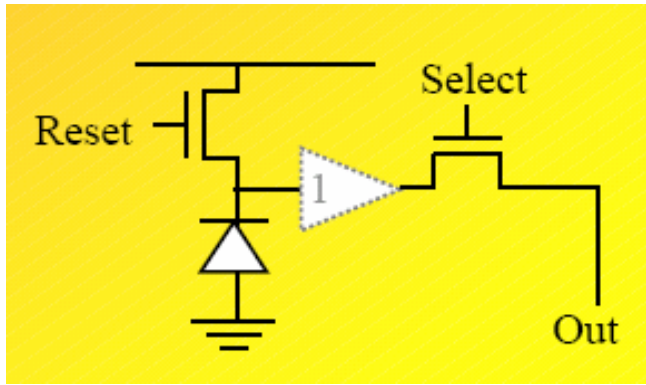
Idea by D. Burt and R. Bell (e2v)

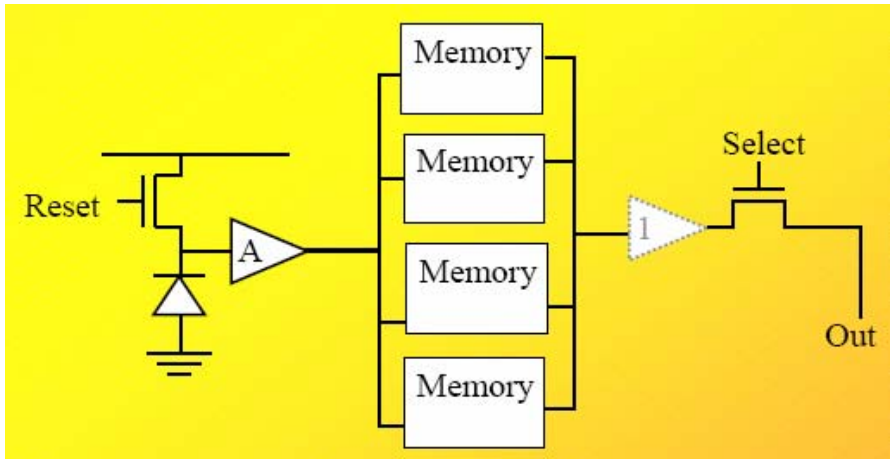
Sensors – FAPS

- Monolithic Active Pixel Sensors also under investigation for ILC.



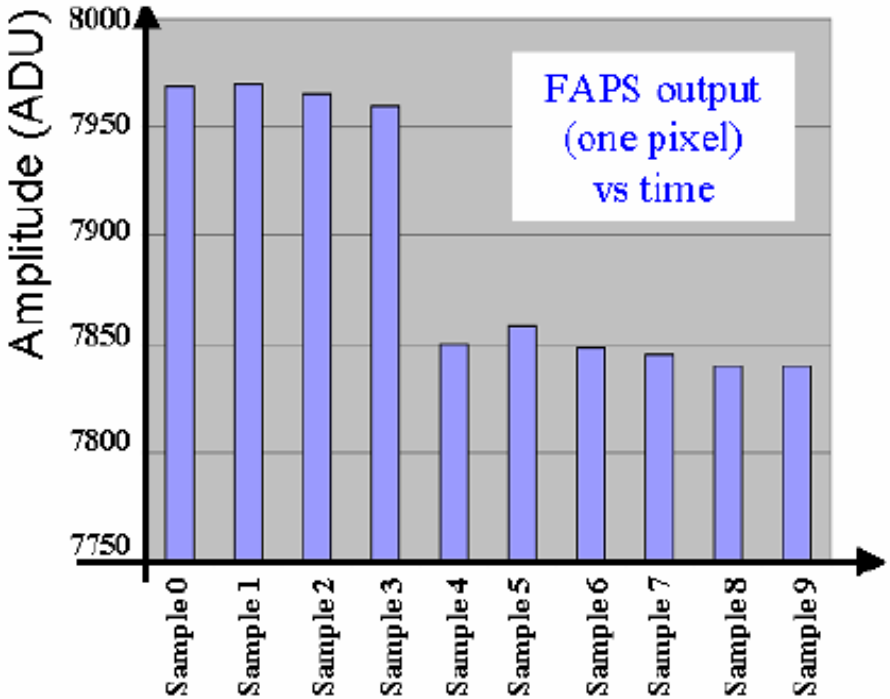
- Storage capacitors added to pixels: Flexible Active Pixel Sensors.



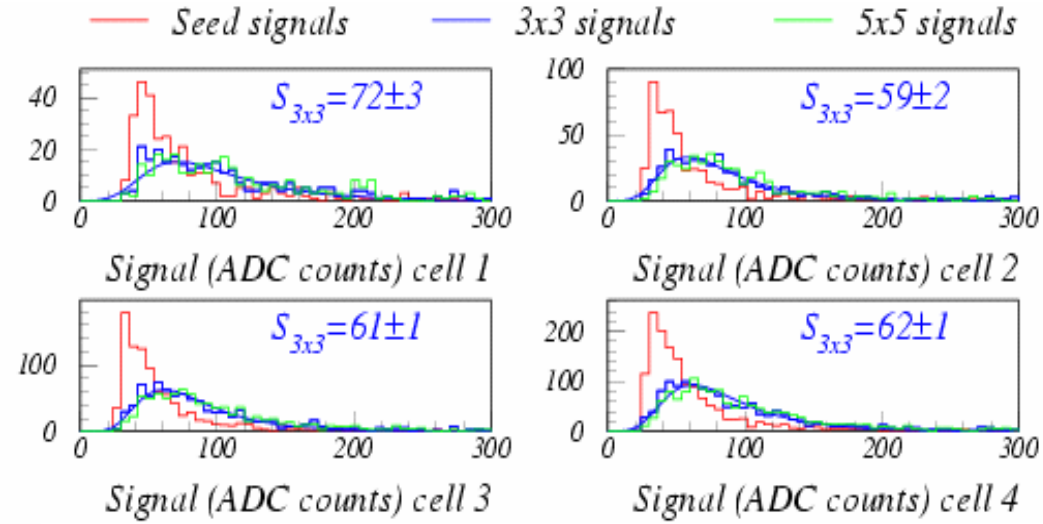


Sensors – FAPS

- Present design “proof of principle”.
- Pixels 20 x 20 μm^2, 3 metal layers, 10 storage cells.
- Test of FAPS structure with LED:



- ^{106}Ru β source tests:

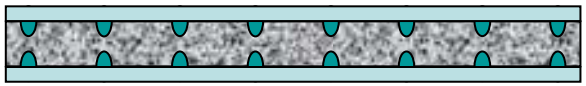


- Signal to noise ratio ~ 14.
- Ongoing development of APS for scientific applications by MI3 collaboration.

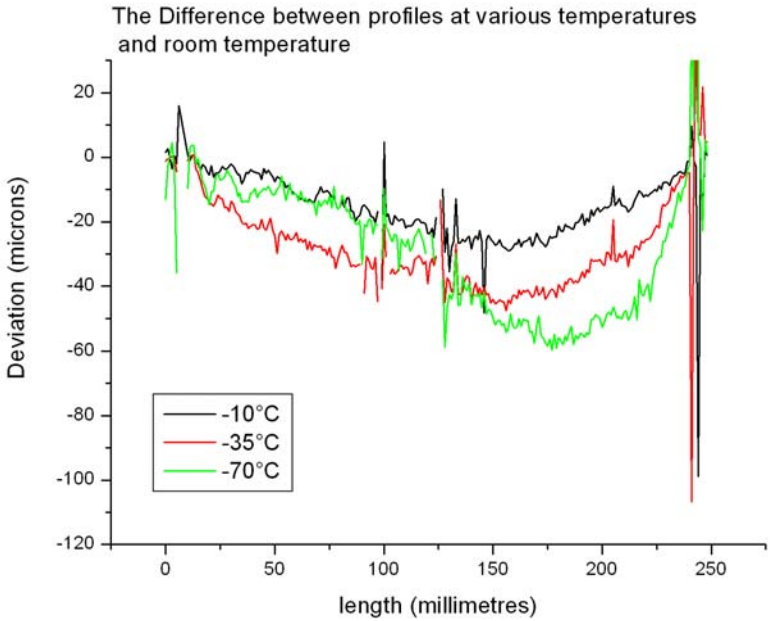
Mechanical studies

- "Stretched" sensor studies revealed thickness of ~ 50 μm Si needed.
- Beryllium results poor: bad match of thermal expansion with Si.
- Look at silicon "floating" on silicon carbide...

- ...and silicon/carbon-foam (reticulated vitreous carbon) sandwich.



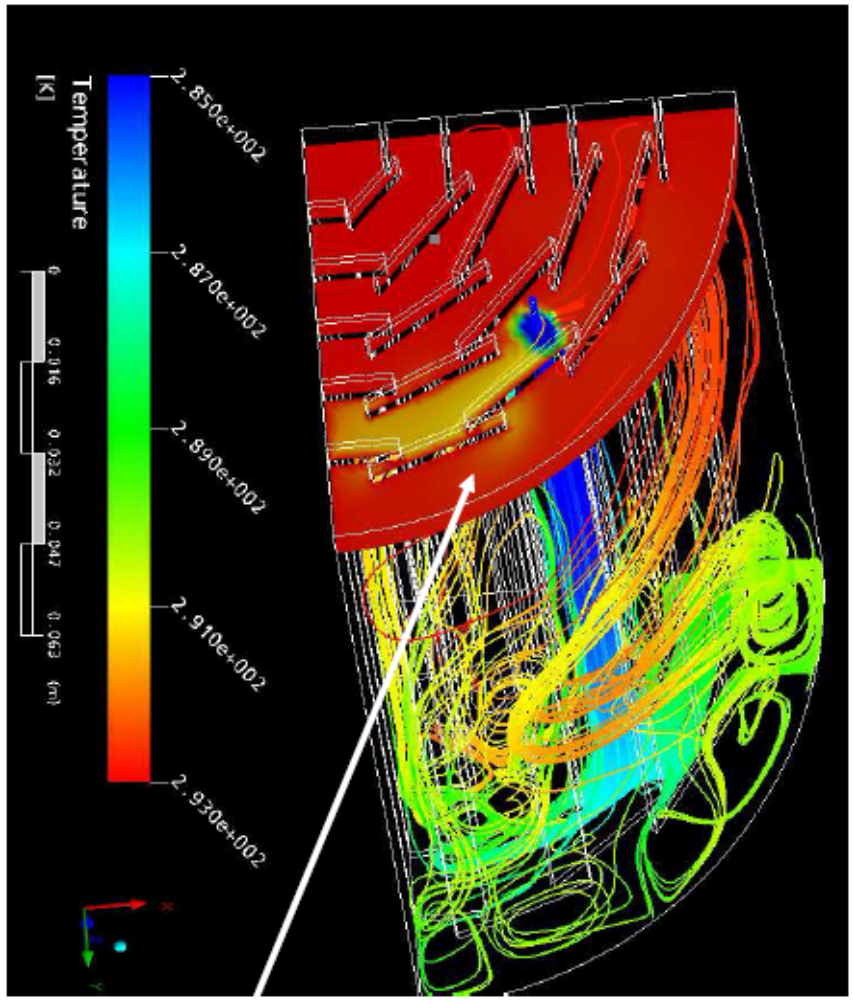
- Use "Nusil" silicone pillars to attach the silicon to the substrate.



Ladder	Material	X/Xo
Silicon on SiC foam (~ 8% density)	Silicon (25 μm), SiC foam (1.5mm); silicone adhesive (~ 300 μm in tiny pads)	0.16% (~ 0.26% at glue pad locations)
Silicon-RVC foam sandwich (~ 3% density)	Silicon (25 μm) ×2; RVC foam (1.5mm); silicone adhesive (~100 μm in tiny pads) × 2	0.08% (~ 0.14% at glue pad locations)

Thermal studies

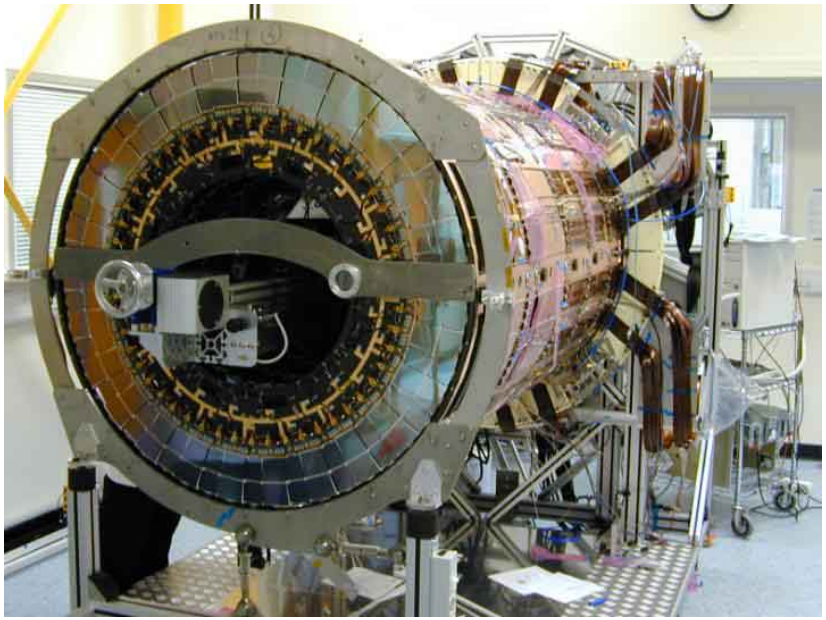
- CPCCD drive will exploit LC duty cycle of 0.5% to achieve low average power consumption: cool using N_2 gas.
- Investigations of efficacy of cooling starting using quarter vertex detector thermal test rig.
- Simulations also under development to aid design of cooling system.



Temp profile across a section close to the inlet nozzle

Other plans

- Construction of ATLAS semiconductor track detector now nearing completion (e.g. endcap will be transported from Liverpool to CERN this month.)



- UK-ATLAS institutes have submitted a "Statement-of-Interest" for contributing to design and construction of new tracker for SLHC
- Proposal in 2009, build from 2010?
- Pixels: 4.0 m^2, ~210 Mchannels
- Short strips (3 cm): 46 m^2, ~30 Mchannels
- Long strips (12cm): 108 m^2, ~11 Mchannels.
- Interest expressed by e2v.
- Small amount of funding available to develop MAPS based on SoI with Andor (Belfast).

Summary

- Studies of sensors for ILC in UK so far geared towards vertex detector (LCFI Collaboration).
- Studies of sensors, optimisation of vertex detector design for physics continuing.
- CCDs with column parallel readout look to be one sensor type which can provide the necessary performance.
- In-situ Image Storage Sensor offers high degree of immunity to possible RF pick-up problems, improved radiation hardness and relaxed readout speed requirements – first proof of principle device now tested.
- Active Pixel Sensor studies continuing mainly within MI3 framework for general science applications.
- Silicon/foam sandwich structures promise to provide very low mass support structures for silicon sensors.
- Studies of vertex detector cooling have now started.
- Increased interest in, and effort available for, μ-strip tracker studies as ATLAS build draws to a close.