Technologies offered and foundry access through EUROPRACTICE at IMEC

EUROPRACTICE
IC SERVICE

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0.35 µm

0.25 µm

0.18 µm

0.13 µm

90nm

SEEDS FOR TOMORROW'S WORLD

IMECNOLOGY

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Outline

EUROPRACTICE IC SERVICE

The Right Cocktail of ASIC Services

- Introduction of IMEC and the Europractice service
- Supported foundries and technologies
- Access to the technologies
- Getting the silicon manufactured
- Focus on the total solution
- Conclusion

EUROPRACTICE IC SERVICE

The Right Cocktail of ASIC Services

IMEC

- Founded in 1984, located in Leuven, Belgium
- Largest independent R&D institute in Europe
- Turn-over in 2004 : 159 mio €
- ~1350 people

Activities

- Advanced nanoelectronics technology development (45 nm and below)
- Microsystems, advanced packaging and interconnection technology development
- New design methodology development for ultra low-power, wireless sensor networks and Multi-Mode MultiMedia applications
- Training and industrial support (ex. EUROPRACTICE service)

Infrastructure

- 6500 m^2 200 mm cleanroom
- New 3200 m^2 300 mm cleanroom

www.imec.be

Europractice offers you ASICs for small and medium volume applications

EUROPRACTICE IC SERVICE

The Right Cocktail of ASIC Services

When you want to develop an ASIC, you need :

- Foundry design rules & documentation
- Cell libraries and design kits
- Access to flexible prototype and volumes
- Technical support
- Design support (layout)
- Support in choice of package
- Support in test development

When you contact a foundry or a library vendor, the first question to qualify you as a potential customer is :

> ➢"how many million units do you need during the next years"

If you can not commit for high volume, then the foundry is not interested

EUROPRACTICE has agreements with the foundries and library vendors to give you access and support to prototyping and small volume without volume commitment

The ONE-STOP Shop

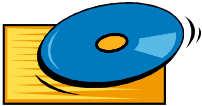
EUROPRACTICE IC SERVICE

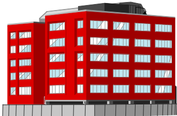
The Right Cocktail of ASIC Services

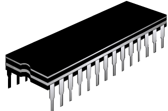
Customers

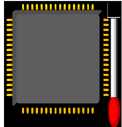
Europractice

Suppliers









Library vendors | **Foundries** | **Packaging houses** | **Test Houses**

easyCOT turnkey solution

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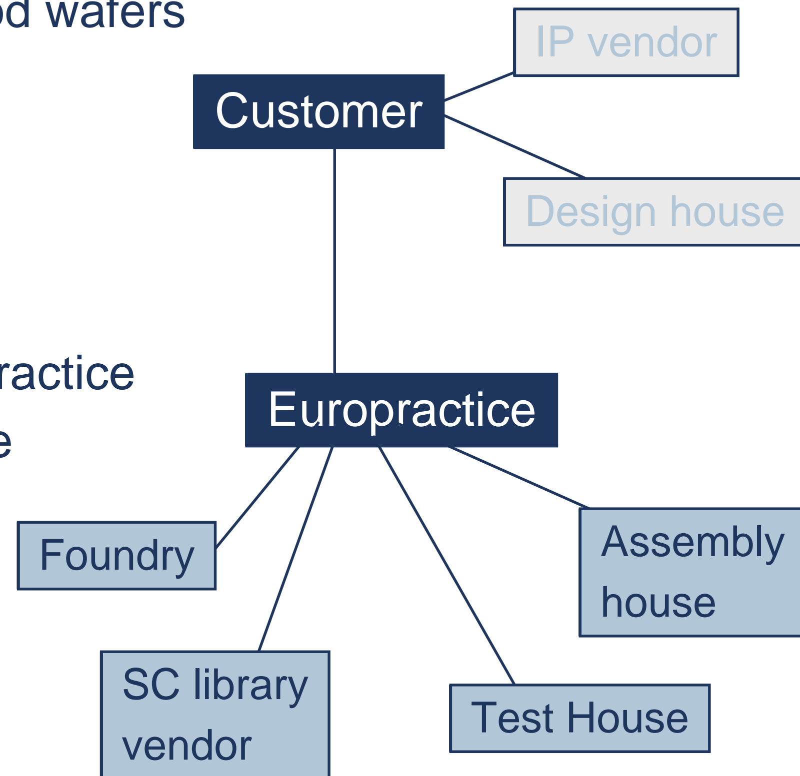
Europractice provides Turnkey Solution : Europractice is the single point of contact and/or contract

- Standard Cell Library Vendor
- Foundry - delivery of PCM-good wafers
- Assembly house
- Test house

easyCOT

- COT model but through Europractice
- Europractice provides interface
- 1 contract
- Yield risk is taken by customer



CUSTOMER = YOU takes responsibility of yield

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EUROPRACTICE
an easyCOT turnkey ASIC solution

The Right Cocktail of ASIC Services

EUROPRACTICE offers an easyCOT turnkey ASIC solution including

- easy access to foundry technology, cell libraries and support
- deep-submicron RTL-to-layout service + design support
- flexible access to silicon prototyping and production at leading foundries
- Qualification, packaging and test
- logistics (from prototypes to volume delivery)

EUROPRACTICE is not a legal entity !

EUROPRACTICE IC SERVICE

The Right Cocktail of ASIC Services

EUROPRACTICE is NOT a company

the brand name of a SERVICE

offered by IMEC

Outline

EUROPRACTICE
IC SERVICE

The Right Cocktail of ASIC Services

Introduction of IMEC and the Europractice service

Supported foundries and technologies

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Conclusion

Supported foundries and technologies

- 0.7µ CMOS A/D
- 0.5µ CMOS A/D 3M
- 0.35µ CMOS A/D 5M
- 0.7µ CMOS A/D I2T 100V
- 0.7µ CMOS A/D I2T 30V (B)
- 0.35µ CMOS A/D I3T80 80 V (B)
- 0.5µ CMOS C5 EEPROM (US)

MOSAID Virtual Silicon

Cell libraries and design kits for UMC's 0.25, 0.18 & 0.13µ CMOS technologies

- 0.25µ SiGe:C 120GHz
- 0.25µ SiGe:C 200GHz
- 0.25µ SiGe:C 30GHz, BVCEO>7V
- 0.25µ SiGe:C Ft/Fmax 190/230 GHz

austriamicrosystems

- 0.8µ CMOS A/D
- 0.8µ CMOS 50V
- 0.6µ CMOS A/D 3M
- 0.35µ CMOS A/D 4M
- 0.35µ SiGe BiCMOS 4M
- 0.35µ CMOS EEPROM
- 0.35µ CMOS 50V
- 0.35µ CMOS OPTO

UMC

- 0.25µ CMOS D
- 0.25µ CMOS MMC/RF
- 0.18µ CMOS D
- 0.18µ CMOS MMC/RF
- 0.13µ CMOS D
- 0.13µ CMOS MMC/RF
- 90nm CMOS MMC/RF

Our Foundry Partners

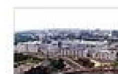
UMC Foundry and Fabs

Diversification of manufacturing bases

Fab 6A
Clean Room Level: 0.1um/Class 10
Process: 0.45um
Design Capacity: 50,000 wafers/month
Wafer Size: 6"
Location: Hsin-Chu, Taiwan

Fab 8AB
Clean Room Level: 0.1um/Class 1
Process: 0.25um
Design Capacity: 70,000 wafers/month
Wafer Size: 8"
Location: Hsin-Chu, Taiwan

Fab 8E
Clean Room Level: 0.1um/Class 1
Process: 0.18um
Design Capacity: 35,000 wafers/month
Wafer Size: 8"
Location: Hsin-Chu, Taiwan



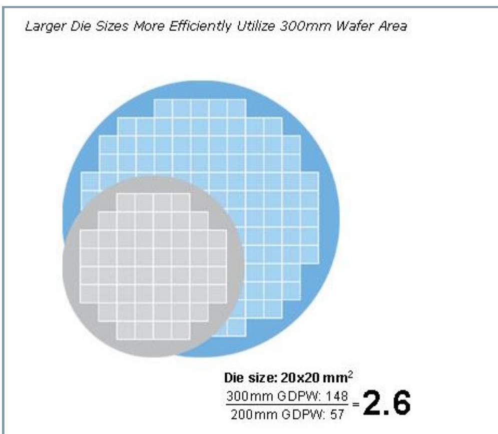
Fab 8F
Clean Room Level: 0.1um/Class 1
Process: 0.15um
Design Capacity: 40,000 wafers/month
Wafer Size: 8"
Location: Hsin-Chu, Taiwan

Fab 8C
Clean Room Level: 0.1um/Class 1
Process: 0.35um - 0.15um
Design Capacity: 35,000 wafers/month
Wafer Size: 8"
Location: Hsin-Chu, Taiwan

Fab 8D
Clean Room Level: 0.1um/Class 1
Process: 90nm
Design Capacity: 35,000 wafers/month
Wafer Size: 8"
Location: Hsin-Chu, Taiwan

Fab 12A (12-inch Fab)
Process: 65nm
Design Capacity: 40,000 wafers/month
Wafer Size: 12"
Location: Tainan, Taiwan

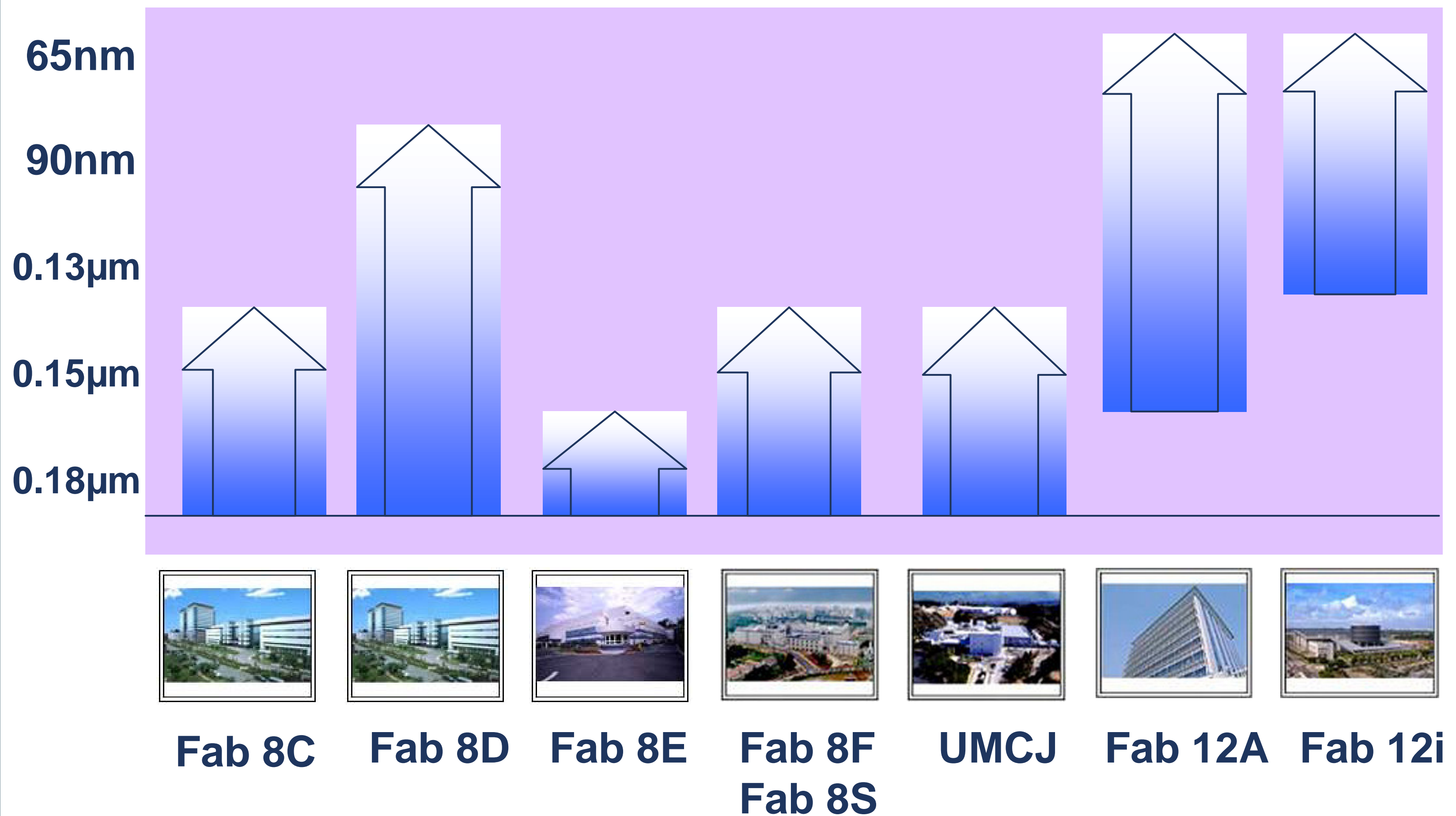
UMCJ
Process: 0.15um
Design Capacity: 32,000 wafers/month
Wafer Size: 8"
Location: Japan



Fab 12i (12-inch Fab)
Process: 90nm
Wafer Size: 12"
Location: Singapore

Fab 8S
Clean Room Level: 0.1um/Class 1
Process: 0.25-0.15um
Design Capacity: 25,000 wafers/month
Wafer Size: 8"
Location: Hsin-Chu, Taiwan

Multiple Fabs for Each Technology



Wide Range of Available Processes*

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The Right Cocktail of ASIC Services

Technology	Voltage Options			Max. Metal Layers
	Core	IO	High Voltage	
90nm Copper Logic (L90)	1.0V, 1.2V	1.8V, 2.5V, 3.3V		9Cu
90nm Copper Mixed Mode	1.0V, 1.2V	1.8V, 2.5V, 3.3V		9Cu
0.13um Copper Logic (L130)	1.2V	3.3V		8Cu
0.13um Copper Mixed-Mode/RFCMOS	1.2V	3.3V		8Cu

* This only represents a partial list of technologies available from UMC.

A glance on UMC L250 (and up) processes

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		0.25um	0.35um	0.5um
Vcc		2.5/3.3V, 2.5/5V	3.3V/5V	5V
Poly/Metal layer		1P5M	1P5M	1P3M
Substrate/Well		P-sub, Twin Well	P-sub, Twin Well	P-sub, Twin Well
Isolation		Shallow Trend Isolation	LOCOS	LOCOS
Gate Oxide		50/65/120	65/120	135
Salicide		Titanium salicide	Titanium salicide	Titanium salicide
Backend	ILD	PSG+CMP	USG/BPSG+Etch-back	USG/BPTEOS+Etch-back
	IMD	HDP+PeOX+CMP	SRO+SOG+PEOX+CMP	SRO+SOG+E.B.+PEOX
	Intercont.	W-plug/AI	W-plug/AI	W-plug/AI
Capactitance		Metal-insulator-Metal	Poly-insulator-Poly	Poly-insulator-Poly
Mass production		1998 at 8" Fab	1996 at 8" Fab	1995 at 8" Fab

UMC L180 1P6M Process, Key Features

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Regular Technology

- 1P6M Process
- Shallow Trench Isolation (STI)
- HEI Retrograde Twin Well
- Dual Gate Ox (32A/65A)
- Co-Salicide for Gate and S/D
- ILD : HDP / PEOX / CMP
- Contact : Ti/CVD-TiN/W-CMP
- IMD1~5 : HDP / PEOX / CMP
- Mvia1~Mvia5 : C-Ti / CVD-TiN / W-CMP
- M1~M6 : Ti / TiN / Al-Cu / Ti / TiN

Special Feature

- Triple Well (for MM only)
- Active Low Vt/Zero Vt Devices (for MM only)
- Passive Devices (HR/ MMC*/ Varactor/ 2um Al Inductor)

** Metal-Metal Capacitor (need extra one mask); Varactors include MIS & Junction*

Multiple special devices in the MM/RF flavour

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Device Characteristics		Regular Vt		Low Vt		Zero Vt		Twell		Unit
		Core 10/0.18um	IO 10/0.34um	Core 10/0.24um	IO 10/0.5um	Core 10/0.3um	IO 10/0.5um	Core 10/0.18um	IO 10/0.34um	
NMOS	Vton	0.51	0.65	0.22	0.31	-0.02	0.02	0.51	0.65	Volts
	Idsn	625	590	720	640	770	750	625	590	uA/um
	Ioff	7.59p	1p	29.4n	0.92n	---	---	7.59p	1p	A/um
	Isub	20	700	---	---			20	700	nA/um
	BVDN	4	9	3.7	10.7			4	9	Volts
PMOS	Vtop	0.5	0.7	0.22	0.42	---	---	---	---	Volts
	Idsp	244.2	260	270	250					uA/um
	Ioff	8.07p	0.5p	12.4n	0.002n					A/um
	Isub	0.16	30	---	---					nA/um
	BVDP	5.2	6.5	5.2	7.2					Volts
P-Well/N-Well T-Well/N-Well	Tdelay	28.5	55	---	---	---	---	28.5	55	psec /stage

GOX_1.8V: 33A(physical), 42A(electrical); GOX_3.3V: 65A(physical), 70A(electrical).

L180 RF Device Characteristics

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Type		RF Characteristic	Value
Core	NMOS	Ft_max @Vd=1.8V for 0.18umx5umx21	49 GHz
		Fmax_max @Vd=1.8V for 0.18umx5umx21	34 GHz
		NFmin @Vg=Vd=1.8V for 0.18um x 5um x 21	0.35 dB (Ga=22dB) @2.4GHz
	PMOS	Ft_max @VD=1.8V for 0.18umx5umx21	28 GHz
I/O	NMOS	Ft_max @VD=3.3V for 0.34umx5umx21	27 GHz
	PMOS	Ft_max @VD=3.3V for 0.34umx5umx21	16 GHz
MIM Capacitor		Capacitance/Area	1 fF/um^2
		Q for Area= 50umx50umx1	170 @2.4GHz
Varactor		MIS structure	N+/Nwell
		Tunning ratio: Cmax/Cmin (VGB= -0.75V~0.75V); 5umx1umx7	2.8 (3.3pF/1.17pF) @2.4GHz
		Q (VGB=-0.75V~ 0.75V)	30 @2.4GHz
		Junction structure	P+/Nwell
		Tunning ratio: Cmax/Cmin (VP=-3.0V~0V; VN=0V); 5umx2umx60	2.6 (1.23p/0.47p) @2.4GHz
		Q (VP=-3.0V; VN=0.0V)	45 @2.4GHz
Inductor		Top Metal Thickness	2um Al
		Q @2.4GHz for L=2.6nH	9

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UMC L130E FSG 1P8M Process

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LOGIC/MIXED MODE

KEY devices

- 1.2V HS N/P (1)
- 1.2V LL N/P (1)
- 1.2V SP N/P (1)
- 3.3V N/P
- 1.2V HS Native Vt NMOS (PSUB)
- 3.3V Native Vt NMOS (PSUB)
- 2.5V IO N/P (2)
- MMC
- HR

(1) Maximum two of tree to be combined
(2) 2.5V cannot be combined with 3.3V

MIXED MODE/RFCMOS

KEY devices

- 1.2V HS N/P (1)
- 1.2V LL N/P (1)
- 1.2V SP N/P (1)
- 3.3V HIGH GAIN N/P
- 1.2V HS Low Vt N/P
- 3.3V High Gain Low Vt
- 1.2V HS Native Vt NMOS (PSUB)
- 3.3V Native Vt NMOS (PSUB)
- MMC
- HR

(1) Maximum two of tree to be combined

Different core devices available

	HS device	LL device	SP device
VCC	1.2V	1.2V	1.2V
Tox	22A	22A	22A
Ioff (N/P)	4/-4 nA/um	4/-6 pA/um	0.2/0.2 nA/um
Stage Delay	14ps	33ps	19.6ps
Vton (N/P)	0.38V/-0.33V	0.58V/-0.52V	0.47V/-0.42V

Diversification for IO devices

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M130E I/O vs L130E I/O

Device	NFET		PFET	
Parameter	M130E HG IO	L130E HS IO	M130E HG IO	L130E HS IO
Vt_Gm (V)	0.55	0.642	0.547	0.576
Vsat (V)	0.505	0.540	0.528	0.552
Idsat (uA/um)	590	590	270	270
Ioff (pA/um)	4.0	1.0	1.0	1.0
DIBL	22	39	15	16
GM	6.17E-04	6.65E-04	1.48E-04	1.48E-04
Rout	1.20E+05	5.18E+04	7.07E+04	5.86E+05
GM*Rout	73.7	34.4	104.5	86.4

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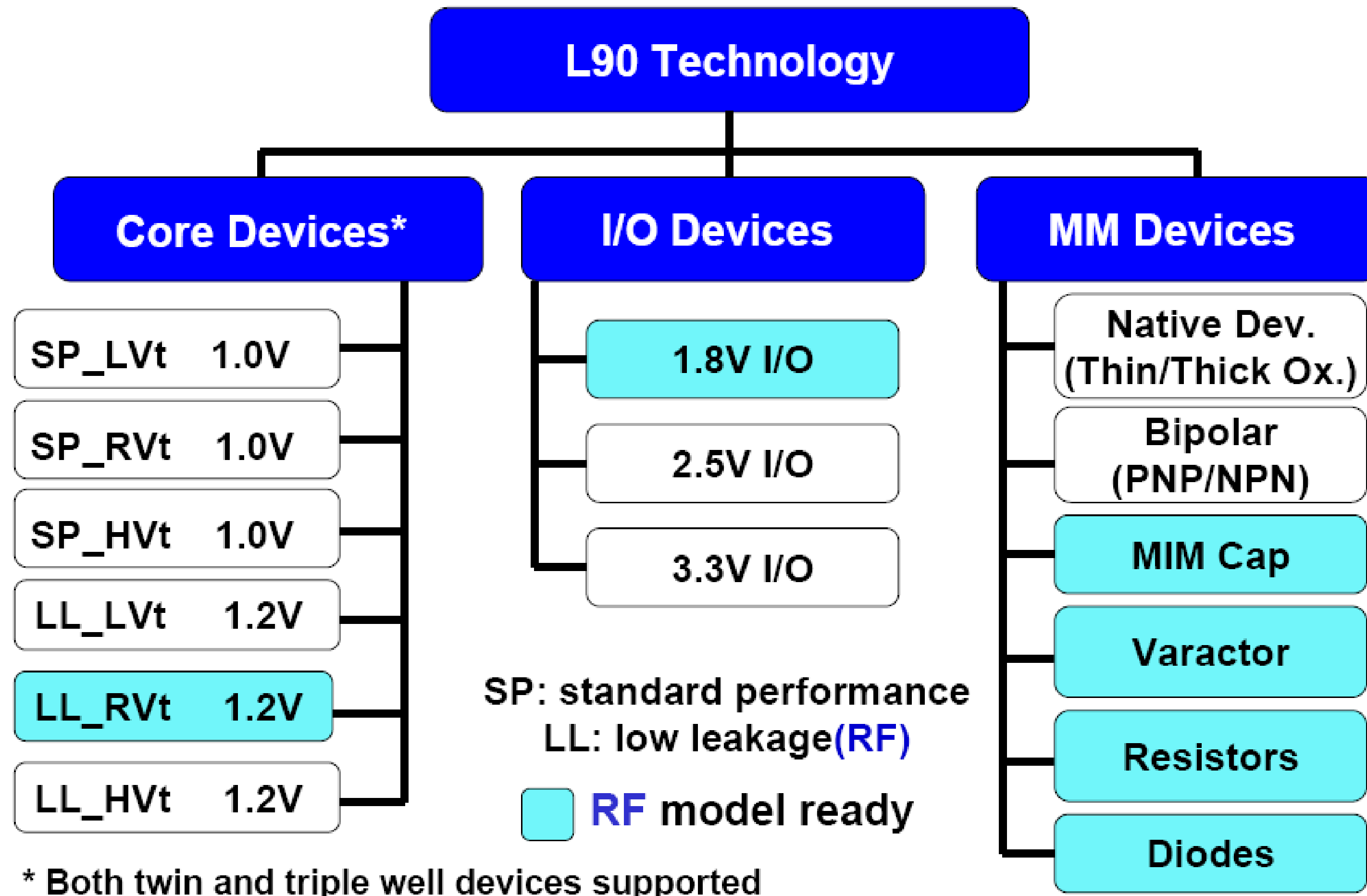
130nm RF Performance Summary

Type		RF Characteristic	Value
Core	NMOS	Ft @Vd=1.2V	110 GHz
		Fmax @Vd=1.2V	90 GHz
		NFmin @Vg=Vd=1.2V	0.53dB @5.8GHz
	PMOS	Ft @Vd=1.2V	54 GHz
I/O	NMOS	Ft @Vd=3.3V	26 GHz
	PMOS	Ft @Vd=3.3V	17 GHz
MIM Capacitor		Capacitance/Area	1 fF/um^2
		Q@5.8GHz	50
MOM Capacitor		Capacitance/Area	1.78 fF/um^2 (M1-M6)
		Q@5.8GHz	> 50
N+/Nwell MIS Varactor (W/L/Nf/M)		Tuning ratio: Cmax/Cmin (VGB=-1.0V~1.0V)	8.3 @5.8GHz
		Q	>10
P+/Nwell Junction Varactor (W/L/Nf/M)		Tuning ratio: Cmax/Cmin (VD=0V~1.2V)	1.1 @5.8GHz
		Q	50
Inductor (Do/Nt/W/S)		Top Metal Thickness	2um Cu
		Q for L=2.5nH	13 @5.8GHz

UMC L90N lowK 1P9M Process



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L90N (SP and LL) Logic/MM Core Devices

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Device Type	SP_HVt	SP_RVt	SP_LVt	LL_HVt	LL_RVt	LL_LVt
Vcc (V)	1.0	1.0	1.0	1.2	1.2	1.2
Tox (A)	16	16	16	22	22	22
Lg_Si (um)	0.07	0.07	0.07	0.08	0.08	0.08
Vt_sat N/P (V)	0.38/0.31	0.24/0.2	0.17/0.14	0.57/0.465	0.48/0.44	0.4/0.315
Idsat N/P (uA/um)	460/190	655/280	760/330	355/155	450/170	540/230
Ioff (A/um)	300p	5n/10n	50n/100n	4p/10p	30p	400p
Delay (ps/stage)	18.5	11.5	9.8	25.5	20.5	15.5
I/O device options	I/O option of 3.3V, 2.5V or 1.8V					

Note: Both dual and triple oxide (SP+LL) devices offered

L90N Logic/MM I/O Devices

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Device Type	1.8V	2.5V	3.3V
Vcc (V)	1.8	2.5	3.3
Tox (A)	31	52	65
Lg_Si (μm)	0.16	0.23	0.36
Vt_sat (V) N/P	0.47/0.38	0.44/0.40	0.50/0.50
Idsat (μA/μm) N/P	600/255	600/275	590/260
Ioff (A/μm) N/P	10p/20 p	15p/15p	10p/10p
Gate Delay (ps/stage)	26	30	43
Gm*Rout	32/39	27/37	62/70
Matching Report	Available	Available	Available

Note: Single I/O option of 3.3V, 2.5V, or 1.8V

L90N Logic/MM BEOL Scheme

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Layer	Dimension	Pitch	Material	Thickness (A)	Resistance
M1	0.12um	0.24um	Low-*k* | FSG	2.2K	115 mohm/sq
M2-M6 (1X)	0.14um	0.28um	Low-*k* | FSG	2.5K	105mohm/sq
M7-M8 (2X)	0.28um	0.56um	FSG	5K	42 mohm/sq
M9 (4X)	0.56um	1.12um	FSG	8.1K	27 mohm/sq
V1-V5	0.14um	0.32um	Low-*k* | FSG	3.2K	1.85 ohm/via
V6-V7	0.28um	0.56um	FSG	4K	0.6 ohm/via
V8	0.56um	1.12um	FSG	9.4K	0.2 ohm/via

* At least one FSG layer at the top; up to 6 low-k layers.

L90N RF Performance

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Type		RF Characteristic	Value
Core	NMOS*	Ft @Vd=1.2V; 0.09umx2umx16x2	124 GHz
		Fmax@Vd=1.2V; 0.09umx2umx16x2	106 GHz
		NFmin @Vg=Vd=1.2V; 0.09umx2umx16x2	0.3 dB/0.53 dB @2.4GHz/5.8GHz
	PMOS	Ft@Vd= -1.2V; 0.09umx4umx16x2	58 GHz
I/O	NMOS*	Ft@Vd=1.8V; 0.18umx4umx16x1	66 GHz
	PMOS	Ft@Vd= -1.8V; 0.18umx4umx16x2	27 GHz
MIM Capacitor		Capacitance/Area	1.5 fF/um^2
		Q for Area= 5umx5umx1	86 @5.8GHz
N+/Nwell MIS Varactor (W/L/Nf/M)		MIS structure (5um/0.5um/4/4)	1.2V N+/Nwell
		Tuning ratio: Cmax/Cmin (VGB=-1.2V~1.2V)	6.47 @5.8GHz
		Q @VGB=0V	8.68 @5.8GHz
P+/Nwell Junction Varactor (W/L/Nf/M)		Junction varactor structure (5um/0.5um/8/8)	1.2V P+/Nwell
		Tuning ratio: Cmax/Cmin (VD=0V~3V)	1.31 @5.8GHz
		Q @VD=0V	14.1 @5.8GHz
Inductor (Do/Nt/W/S)		Top Metal Thickness (150um/3.5/6um/2um)	3um Cu
		Q for L=2.2nH	14 @5.8GHz

*: Twin & Triple-well device

All Europractice supported technologies provide an FDK

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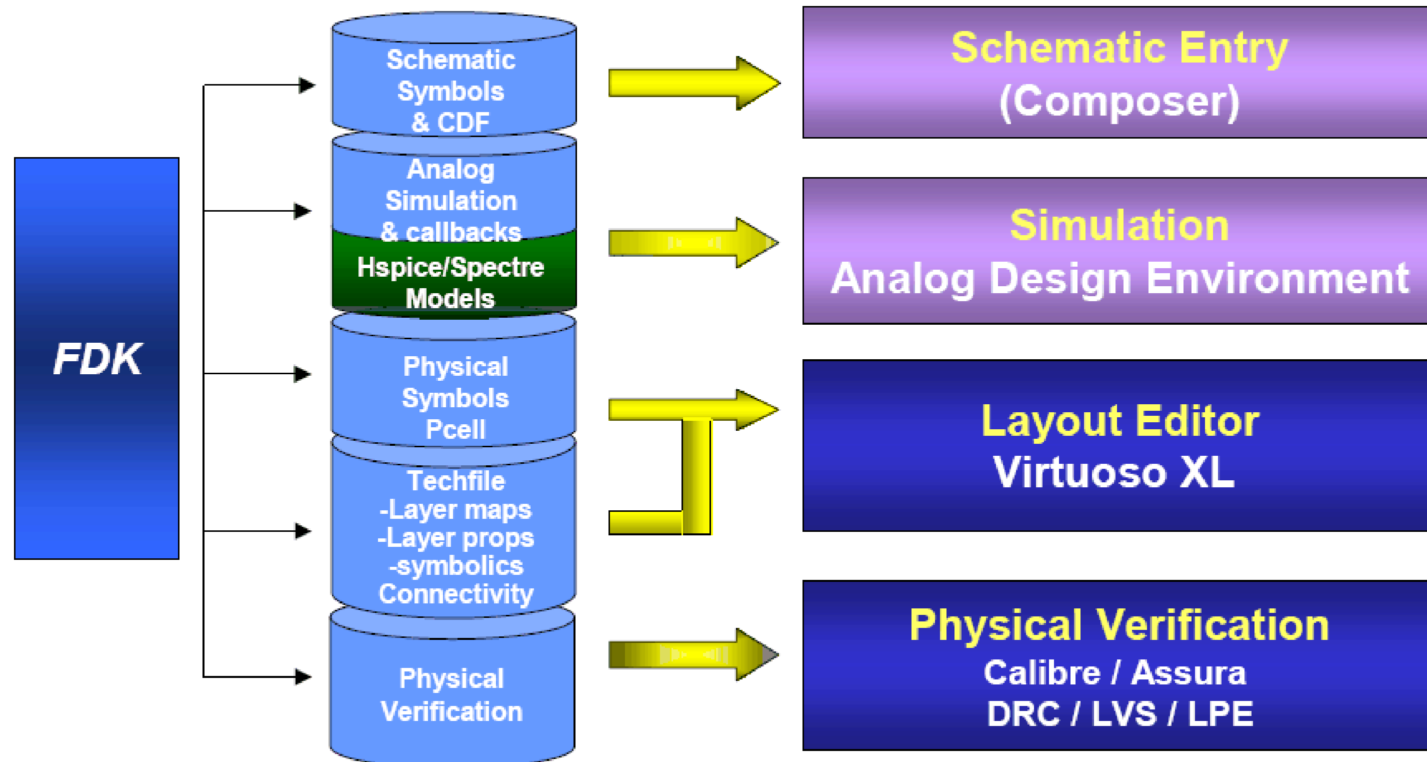

Our Foundry Partners

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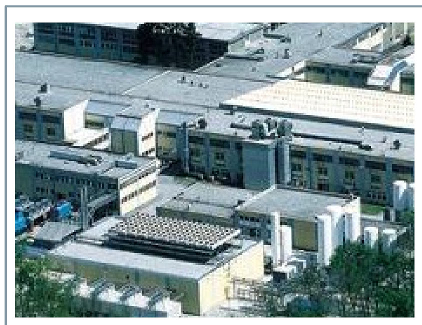
AMS Foundry

State of the art wafer Fab B (8 inch)

- Installed capacity of 5,200 WSPM (1) out of potential maximum of 8,600 WSPM (1
- 0.35 µm TSMC base process



Wafer Fab A (4 inch) and mask lithography

- Installed capacity of 9,200 WSPM (1) (4 inch wafers)

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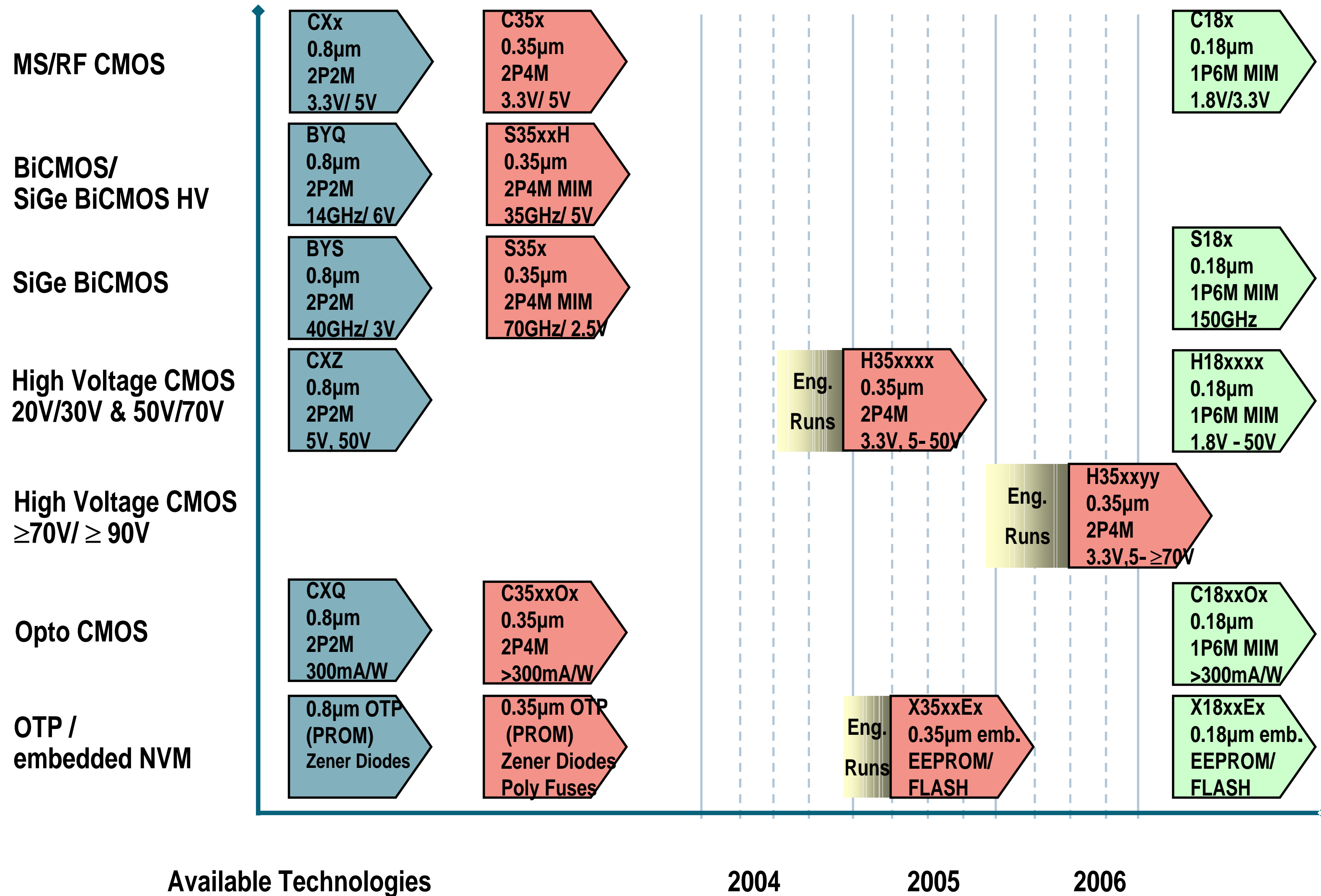
AMS Technology roadmap



SiGe BiCMOS 0.35um

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Process Name	units	S35D3H1	S35D4H2	S35D4H5	S35D3M2	S35D4M2	S35D4M5
Process Type		HV-SiGe BiCMOS			SiGe-BiCMOS		
Drawn MOS Channel Length,	µm	0.35			0.35		
Drawn Emitter Width	µm	0.4			0.4		
Operating Voltage CMOS	V V	3.3/5	3.3	3.3/5	3.3	3.3	3.3/5
Number of Metal Layers		3	4	4	3	4	4
Number of Poly Layers		4	4	4	4	4	4
Substrate Type		p			p		
Diffusion Pitch	µm	0.9			0.9		
Metal1/2/3 Pitch	µm	0.95/1.1/1.2			0.95/1.1/1.2		
Poly1 Pitch	µm	0.8			0.8		
Thick Metal 4 pitch	µm	-	4.5	4.5	-	4.5	4.5
High Resistive Poly	kOhm/#	-	-	1.2	-	-	1.2
Poly1 / Poly2 Precision Caps	fF/µm²	0.9	0.9	0.9	0.9	0.9	0.9
Metal 2 / Metal 3 Precision Caps	fF/µm²	-	1.25	1.25	1.25	1.25	1.25
N/PMOS Active Channel Length	µm	0.30/0.30			0.30/0.30		
N/PMOS Saturation Current	µA/µm	540/240			540/240		
Gain	-	160			160		
Early Voltage VAF	V	100			100		
HS-HBT: BVceo	V	-	-	-	2.7	2.7	2.7
ft / fmax	GHz	-	-	-	60 / 70	60 / 70	60 / 70
HV-HBT: BVceo	V	5.5	5.5	5.5	-	-	5.5
ft / fmax	GHz	35 / 50	35 / 50	35 / 50	-	-	35 / 50

Design Environment: HIT-Kit

EUROPRACTICE IC SERVICE

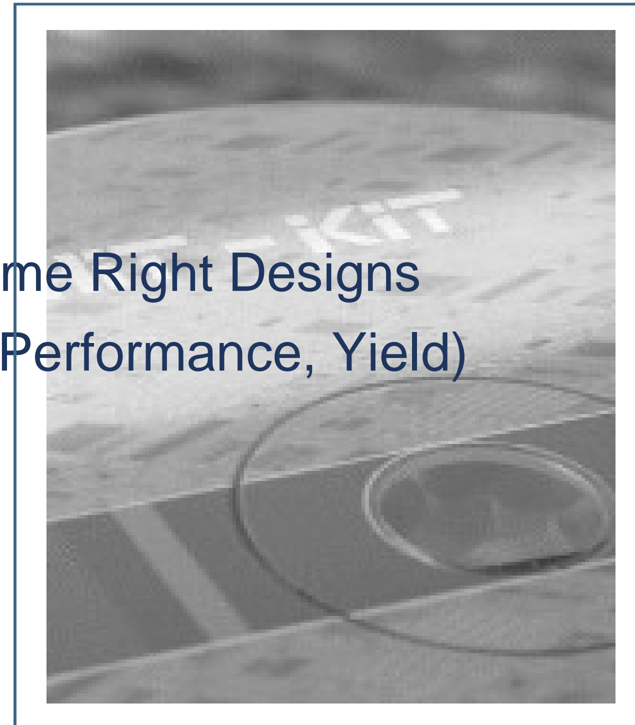
The Right Cocktail of ASIC Services

Analog/**M**ixed **S**ignal **H**igh Performance **I**nterface **T**ool **Kit**

The AMS HIT-Kit enables product developers to concentrate on their core competence **IC design** rather than on setting up and mastering the EDA environment

This leads the partner to

- ✓ Shorter Time to Market
- ✓ Complete Environment for First Time Right Designs
- ✓ More Efficient Designs (Die Size, Performance, Yield)



Our Foundry Partners

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The Right Cocktail of ASIC Services

Focus on SiGe:C
Technology Performance Parameters

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Technologies

SG25H1	Technology with highest speed HBT devices, replacement for SGC25C which features additional HBTs with fmax up to 220 GHz, Schottky diodes, RF-CMOS and an improved Design Kit
SG25H2	Unique complementary technology with high speed npn HBT devices **fmax/fT/BVCE0 = 170/170/1.9** and world record pnp HBT devices **fmax/fT/BVCE0 = 120/85/2.5**
SG25H3	High performance technology with high speed and high breakdown devices. This is an replacement for SGC25B and features additional HBTs with **BVCE0** up to 7V, Schottky diodes, RF-CMOS and an improved Design Kit.
SGB25VD	High speed HBTs are combined with complementary RF high-voltage LDMOS

Devices	Performance	Technologies			
		SG25H1	SG25H2	SG25H3	SGB25VD
HBT	$f_{max}/f_T/BV_{CE0}$ (GHz/GHz/V)	190 / 190 / 1.9(npn) 220 / 190 / 1.9(pnp)	170 / 170 / 1.9(npn) 120 / 85 / 2.5(pnp)	140/ 120 / 2.3(npn) 180 / 110 / 2(npn) 140 / 45 / 5(npn) 80 / 25 / 7(npn)	95 / 75 / 2.4 90 / 45 / 4.0 70 / 25 / 7.0
n-LDMOS	$f_{max}/f_T/BV_{CE0}$ (GHz/GHz/V)				43 / 18 / 26.0 53 / 23 / 16.0 48 / 23 / 11.5
p-LDMOS	$f_{max}/f_T/BV_{CE0}$ (GHz/GHz/V)				21 / 8 / -11.0 22 / 11 / -13.5

Outline

EUROPRACTICE
IC SERVICE

The Right Cocktail of ASIC Services

- Introduction of IMEC and the Europractice service
- Supported foundries and technologies
- Access to the technologies
- Getting the silicon manufactured
- Focus on the total solution
- Conclusion

Easy access to technology manuals, qualified cell libraries and design kits

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The Right Cocktail of ASIC Services

Sign NDA or DKLA with Europractice and get access and support to:

- Foundry technology documentation : design rules, model parameters, design manual, design rule decks …
- Libraries and design kits

Data provided though various distribution channels

- CD-ROM
  - ➢data encrypted per technology = per NDA or DKLA
- Secure FTP
  - ➢Channeled through www.europractice-online.be
- www.europractice-online.be
  - ➢Dynamic system offering FAQ, news, mailinglists …

Technical support

Knowledge platform following the updates of the technologies

EUROPRACTICE IC SERVICE

The Right Cocktail of ASIC Services

the IMEC-MTC square 3.7

WHAT'S NEW | MY SQUARE | Europractice : UMC : UMC-Closed

DOMAINS | SEARCH | Info | FAQ (24) | News (1) | Mailing list (270) | Document (1) | Calendar (0)

8 Users online

- MTC-online
- CARBonCHIP
- Europractice
  - AMIS
  - austriamicrosystems
  - UMC
    - UMC-Closed
      - L90
      - L130
      - L180
      - L250
      - CIS18
      - CIS25
      - CIS35
  - VST
  - Small volume
  - Packaging
  - Promotion & Material
  - IHP
- Flemish-Communities
- MultiMedia
- NanoCMOS-moreMoore
- Nano-RF
- For-students
- E-Learning

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Large variety of offered technologies

MPW service in more than 20 technologies

More than 150 MPW runs scheduled in 2005

Yearly about 400…450 designs prototyped on MPW runs

Wide spectrum of technologies

- AMIS, austriamicrosystems, IHP, UMC
- CMOS : 0.8µ … 90nm (analog + digital)
- High speed : 0.8µ BiCMOS ... 0.25µ SiGe BiCMOS
- High voltage : 0.8 & 0.7µ + 0.35µ CMOS

Europractice offers Prototyping …

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Through Multi Project Wafer runs (MPW, Shuttle, …)

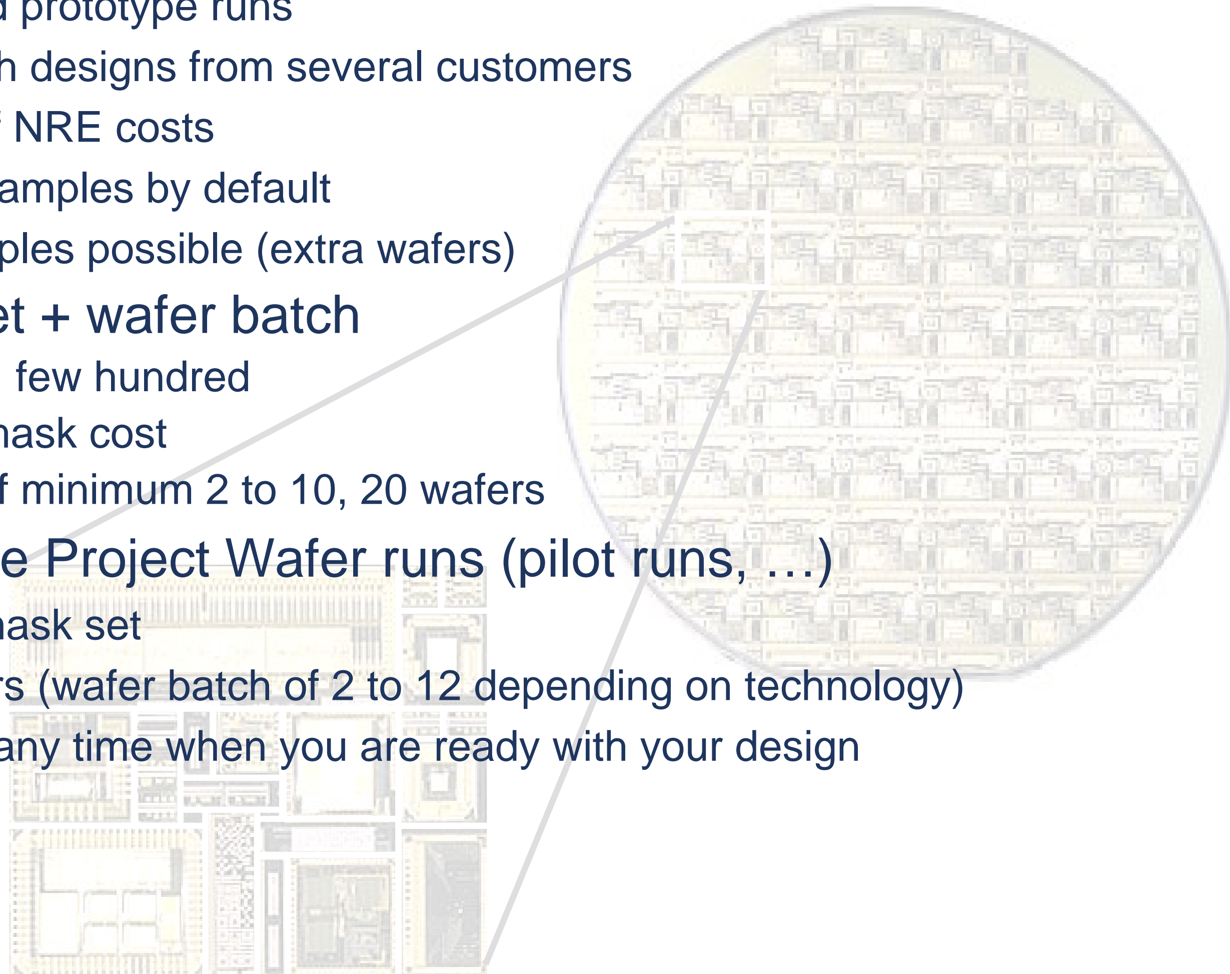
- Scheduled prototype runs
- Masks with designs from several customers
- Sharing of NRE costs
- 20 or 50 samples by default
- More samples possible (extra wafers)

MPW mask set + wafer batch

- Pre-serie : few hundred
- No NRE mask cost
- Batches of minimum 2 to 10, 20 wafers

Through Single Project Wafer runs (pilot runs, …)

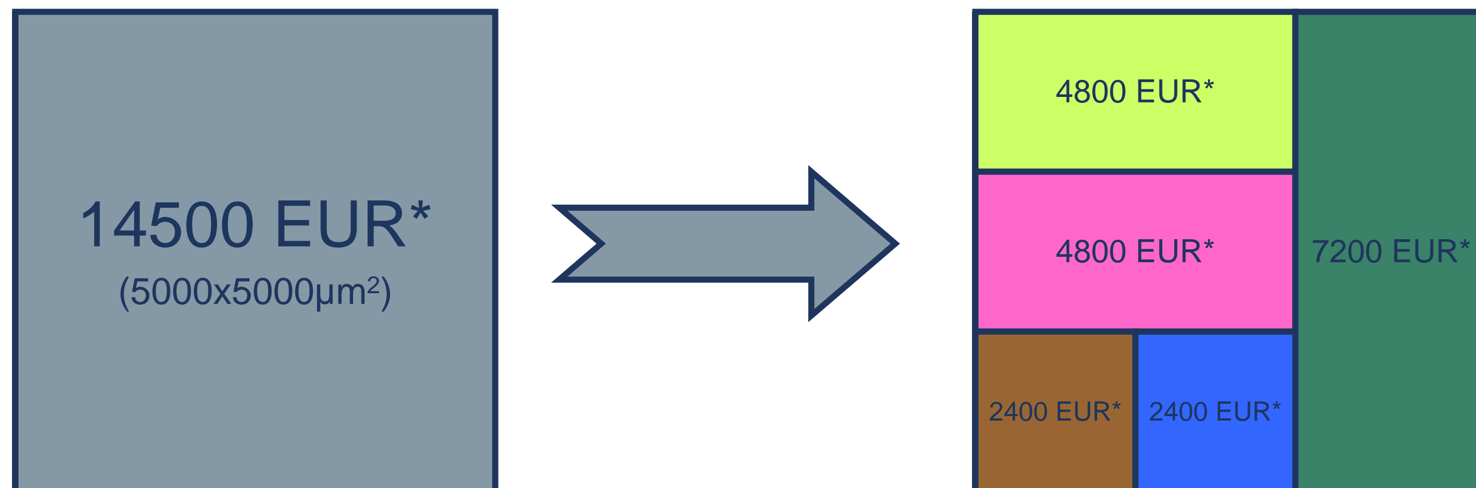
- With full mask set
- Few wafers (wafer batch of 2 to 12 depending on technology)
- Can start any time when you are ready with your design



Mini@sic: reducing the minimum area*

Design area to be used in blocks of ~1500x1500 um*

- Strongly reduced cost
- Multiple combinations possible
- Available for 0.18um and 0.13um
- Organized 3 times per year



(*) example for 0.18um 1P6M MM/RF, from European Academic or Research institute

The Right Cocktail of ASIC Services

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… and small volume ASIC production

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What is small volume ?

- That volume the foundry is not willing to give you directly
- can be foundry dependent
- can be anything volume up to 1000 wafers/year for some foundries

But small volume for foundry = big volume for you

- UMC agreement says that UMC sends all customers to Europractice with volume < 1000 wafers/year
- Austriamicrosystems sends customers with < 100 wafers/year

Small volume ASIC production possible through EUROPRACTICE and network of subcontractors

- Wafer fabrication at foundries
- Packaging at assembly houses
- Testing at test houses
- EUROPRACTICE takes care about logistics and delivers components to end-customer

What if volume goes higher ?

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The Right Cocktail of ASIC Services

Close partnership with foundry ensures smooth transfer from Europractice to foundry

- In many cases Europractice's subcontractors for packaging and test are also qualified by foundry
- Foundry is aware of running projects and future needs by regular forecast reporting by Europractice to foundry about ongoing projects

Discussion together with you and foundry to select the most appropriate option

- Europractice continues and buys larger wafer volumes, uses existing packaging and test solution
- Foundry takes over and uses existing packaging and test solution
- Foundry takes over and uses own resources for test and packaging

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EUROPRACTICE
an easyCOT turnkey ASIC solution

The Right Cocktail of ASIC Services

EUROPRACTICE offers an easyCOT turnkey ASIC solution including

- easy access to foundry technology, cell libraries and support
- **deep-submicron RTL-to-layout service + design support**
- flexible access to silicon prototyping and production at leading foundries
- **Qualification, packaging and test**
- **logistics (from prototypes to volume delivery)**

Deep-submicron Place and Route

Many customers or design houses do not have layout tools for deep-submicron technologies

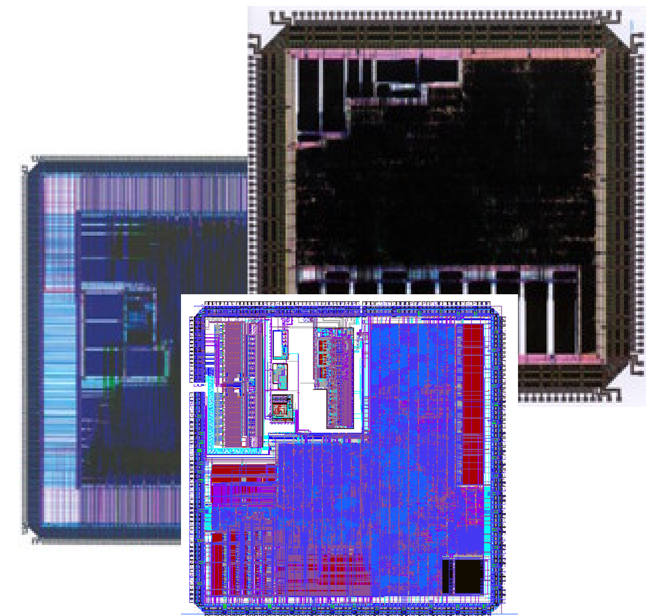
Europractice provides RTL-to-Place and Route service

- For Digital + Mixed designs
- Iterate on layout with customer for timing closure
- Full DRC, ERC and LVS check
- Tape out preparation

Since 1998, ≈15…20 tape-outs / year

- 0.5µm down to 0.13µm libraries
- up to 2.2 MGates in 0.18µm
- system clock rates up to 200MHz
- >50 different clock regions
- up to 912 staggered I/O pads
- up to 144 IP blocks in one design

Excellent first-time right record



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Assembly

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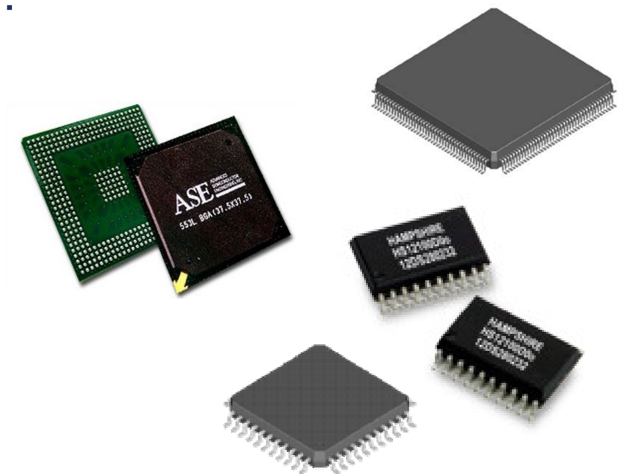
The Right Cocktail of ASIC Services

Ceramic

- subcontracted to Assembly Houses in Europe
- Main subcontractors are : Edgetek, HCM, SELMIC
- DIL, CSOIC, JLCC, CQFP, PGA, BGA

Plastic

- Mainly subcontracted to Assembly Houses in Far-East
- Main subcontractors are : ASE, ASAT, Unisem
- DIL, SOIC, PLCC, PQFP, BGA, QFN, …
- Available already for +20 samples
- Low to high volume capacity



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Test

Subcontracted to Test houses in Europe (Microtest) or Far-East (ASE)

Main subcontractors for test development are : Microtest

Test solution development

- Test program development
- Test hardware development
- Debugging

Qualification

- Life tests, burn-in
- automotive, space, MIL specs

Wafer probing

Final test

Customer Support

Product Qualification

Product can be qualified according to the specifications from the customer

- Automotive qualification
- Medical qualification
- Space qualification
- Industrial qualification

Samples from SPW or MLM prototype run can be used for qualification

Qualification includes :

- Characterization : Cpk values
- Life tests or burn-in
- Humidity storage
- Temperature cycling
- Pressure Cooker
- Low temperature life tests

Logistics for volume production (1)

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Request for Quote

- Budgetary quote based on customer ASIC specification (# gates, I/Os, memories, test, package, …), technology and volume including die size estimation

Prototypes

- Prototype fabrication on MPW (or SPW)

Contract

- Includes fixed pricing, technical specifications, delivery times

Package development if not open-tool package available

Test board and program development by European Test house

- Prototype testing / debugging

Qualification

- Depending on customer specifications

Logistics for volume production (2)

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Volume production

- Pilot run = SPW prototype run = production mask set + few wafers needed to have production mask set
- Forecasting in order to reserve capacity at foundry
- Wafer production : 12 or 25 wafers up to +1000 wafers per year per product
- Transfer Test board and software to Far-East test house
- Probing
- Assembly of good dies
- Final test
- Delivery to customer

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Recent HEP related collaboration examples

PSI Switzerland - SLS Detector Group UMC L250

- SLS11 (pilot run =[maskset + wafers])
- PSI50 (pilot run)

CERN IBM

- SYNC (Assembly + test)
- CARIOCA (Assembly + test)
- CARIOCAGEM (Assembly + test)

INFN ROMA UMC L180

- CMA (pilot run + Assembly + test)

INFN FERRARA UMC L180

- AMCHIP (pilot run + Assembly + test)

INFN PISA UMC L180

- XPOL (pilot run)

University of Heidelberg UMC L180

- TRAPP (multiple chips on pilot run)
- OASE
- ATOLL

Europractice offers a easyCOT turnkey solution

EUROPRACTICE IC SERVICE

The Right Cocktail of ASIC Services

Easy and committed access to partner foundries

- Prototyping
- Small and medium volumes

Wide spectrum of technologies

easyCOT : Europractice is interface with subcontractors

Turnkey solution

- Libraries + IP@prototype
- Layout
- Wafer fabrication
- Assembly
- Test incl. qualification

Full technical support

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