Radiation tolerance of commercial 130nm technologies for High Energy Physics Experiments

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Foreword: Total Ionizing Dose (TID)

Ionization in SiO_2

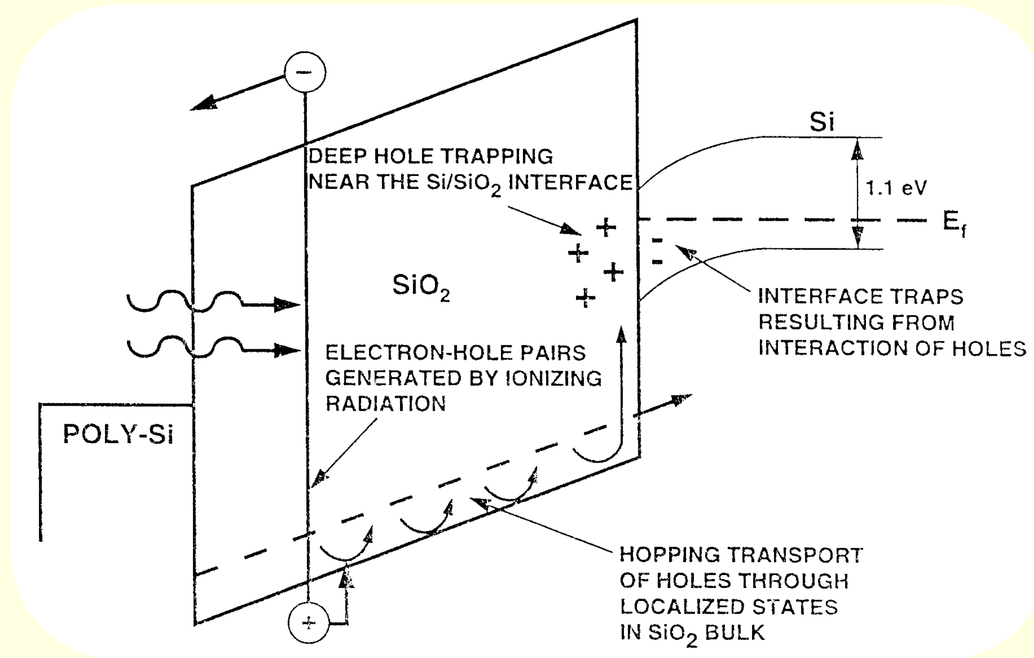
In LHC: (charged hadrons, electrons, gammas, neutrons)

Creation of electron-hole pairs

Buildup of charge/defects

Device degradation

Foreword: TID in CMOS devices



F.B.McLean et al., HDL-TR-2129 internal report, 1987

Trapped holes ➡ **Vt shift, noise, leakage**
fast formation, annealing

Interface states ➡ **Vt shift, mobility, transcond.**
Slow formation, no anneal. below 400°C

Outline

- History of HBD in 250nm CMOS
- Motivation for moving to 130nm
- TID results for 3 different Foundries
- SEE results
- Conclusion

The context: LHC needs

- Large quantities of Rad-Hard ASICs (>100K circuits for some projects)
- Radiation hardness between about 100Krad up to >10Mrad – levels well superior to typical Space applications
- Low power to relax cooling requirements
- Cheap, or at least not too expensive…

The context: available Rad-Hard processes

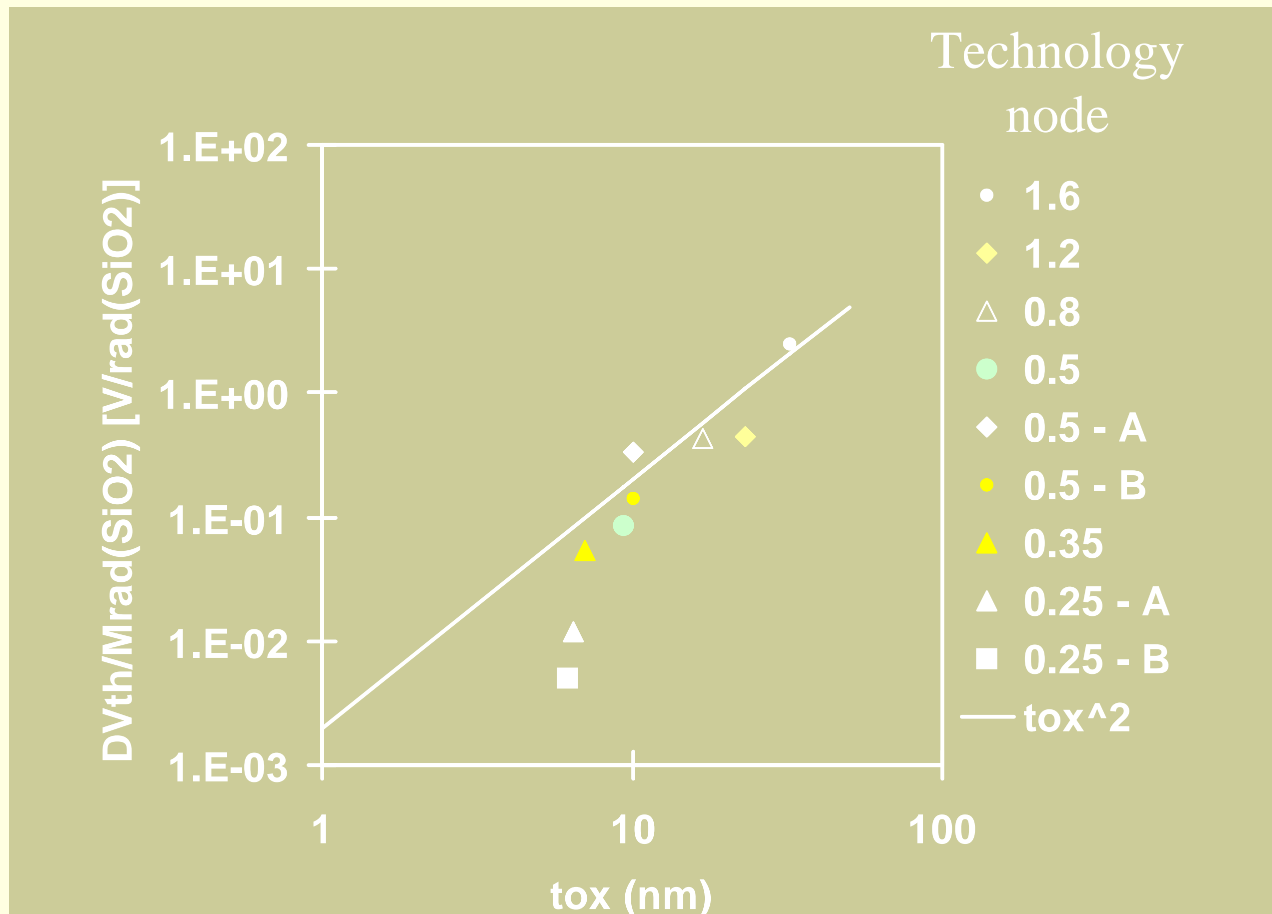
- At the beginning of the 90s, a few Rad-Hard processes were available
- Several HEP groups explored deeply the possibility to use them for mixed-signal ASIC design
- In almost all cases, this effort was unsuccessful:
  - Yield too low
  - Unreliable radiation performance for large quantities
  - Cost too high
  - Processes were discontinued or Foundry closed
  - Analog performance not very good

Looking for alternatives

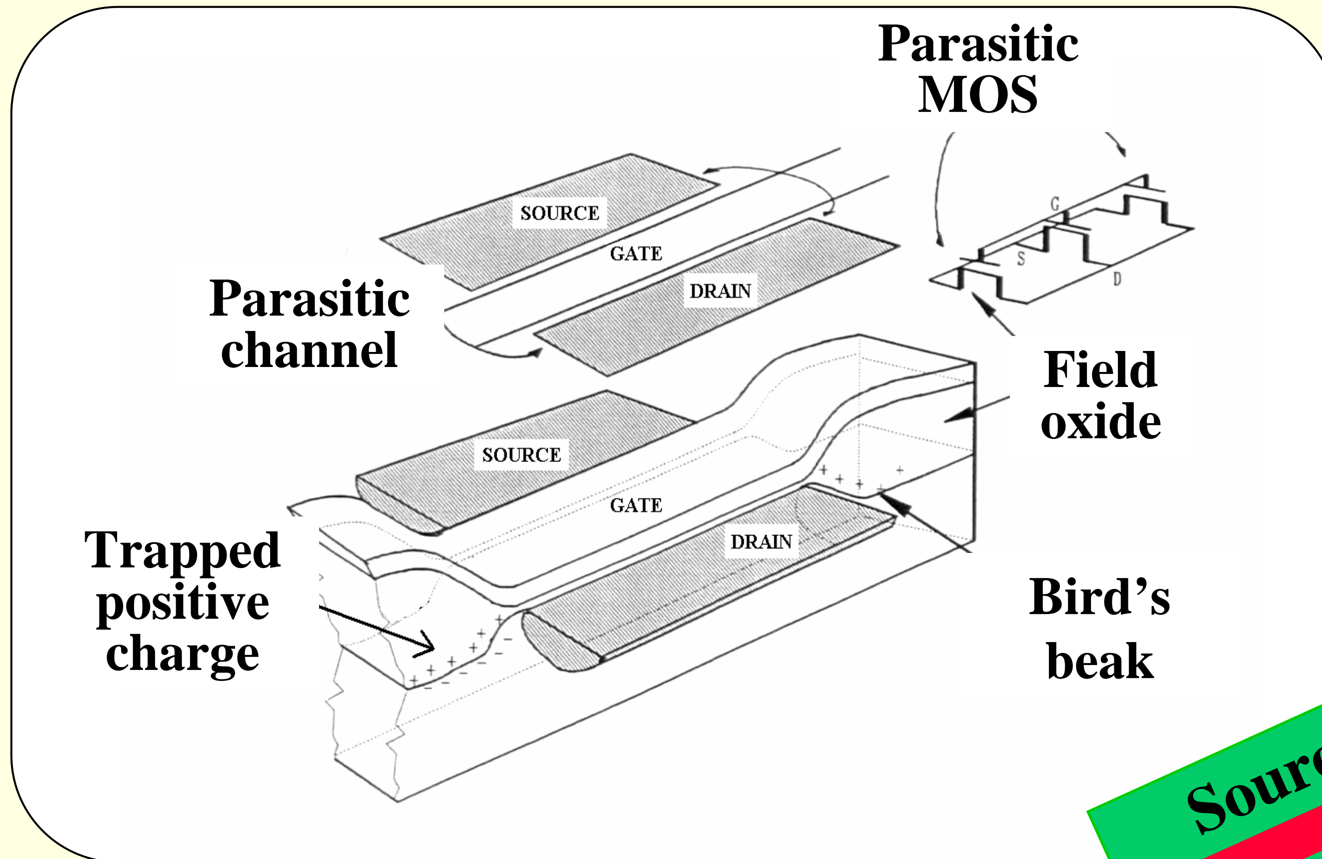
- In 1997, R&D program "RD49-radtol" started with main objective the evaluation of alternatives based on the use of commercial CMOS technologies
- Large collaboration
- Study of:
  - radiation tolerance of technologies in the 0.7-0.25μm nodes
  - layout techniques to improve radiation tolerance
  - SEE sensitivity (SEL, SEU, SEGR)

Times were mature …

- Around mid-90s commercial CMOS technologies were integrating sufficiently thin gate oxides (about 5nm) …

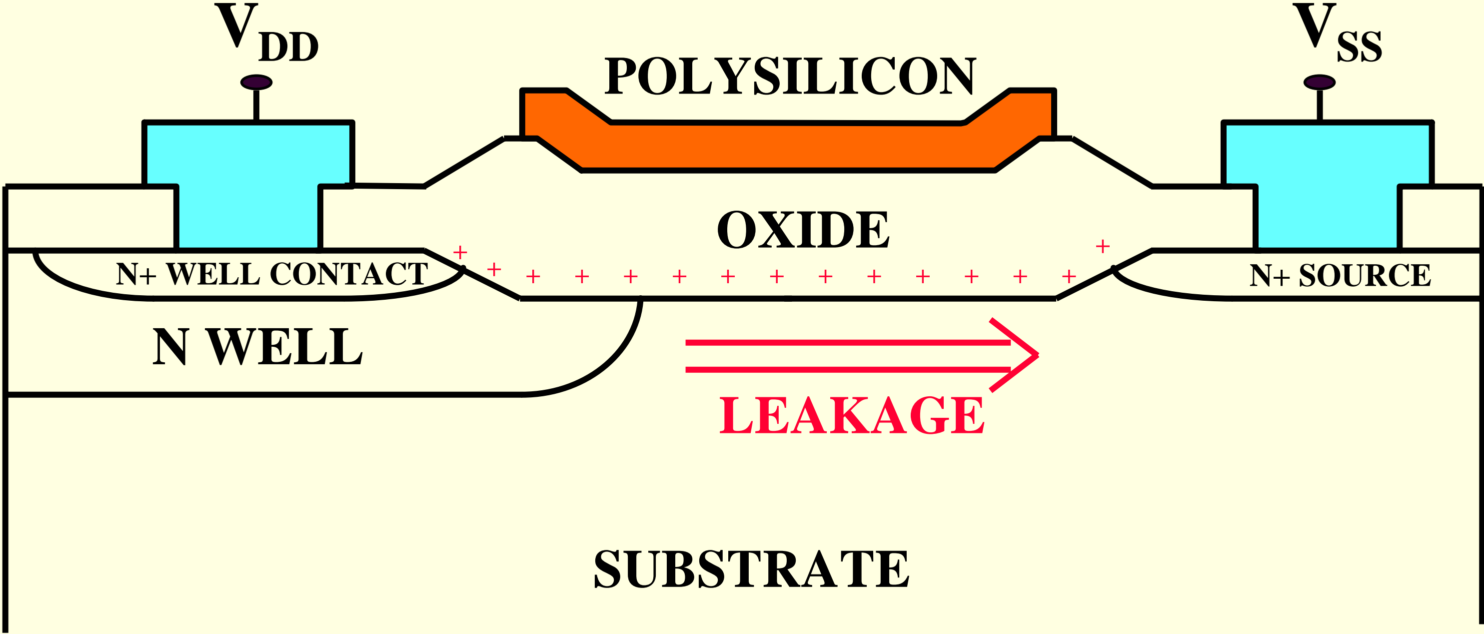


… but not all oxides are thin

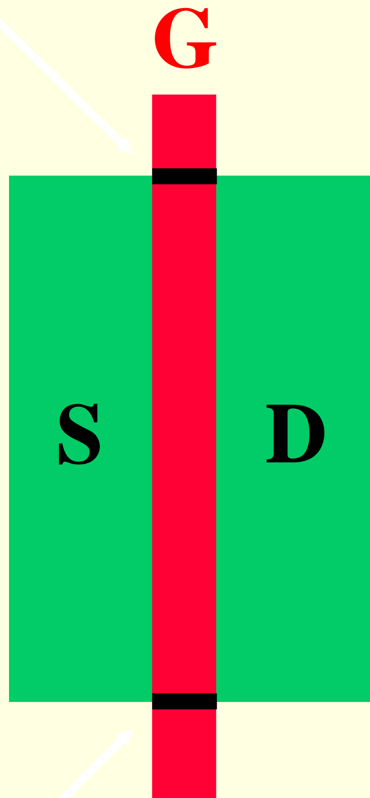


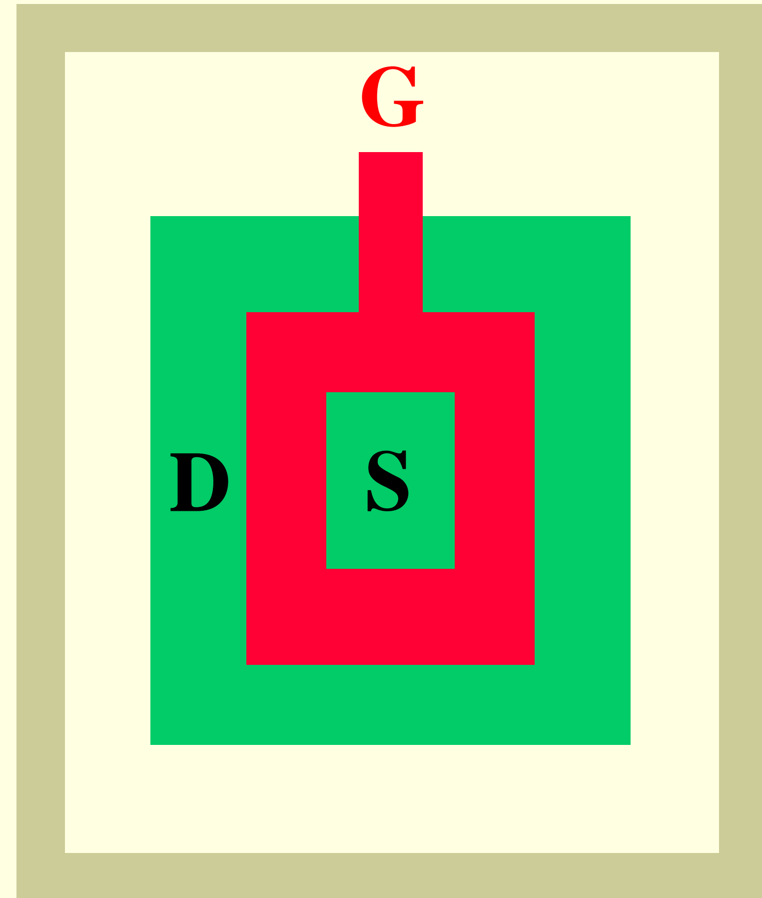
Source
Drain

IC level leakage

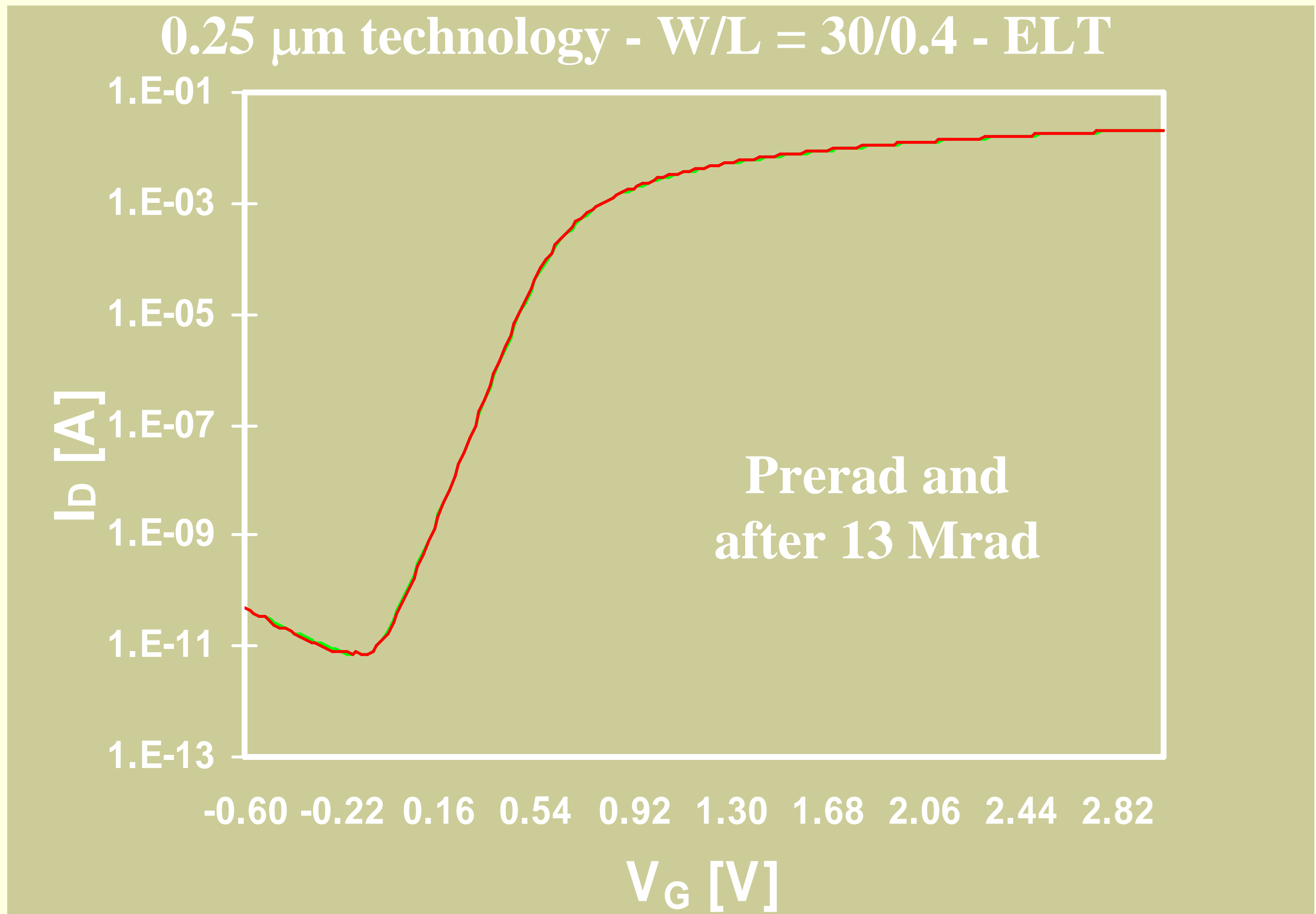


Radiation-tolerant layout (ELT)





Effectiveness of ELTs



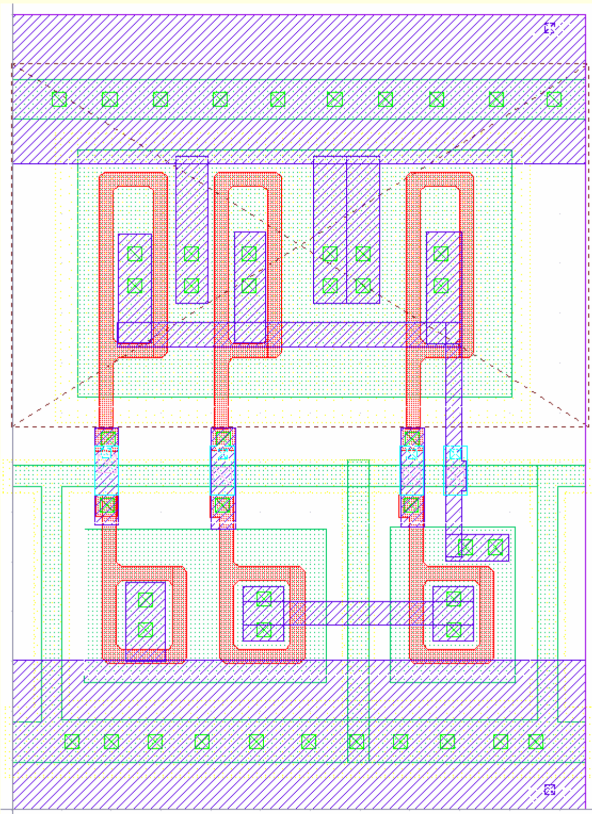
Advantages of this approach

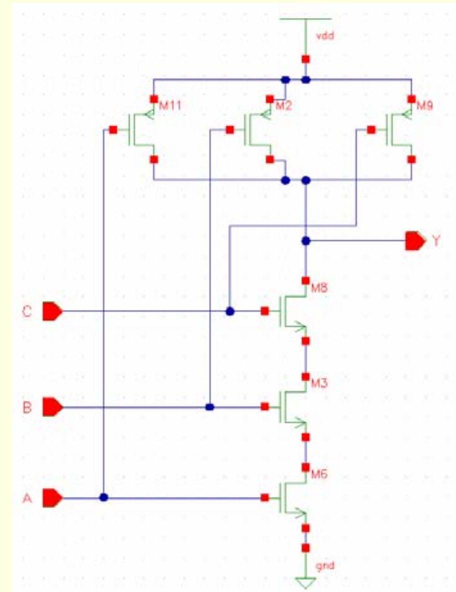
- Relies on physics (thickness of gate oxide): not process-dependent
- Allows for using state-of-the-art technologies:
  - Low power
  - High performance
  - High throughput, high yield, short turnaround times
  - Low cost

Difficulties for this approach

- Modeling of ELT (size W/L?)
- Loss of density
- Yield and reliability???
- Lack of commercial library for digital design

Lack of commercial library (1)





NAND3

Radiation tolerant design :

- Use of enclosed NMOS transistors
- Use of guard rings to isolate all n⁺ diffusions at different potentials (including n-wells)

Lack of commercial library (2)

CERNLIB Digital Standard Cells

Core Logic	Cell Name	Trans. count	Size (µm) 16x	Area (μm^2)
Boolean				
Inverter 1X Drive	E_Inv1	2	3	48
Inverter 2X Drive	E_Inv2	3	5	80
Inverter 4X Drive	E_Inv4	6	9	144
Inverter 8X Drive	E_Inv8	10	17	272
2 Input NAND	E_Nand2	4	7	112
3 Input NAND	E_Nand3	6	12	192
4 Input NAND	E_Nand4	8	14	224
2 Input NOR	E_Nor2	4	5	80
3 Input NOR	E_Nor3	6	11	176
4 Input NOR	E_Nor4	8	21	336
2 Input XNOR	E_Xnor2	12	18	288
Complex Gates				
2-Wide 2-Input AND-OR	E_AO22	10	16	256
2-Wide 2-Input AND-OR-INVERT	E_AOI22	8	13	208
2-Wide 2-Input OR-AND-INVERT	E_OAI22	8	12	192
Multiplexers				
2-Input MUX	E_Mux2	12	18	288
4-Input MUX	E_Mux4	28	40	640
Buffers				
Buffer X4 Drive	E_Buf4	8	11	176
Buffer X8 Drive	E_Buf8	16	26	416
Simple Cells				
Logic 0	LOGIC0	2	3	48
Logic 1	LOGIC1	2	3	48
Adders				
1-bit Half Adder	E_HAD1	18	27	432
1-bit Full Adder	E_FAD1	34	45	720
Flip Flops				
Static D FLIP-FLOP	E_dff	24	33	528
Static D FLIP-FLOP with Reset	E_dff_R	28	41	656
Static D FLIP-FLOP with Set	E_dff_S	28	41	656
Static D FLIP-FLOP with Set & Re	E_dff_SR	32	47	752
Static D Flip Flop with Scan	E_dff_SR_SC	40	59	944
Dynamic TSPC D FLIP FLOP	E_TSPC	11	19	304
Latches				
D-Latch	E_LD	18	25	400
D-Latch with Reset	E_LDR	21	29	464

I/O Logic	Cell Name	Trans. count	Size (µm) 458x	Area (μm^2)
Output Pads				
8mA Drive Standard	OB8mA	16	115	51865
16mA Drive Standard	OB16mA	26	115	51865
20mA Drive Standard	OB20mA	34	115	51865
8mA Drive with Slew Rate control	OBSR8mA	14	115	51865
16mA Drive with Slew Rate control	OBSR16mA	30	115	51865
20mA Drive with Slew Rate control	OBSR20mA	38	115	51865
Input Pads				
CMOS Inverter Input	IB1	6	115	51865
Simple PAD	INPAD	0	115	51865
LVDS I/O Pads				
LVDS TX	LVDStx	33	235	105985
LVDS RX	LVDSrx	18	235	105985
I²C interface I/O Pads				
20mA Open Drain Output	OD20mA	9	115	51865
Bidirectional with 20mA Open Drain	IOD20mA	17	115	51865
Power Pads				
VDD for periphery & core	VDD	0	115	51865
VDD for periphery	VDD_CORE	0	115	51865
VDD for core	VDD_PERI	0	115	51865
VSS for periphery & core	VSS	0	115	51865
VSS for periphery	VSS_CORE	0	115	51865
VSS for core	VSS_PERI	0	115	51865
Corner for I/O periphery	CORNER	0	115	51865
Guard-ring cells				
Endcap Cell Left	CAPL	0	115	51865
Endcap Cell Reft	CAPR	0	115	51865
Filler Cell	FILLERCELL	0	115	51865

- List of Library Standard Cells

Lack of commercial library (3)

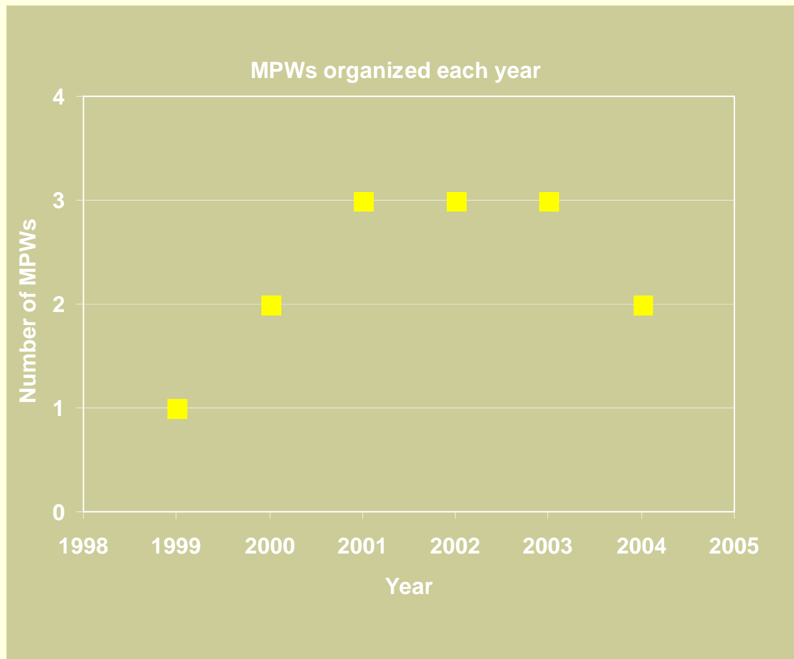
- Development of a “Design Kit” for CADENCE DFII version 97a
- Supported Design Flows:
  - Analog
    - Analog simulations (HSPICE).
    - Device extraction.
    - Physical Design Verification (DIVA, DRACULA).
  - Digital
    - Logic Synthesis (SYNOPSYS).
    - Digital Simulations (VERILOG).
    - Place & Route (SILICON ENSEMBLE).
  - Mixed Signal
    - Simulations (HSPICE/VERILOG).

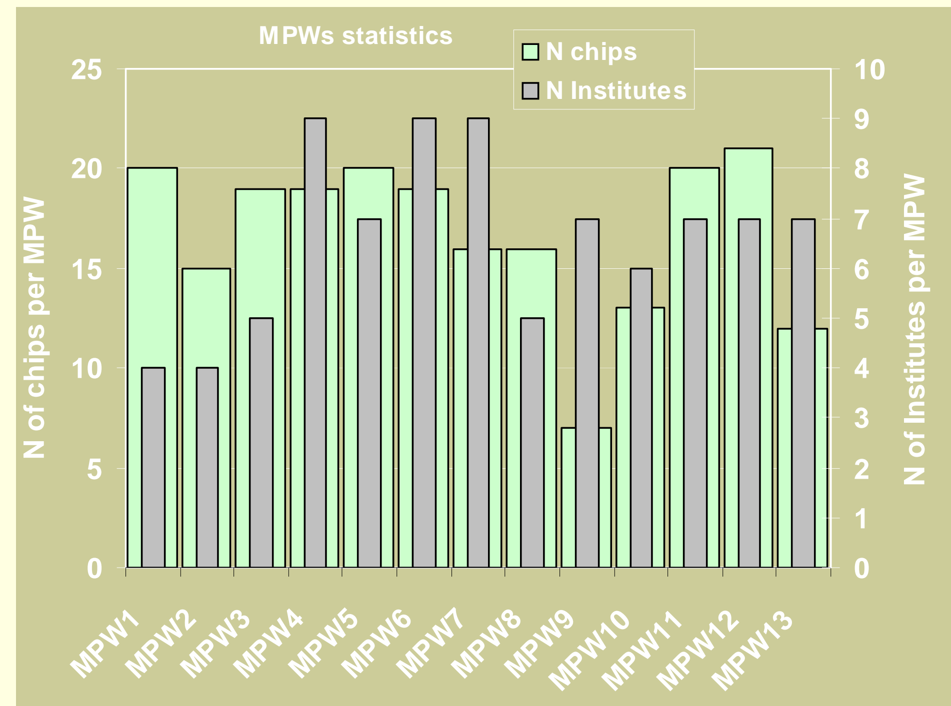
HEP foundry service

- CERN selected a single supplier for foundry service (ASICs), and organized itself a service for High Energy Physics (HEP) Institutes
- All HEP institutes can have access to this service
- CERN acts as contact point for the service (technical, administrative, legal aspects)
- Organization of Multi Project Wafer (MPW) runs, “dedicated” engineering runs and production, mainly related to ASIC need for the LHC

MPW service

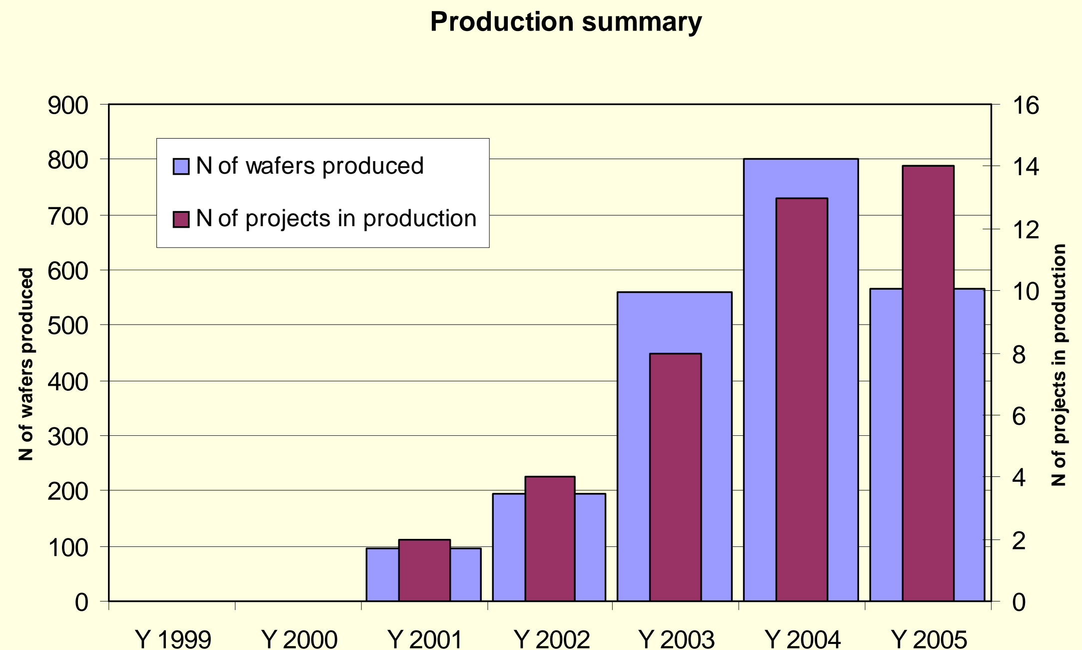
Total number of chips integrated > 200
Institutes involved: > 20





HEP Foundry Service

- MPW service organized for more than 100 different ASICs
- More than 20 different designs in production (some are multi-ASIC)
- More than 2000 wafers (8-inch) produced!



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Motivation to move to 130nm

- LHC upgrades & SLHC will require higher-performance ICs, tolerant to larger TID levels
- 250nm is already an old process and will not stay around much longer
- More-modern CMOS processes have the potential of higher TID tolerance and much better performance

Motivation to move to 130nm

1965: Number of Integrated Circuit components will double every year

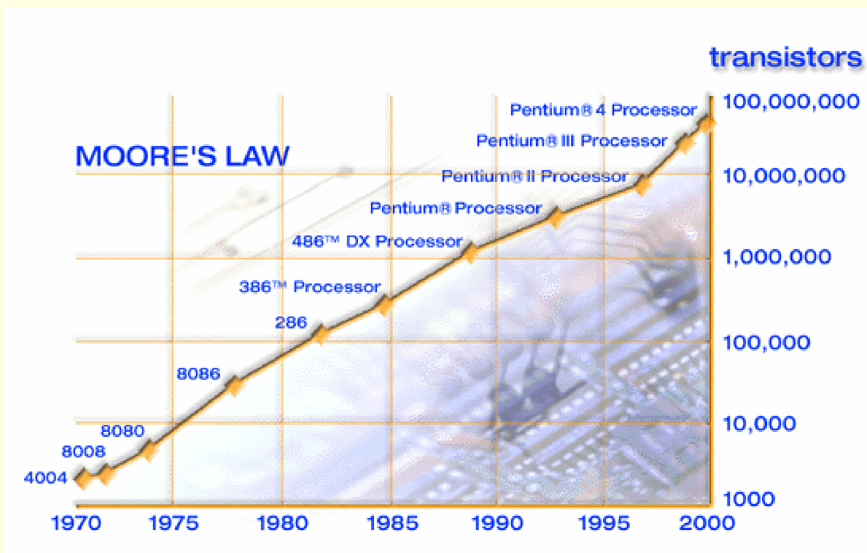
G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

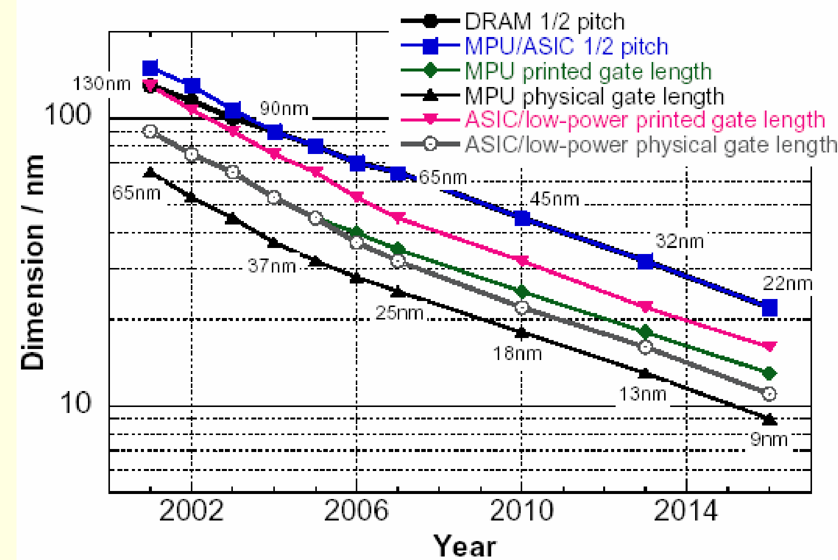
1975: Number of Integrated Circuit components will double every 18 months

G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM 1975*.

1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996

P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.





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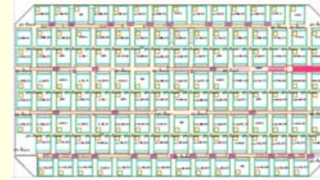
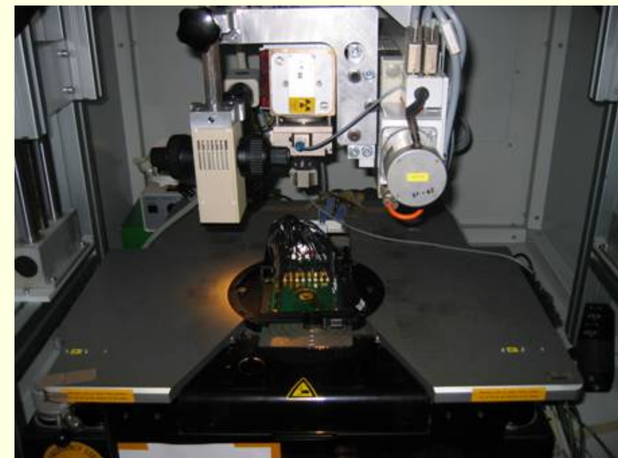
Test structures and measurement setup

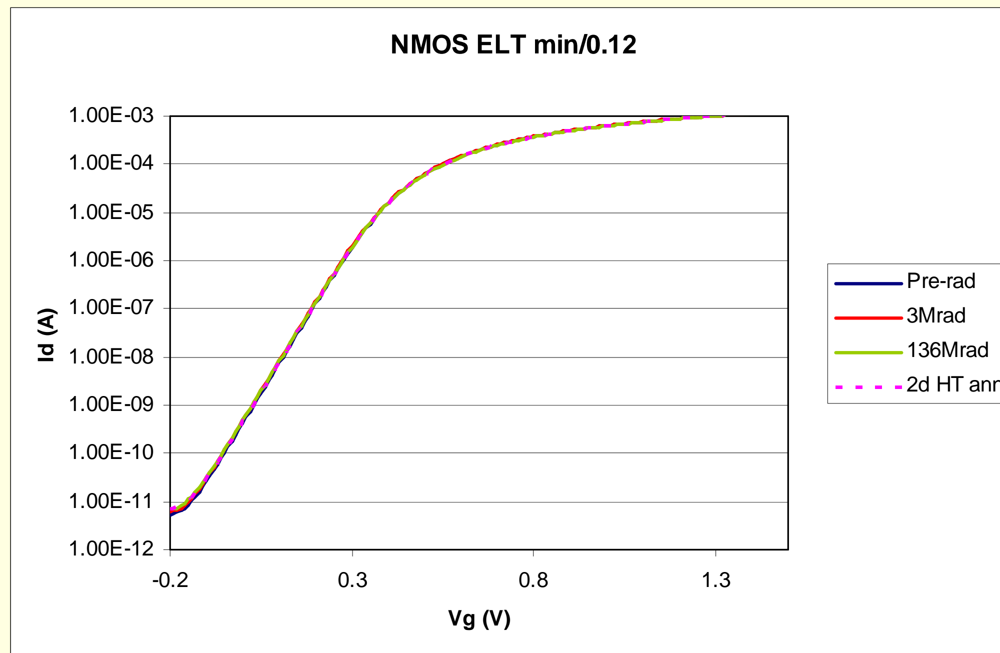
- 3 commercial 130nm CMOS processes: foundries A,B and C
- Some are PMDs from foundry, some custom-designed test ICs
- NMOS and PMOS transistors, core and I/O devices (different oxide thickness), FOXFETs
- Testing done at probe station – no bonding required
- Irradiation with X-rays at CERN up to 100-200Mrad, under worst case static bias





Core NMOS transistors, enclosed layout (ELT)

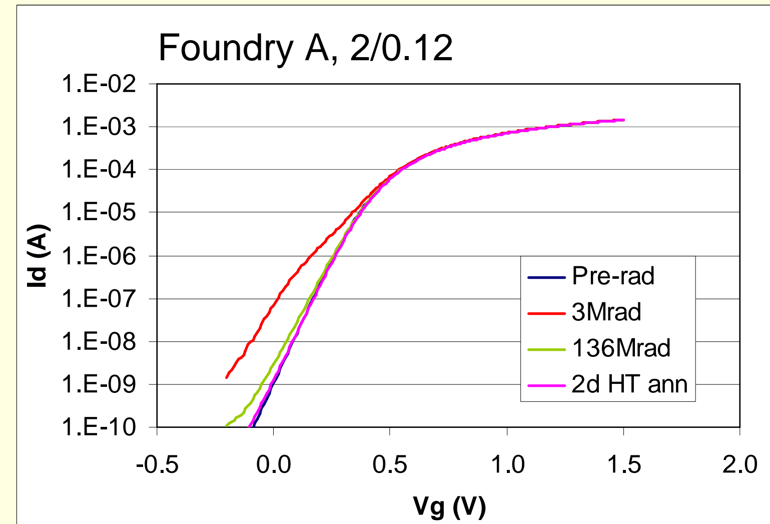
- The radiation hardness of the gate oxide is such that practically no effect is observed – verified for 2 foundries (A up to 140Mrad, B up to 30Mrad)

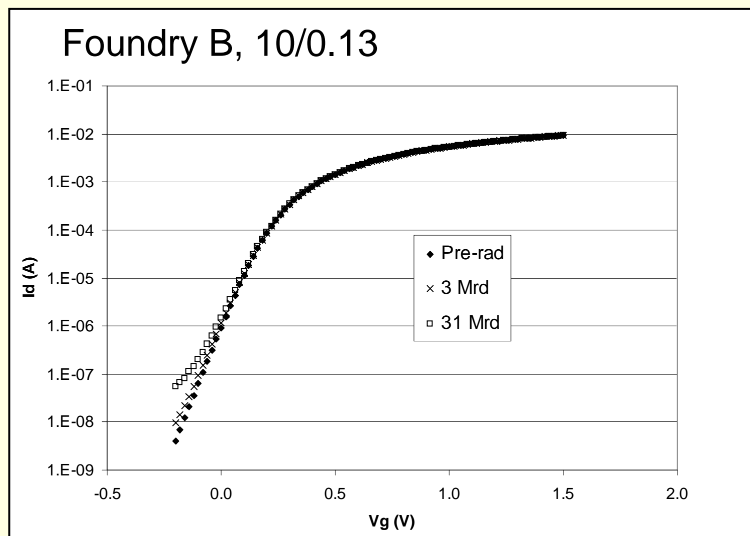


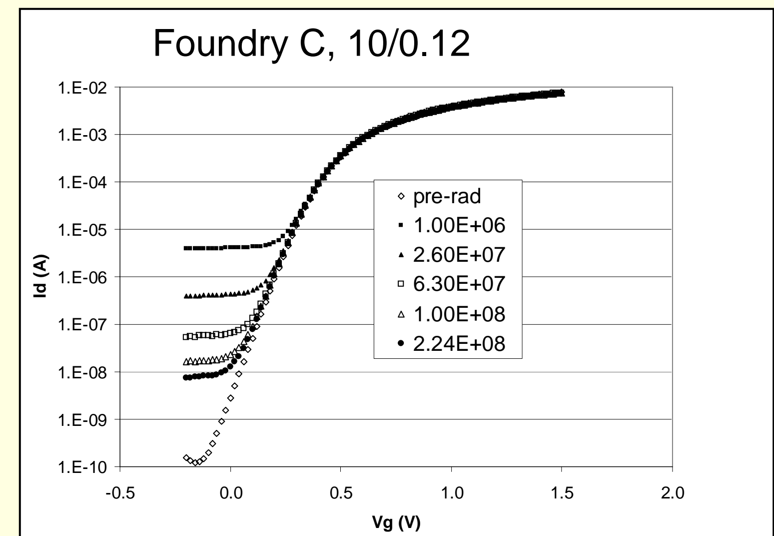
Example: Foundry A

Core NMOS transistors, linear layout (1)

- Wide transistors (W > 1μm):
  - Results different with Foundry
  - When the transistor is off or in the weak inversion regime:
    - Leakage current appears (for all transistor sizes)
    - Weak inversion curve is distorted

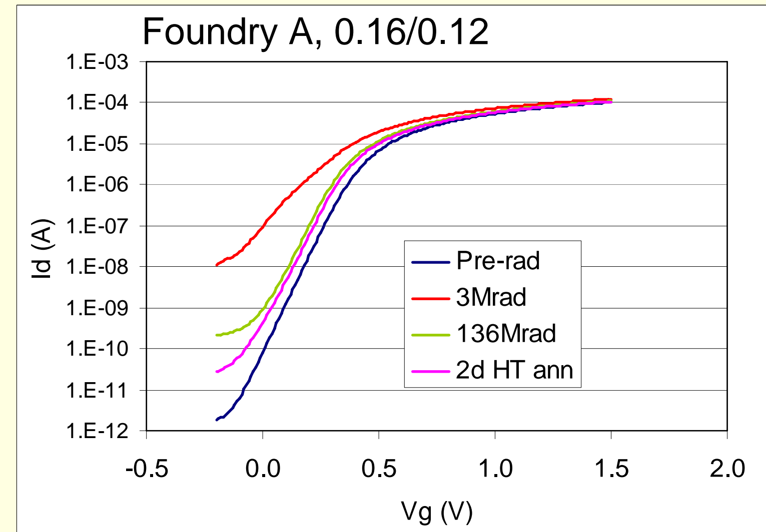


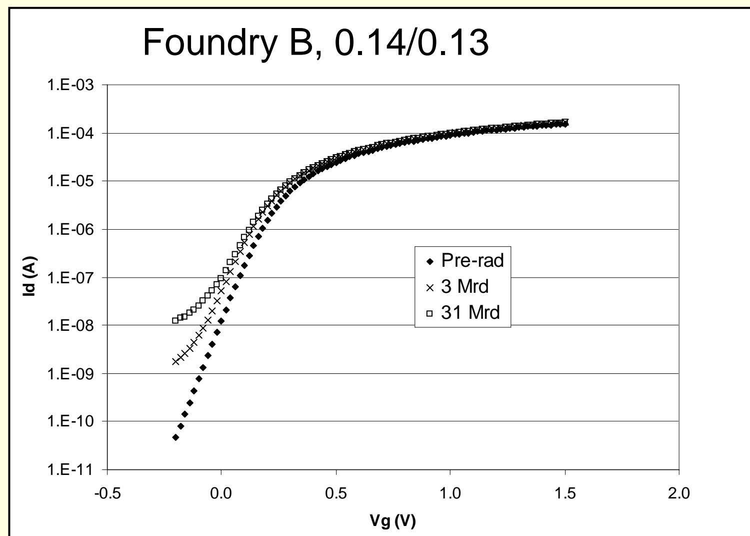


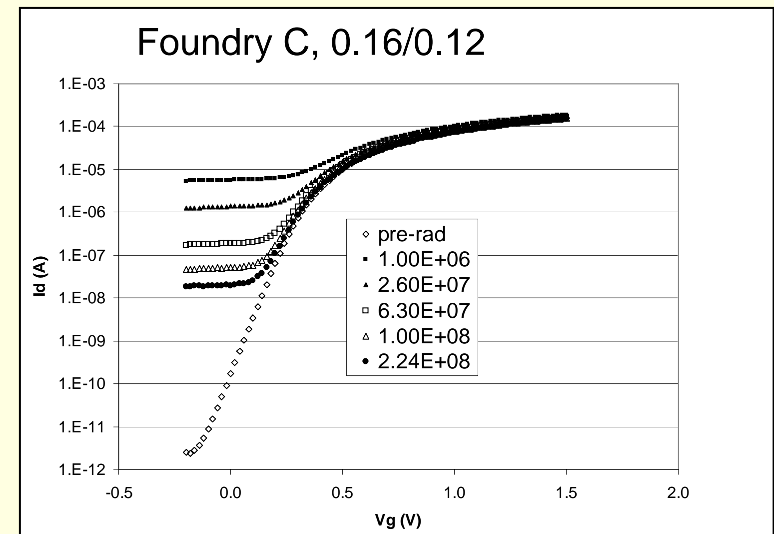


Core NMOS transistors, linear layout (2)

- Narrow transistors (W < 0.8μm):
  - Results different with Foundry
  - An apparent Vth shift (decrease) for narrow channel transistors
  - The narrower the transistor, the larger the Vth shift (RINCE)

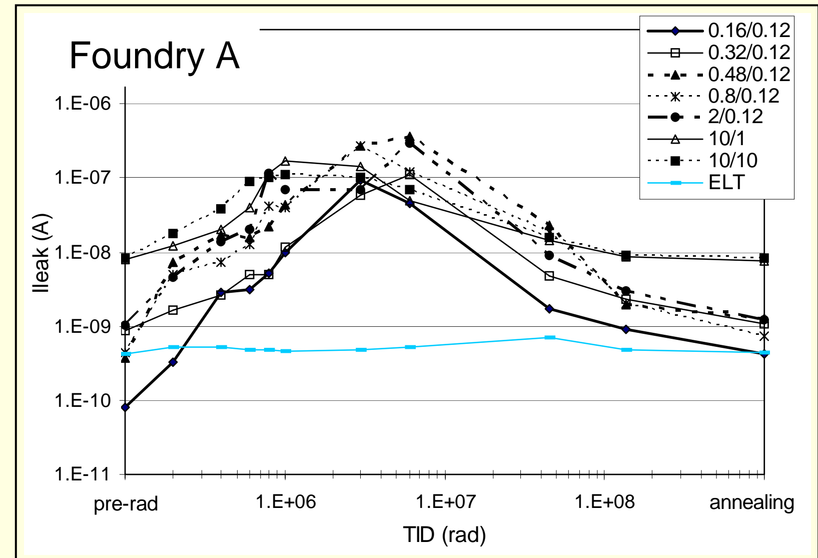


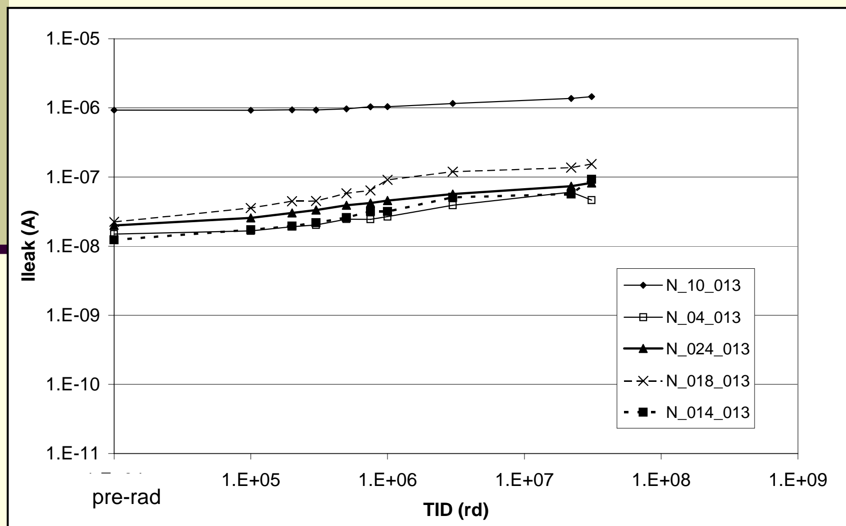


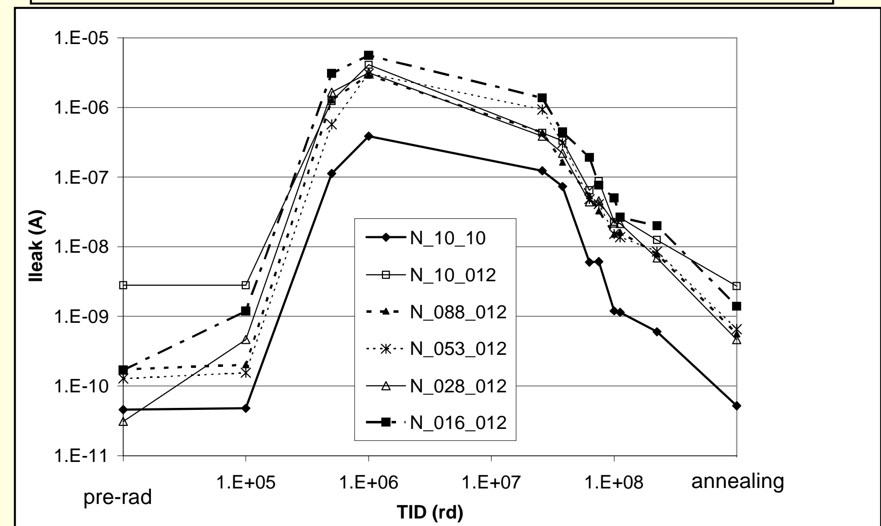


Core NMOS transistors, linear layout (3)

- Effect on the leakage current
  - Peak in leakage at a TID of 1-5Mrad
  - Peaking dependent on dose rate and temperature, difficult to estimate in real environment

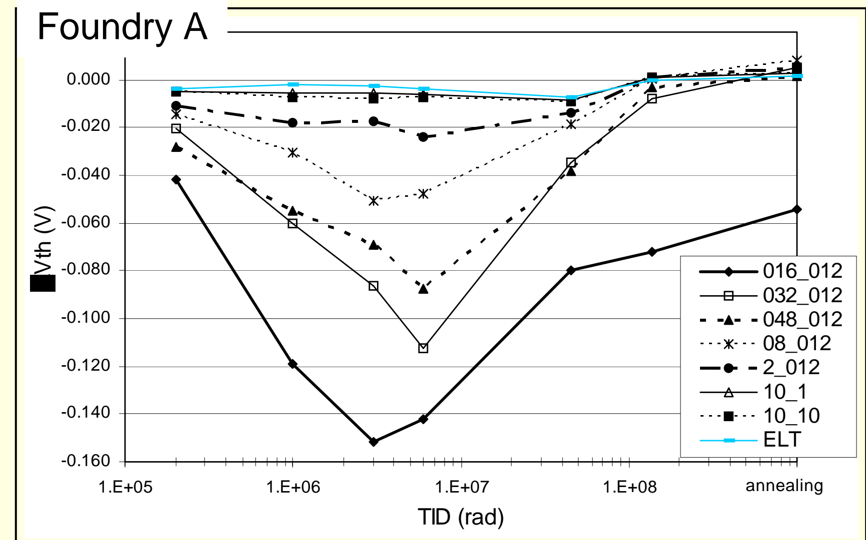


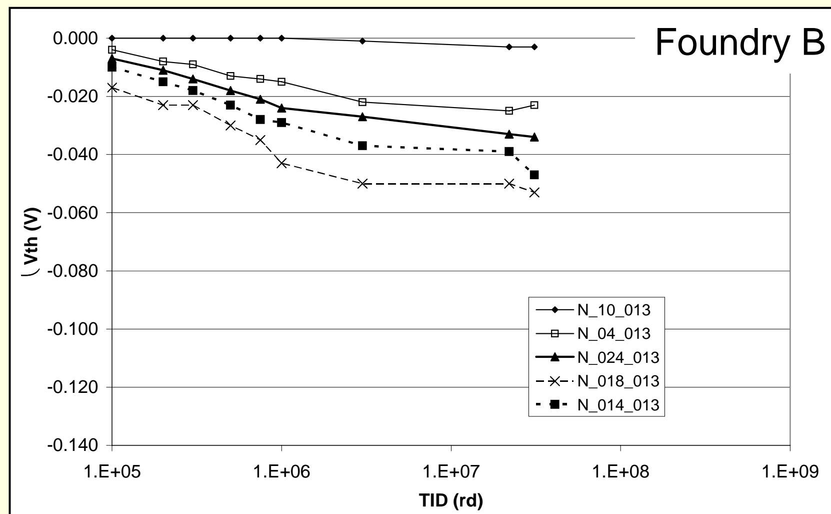


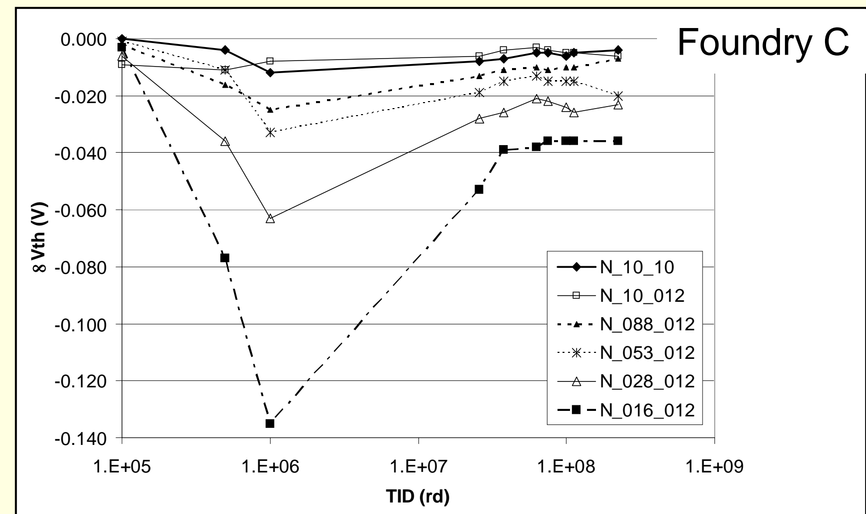


Core NMOS transistors, linear layout (4)

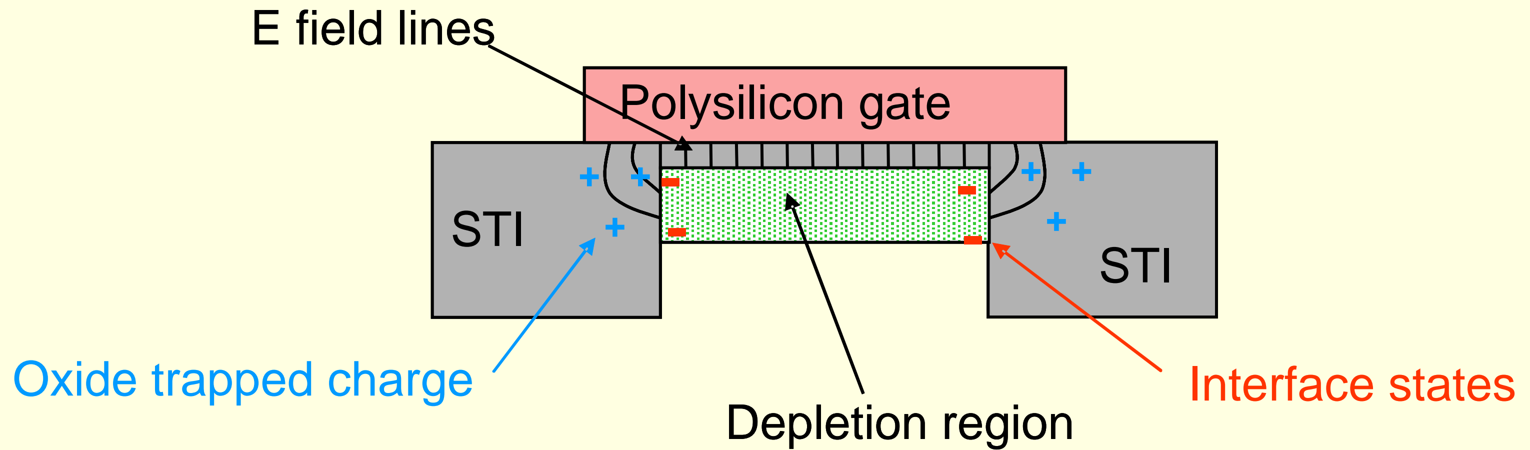
- Effect on the threshold voltage
  - Peak in Vth shift at a TID of 1-5Mrad (A and C)
  - The narrower the transistor, the larger the Vth shift (RINCE)
  - Peaking dependent on dose rate and temperature, difficult to estimate in real environment

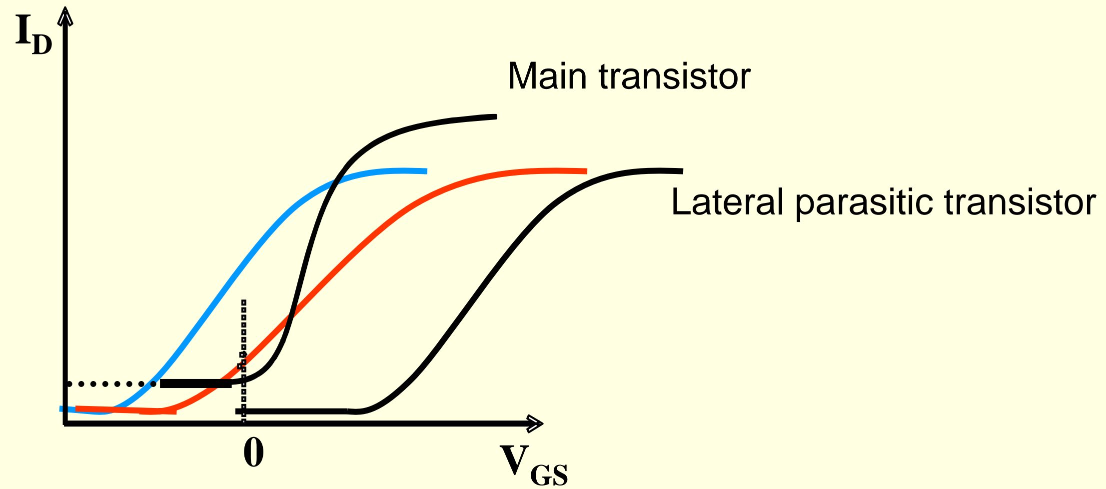






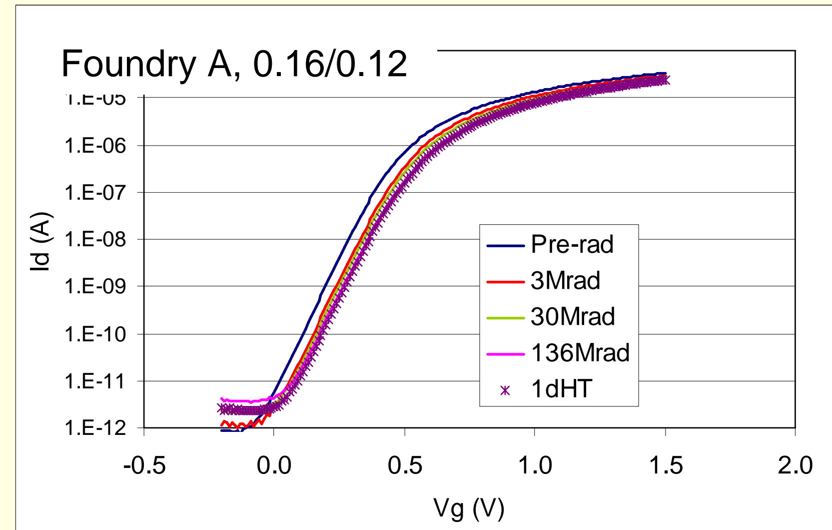
Radiation-induced edge effects - NMOS

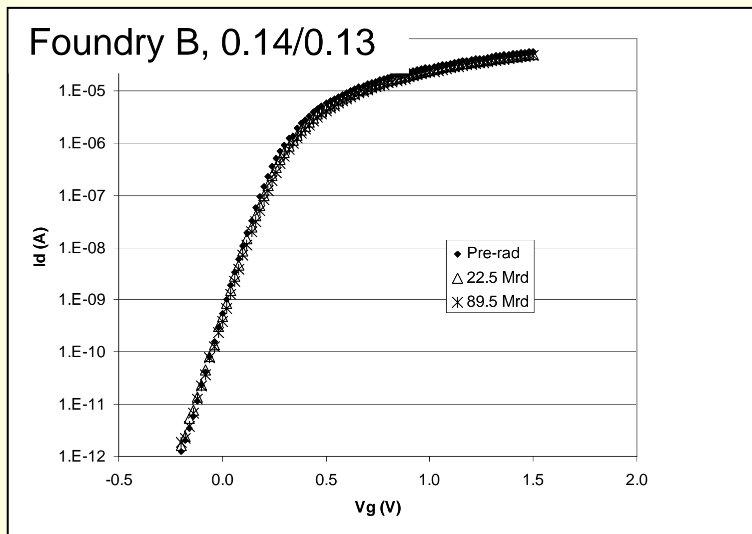


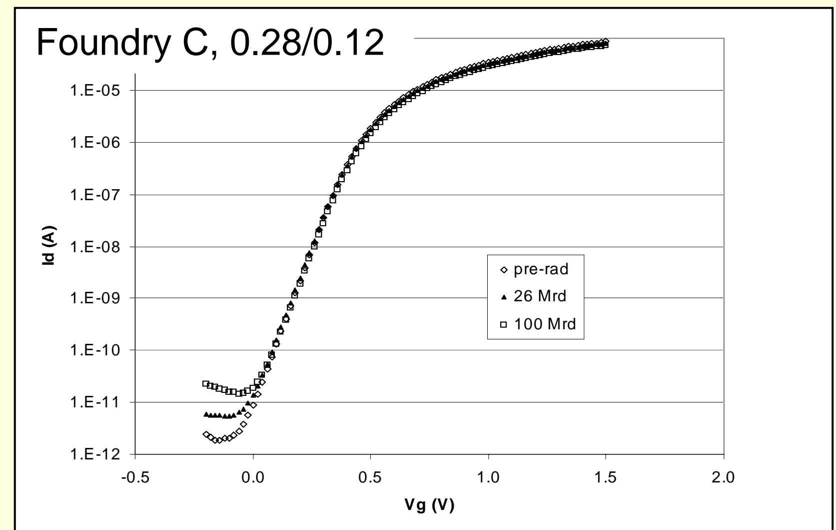


Core PMOS transistors, linear layout (1)

- No change in the weak inversion regime, no leakage
- An apparent Vth shift (decrease) for narrow channel transistors
  - The narrower the transistor, the larger the Vth shift

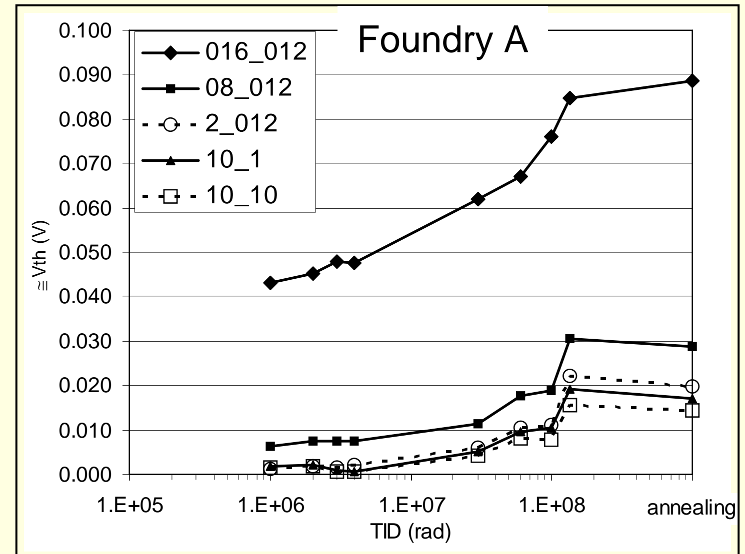


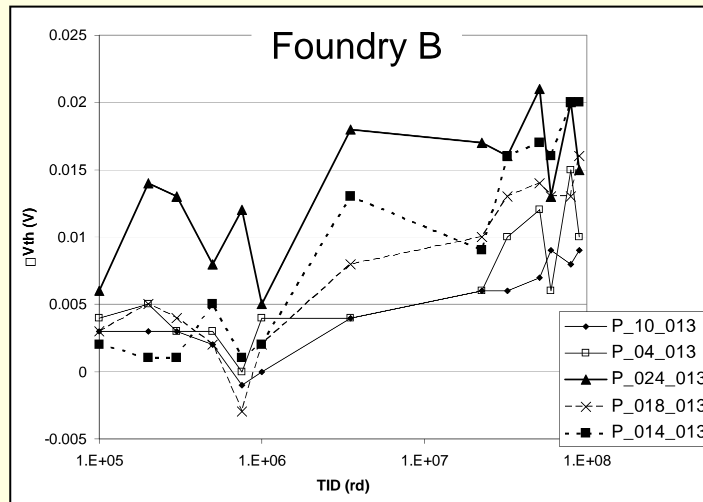


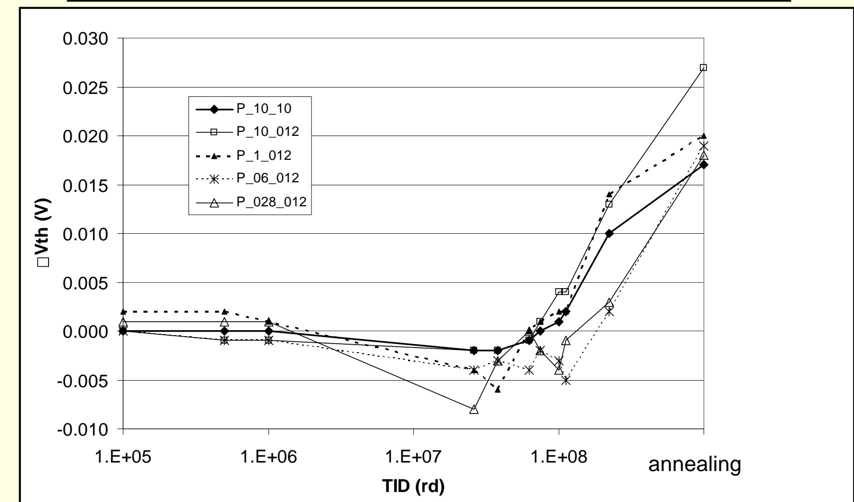


Core PMOS transistors, linear layout (2)

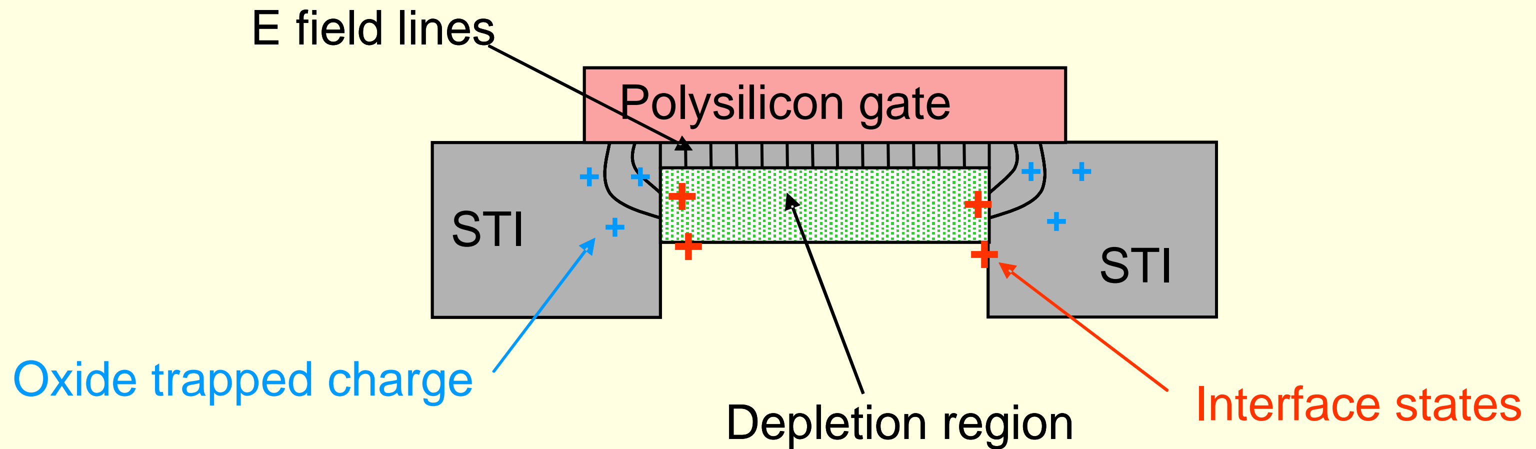
- There is no peak here, but a continuous shift of Vth
- The effect is more pronounced for narrow transistors

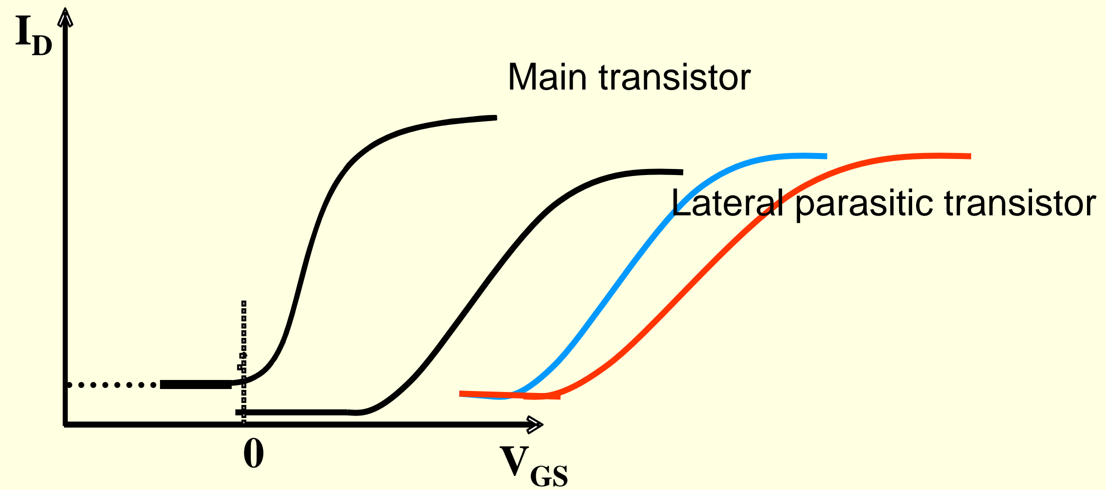






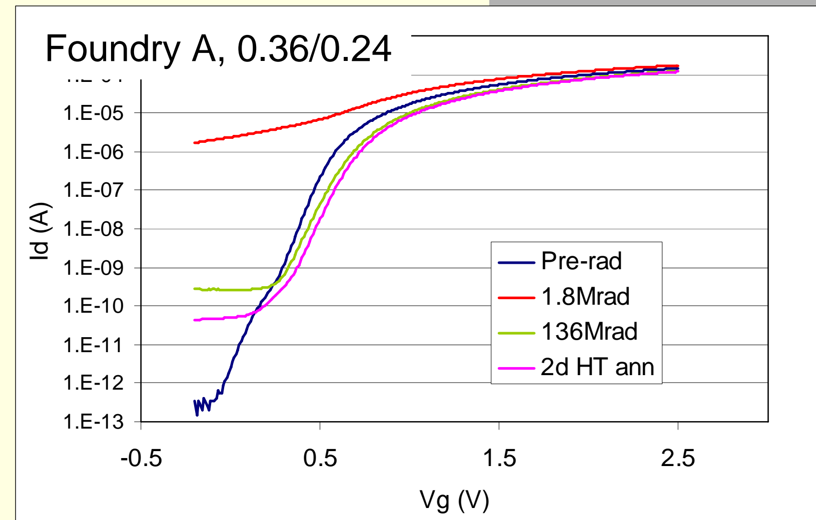
Radiation-induced edge effects - PMOS

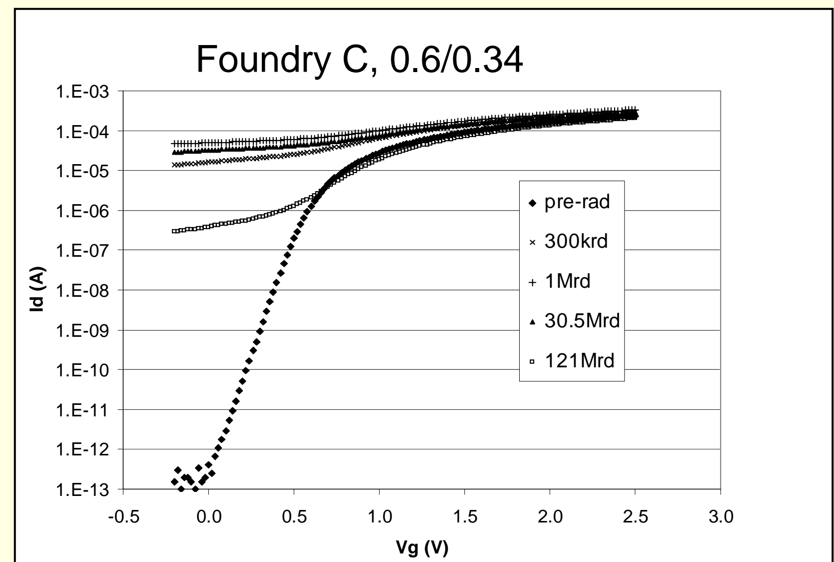




I/O NMOS transistors, linear layout

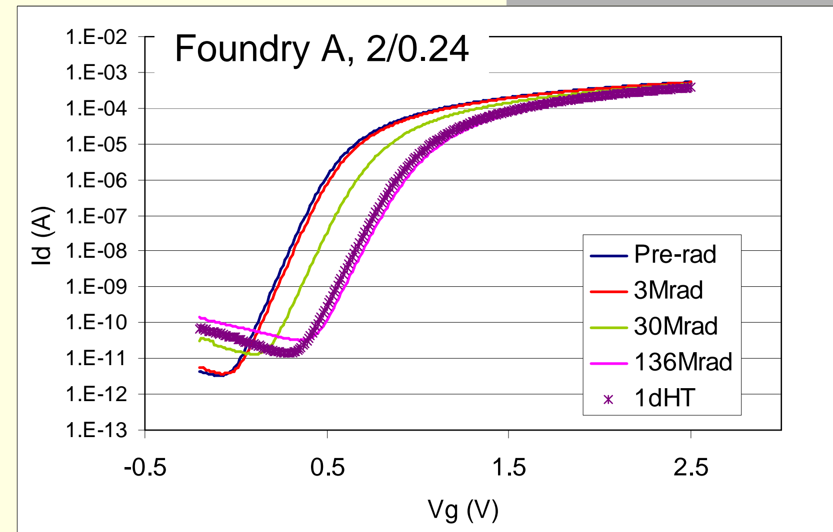
- Large effect for all sizes, but more important for narrow channel transistors
- Results different with Foundry, but for all HBD techniques are required already for TID levels of the order of 50-100krad

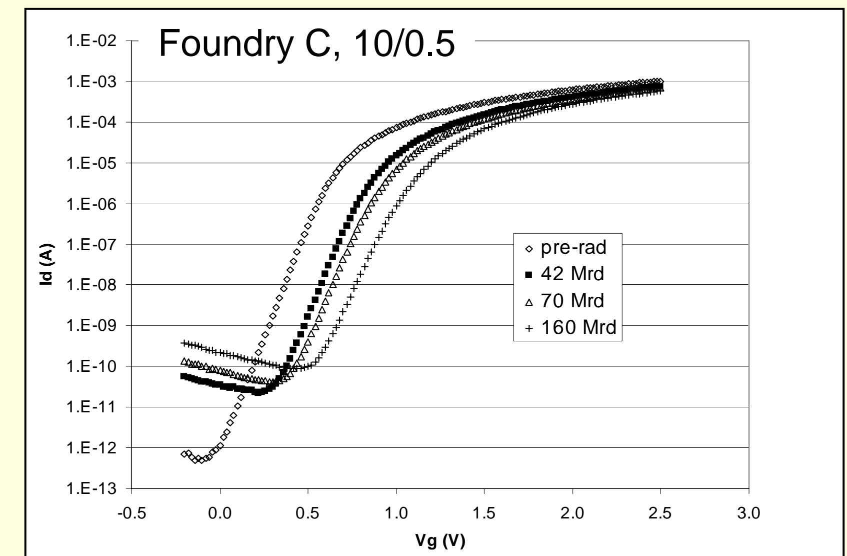




I/O PMOS transistors, linear layout (1)

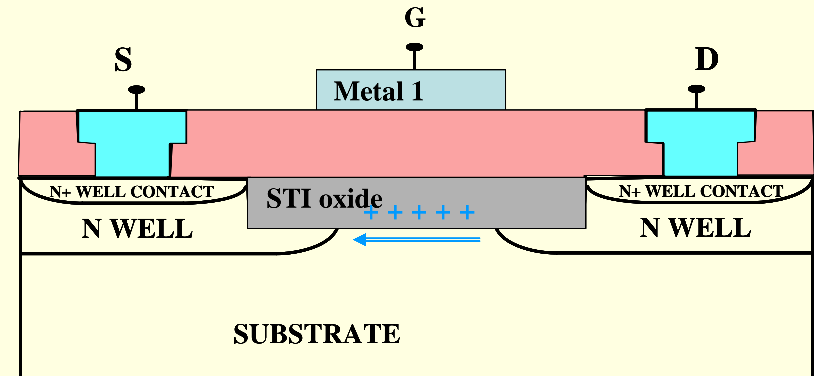
- Large effect on Vth for all sizes, but more important for narrow channel transistors

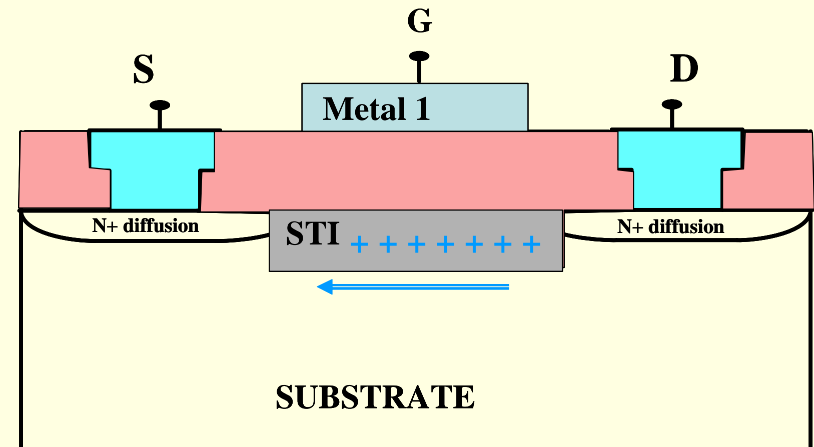




FOXFETs (isolation test)

- FoxFETs are “Field Oxide Transistors”
- Good to characterize isolation properties with TID
- Source-Drain could be either Nwells or n+ diffusions
- Structures available in only 1 technology (1 only Foundry)

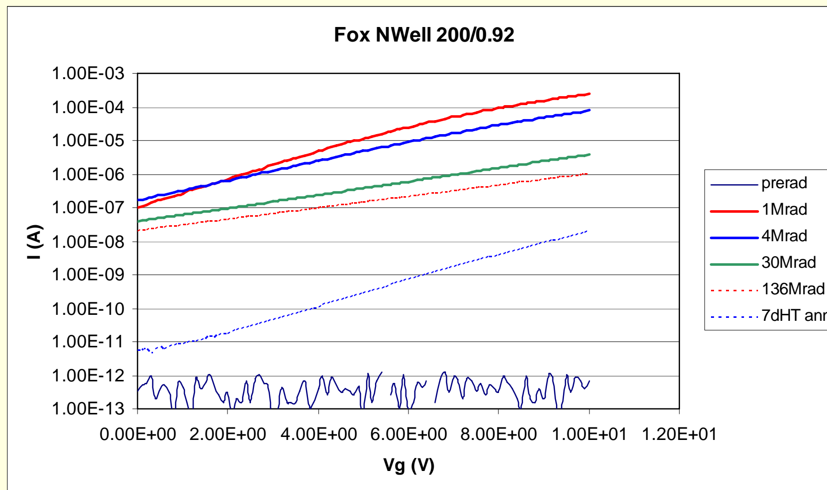


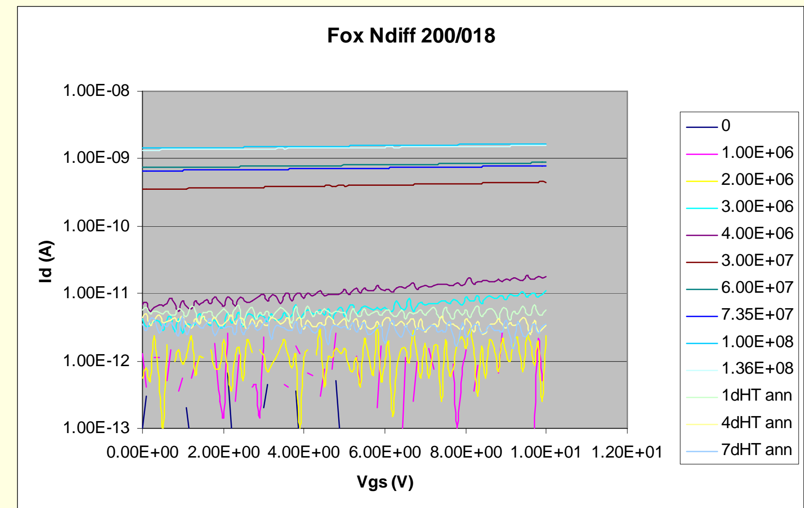


FOXFETs

- Also in this case, a « peak » can be distinguished (isolation oxide has similar properties to lateral oxide)
- Not a problem for digital (all wells at Vdd, low level of inter-transistor leakage), but care must be used for full custom to avoid large effects

Foundry A





Outline

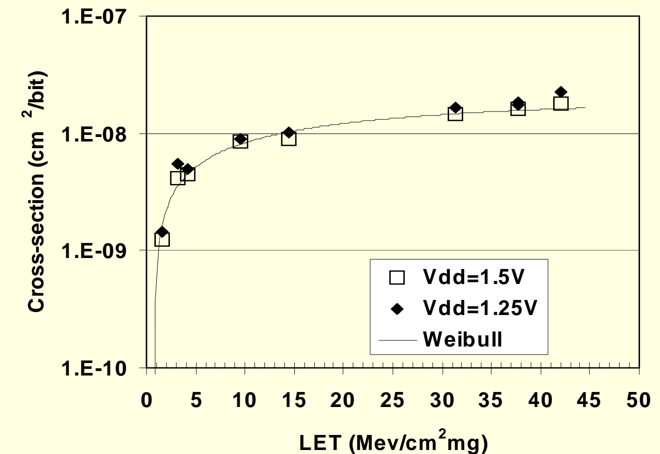
- History of HBD in 250nm CMOS
- Motivation for moving to 130nm
- TID results for 3 different Foundries
- SEE results
- Conclusion

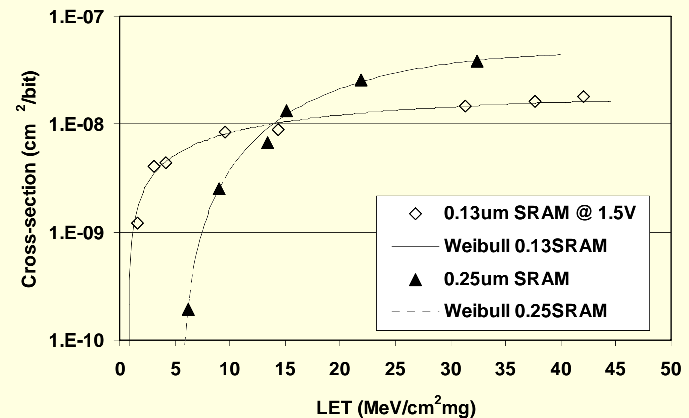
SEE results: the SRAM circuit

- 16kbit SRAM test circuit designed using the SRAM generator from a commercial library provider – not dedicated rad-tolerant design!
- Test performed with Heavy Ions at the Legnaro National Laboratories accelerator in June 2005

Heavy Ion irradiation results

- Test at Vdd=1.5 and 1.25 V, results very similar
- Sensitivity to very low LET values (threshold below 1.6 MeV/cm²mg)
- Comparison with 0.25μm memory (rad-tol design!!):
  - Cross-section 15-30 times larger in LHC environment





Challenges for 130nm

- Technology more expensive than ¼ micron:
  - Strong push for first working silicon
  - Strong push for common solutions to similar problems
- Technology more complex than ¼ micron:
  - Reduced Vdd, difficult for analog
  - Physical effects can not be ignored: proximity effects, filling requirements, "cheesing", …
  - As a consequence, design rules are considerably more complex (impressive growth of the design manual)
  - Larger number of tools is needed
- Competence in radiation effects are also required
  - If non-enclosed transistors are used
  - To protect circuits from SEEs
- All competences in technology, design techniques and tools necessary for a successful project are more difficult to gather in a group of small size

Conclusion

- HBD in quarter micron has made LHC electronics possible/affordable: large scale application of HBD is a reality!
- Natural radiation tolerance of 130nm better than for the quarter micron technology (not for I/O transistors), but Mrad-level still requires HBD for reliable tolerance
- Large effort required to develop library, acquire tools, master the technology:
  - Working with 130nm is MUCH more complex and expensive; pressure to get quickly to working silicon
- CERN is preparing a frame contract with 1 selected Foundry, to develop library/design kit/design flow serving the whole HEP community