Front-end Chip:
From CMOS 180nm to 130nm

- Introduction
- Circuit in 180nm technologies
- Challenges in 130nm technologies
- Circuit architecture
- Perspective

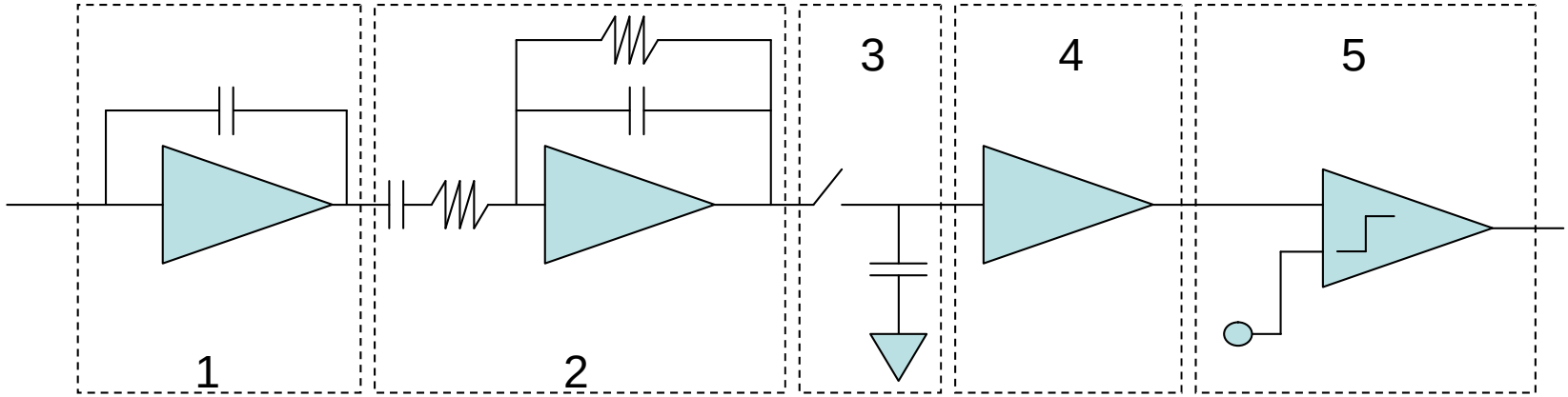
Introduction

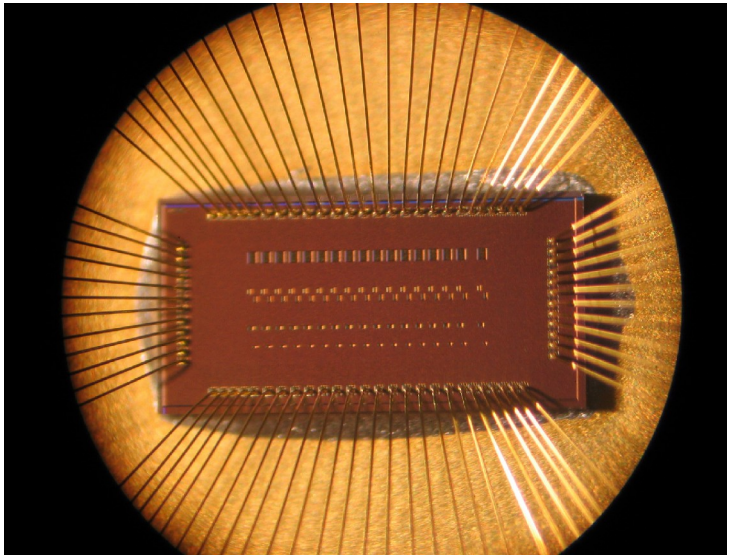
- Encouraging result from front-end in 180nm CMOS

  → Design the new front-end chip in 130nm process

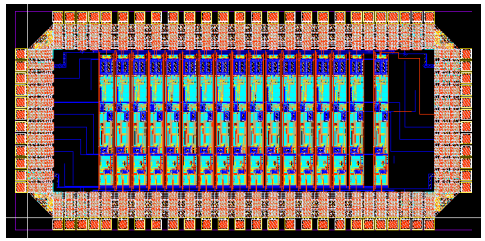
  → Less on- Si detector material, less parasitics, less power

Front-end Prototype chip in 180nm technologie





17 channels (one test Channel)



1. Low noise amplification
2. Pulse shaper
3. Sample and Hold
4. Buffer
5. Comparator

Results in 180nm

Preamp Results

- Gain: 8mV/MIP OK
- Dynamic range: 50 MIP OK
- Linearity: +/-1.5% expected: +/-0.5% -
- Noise @ 70 μW power, 3μs-20μs rise-fall times:

  498 + 16.5 e-/pF 490 + 16.5 e-/pF expected OK

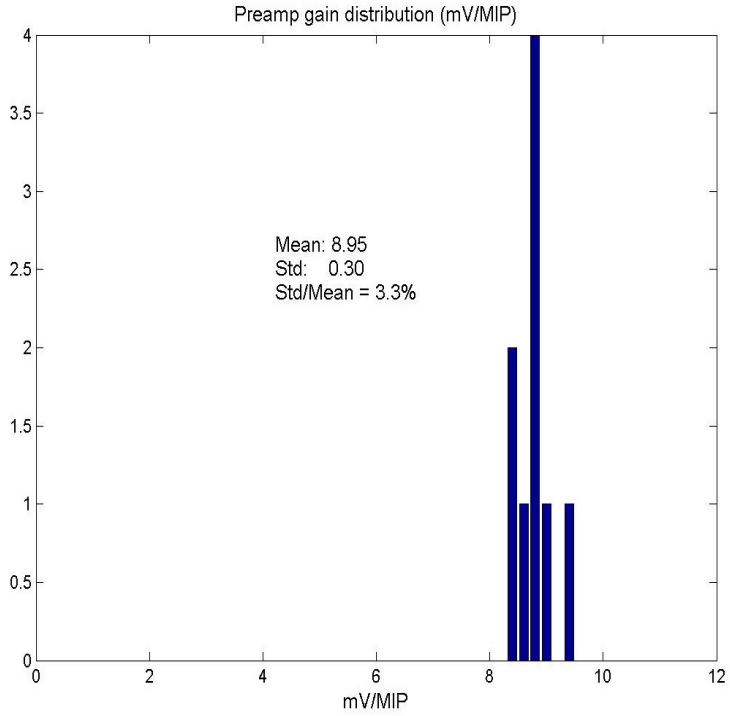
Pulse Shaper results

- Peaking time: 2-6 μs tunable peaking time vs 1-10 expected -
- Linearity: 6%, 3.5% expected -
- Noise @ 3 μs shaping time and 70 μW power:

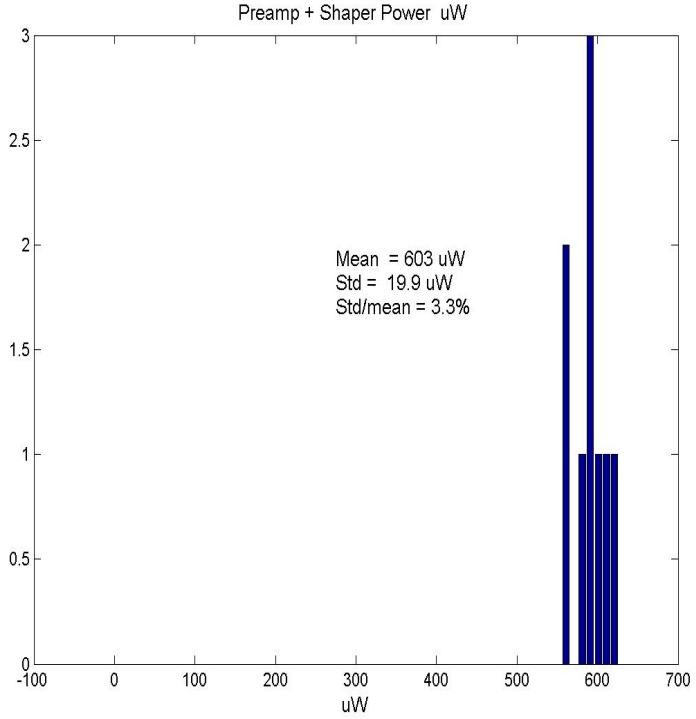
  325 + 10.1 e-/pF vs 274 + 8.9 e-/pF expected OK

Results in 180nm

- Process spreads: 3.3%



Preamp gain distribution



(Preamp + shaper) power distribution

Front-end in 130nm

Cooperation between LPNHE and LAPP Annecy

Why 130nm ?

- VLSI
- Will be dominant in industry in the next few years
- Faster
- Low power

But, it is also more difficult for low noise analog design

Technologies parameters

180 nm Mixed-mode process (including 3.3V transistors)

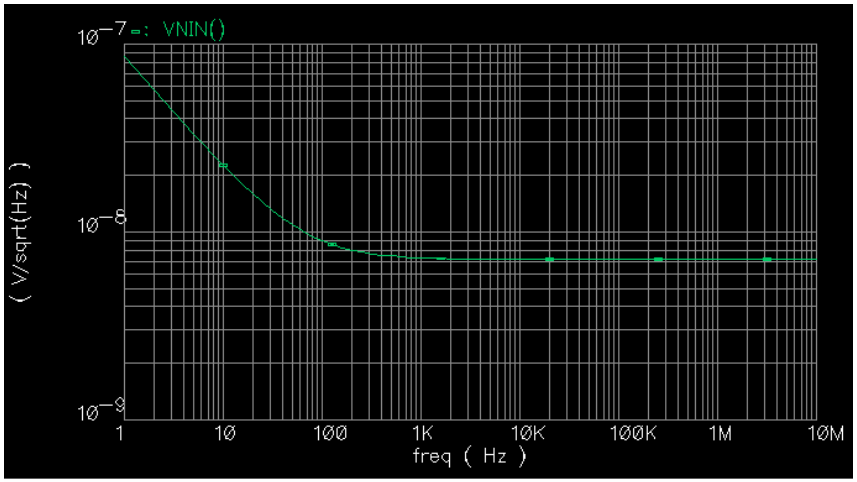
- 6 metals layers
- Cox = 0.0049 F/m² (Low voltage 3.3V transistor)
- Gate's minimum width= 0.5μm
- Metal/Metal capacitance = 1fF/μm²
- Various Vt options

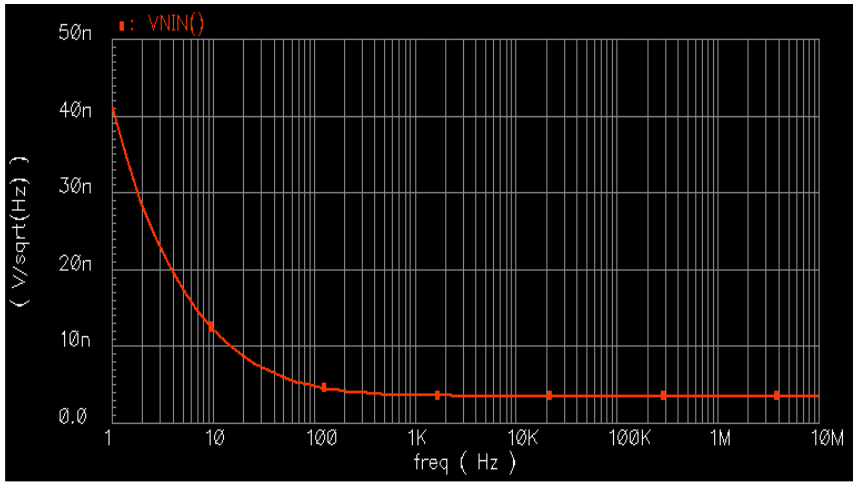
130nm Mixed-mode process (including 3V3 transistors)

- 8 metals layers
- Cox = 0.0048 F/m² (Low voltage 3.3V transistor)
- Gate's width minimum = 0.34μm
- Metal/Metal capacitance =1fF/um²
- Same Vt options

Noise: 130nm vs 180nm (simulation)

- **PMOS:**



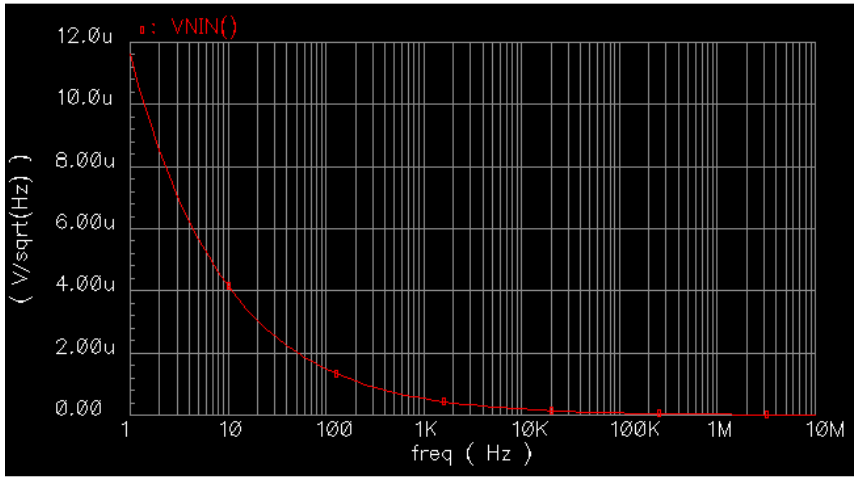


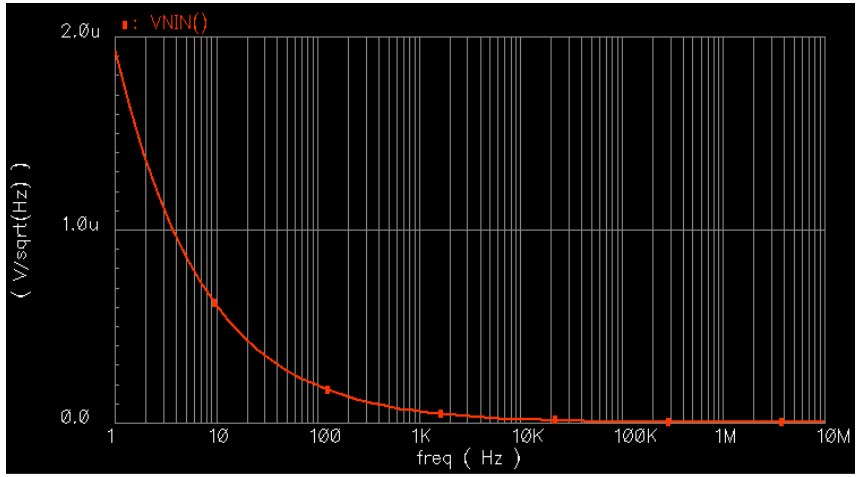
130nm
W/L = 2m/0.5u
Ids = 38.79u,Vgs=-190mV,Vds=-600mV
gm=815.245u,gms=354.118u,gds=4.44907u
1MHz → 7.16nV/sqrt(Hz)
Thermal noise hand calculation = 3.68nV/sqrt(Hz)

180nm
W/L=2m/0.5u
Ids=38.28uA,Vgs=-337mV,Vds=-0.6V
gm=944.4uS,gms=203.1uS,gds=10.2uS
1MHz --> 3.508nV/sqrt(Hz)
Thermal noise hand calculation = 3.42nV/sqrt(Hz)

Noise: 130nm vs 180nm (simulation)

- **NMOS :**

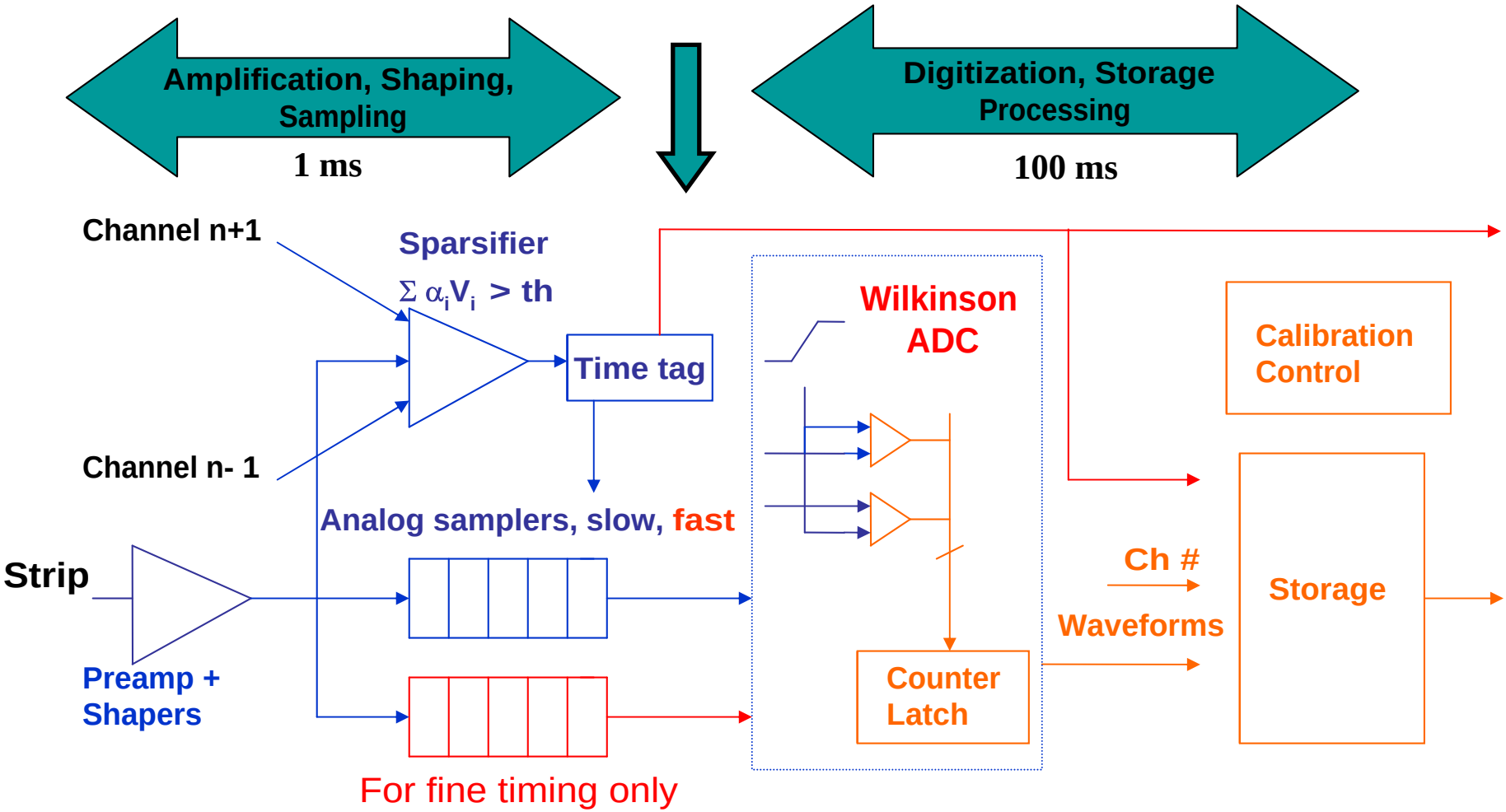




130nm
W/L = 50u/0.5u
Ids=48.0505u,Vgs=260mV,Vds=1.2V
gm=772.031uS,gms=245.341uS,gds=6.3575uS
1MHz --> 24.65nV/sqrt(Hz)
100MHz --> 5nV/sqrt(Hz)
Thermal noise hand calculation = 3.78nV/sqrt(Hz)

180nm
W/L=50u/0.5u
Ids=47uA,Vgs=300mV,Vds=1.2V
gm=842.8uS,gms=141.2uS,gds=16.05uS
1MHz --> 4nV/sqrt(Hz)
10MHz --> 3.49nV/sqrt(Hz)
Thermal noise hand calculation = 3.62nV/sqrt(Hz)

Architecture of 130nm chip



Charge 1- 40 MIP, S/N~ 15- 20
Time resolution ~ 2ns

Time-stamping on all detector layers
fine time resolution
on some layers: under study

Perspective

- The noise problem is under investigation
- If a solution is found, the chip is expected to be submitted mid-April

- Otherwise, goto:
  - CMOS IBM (less noise according to people from NIKHEF and Pavia) or
  - SiGe (1/f far better, thermal OK)